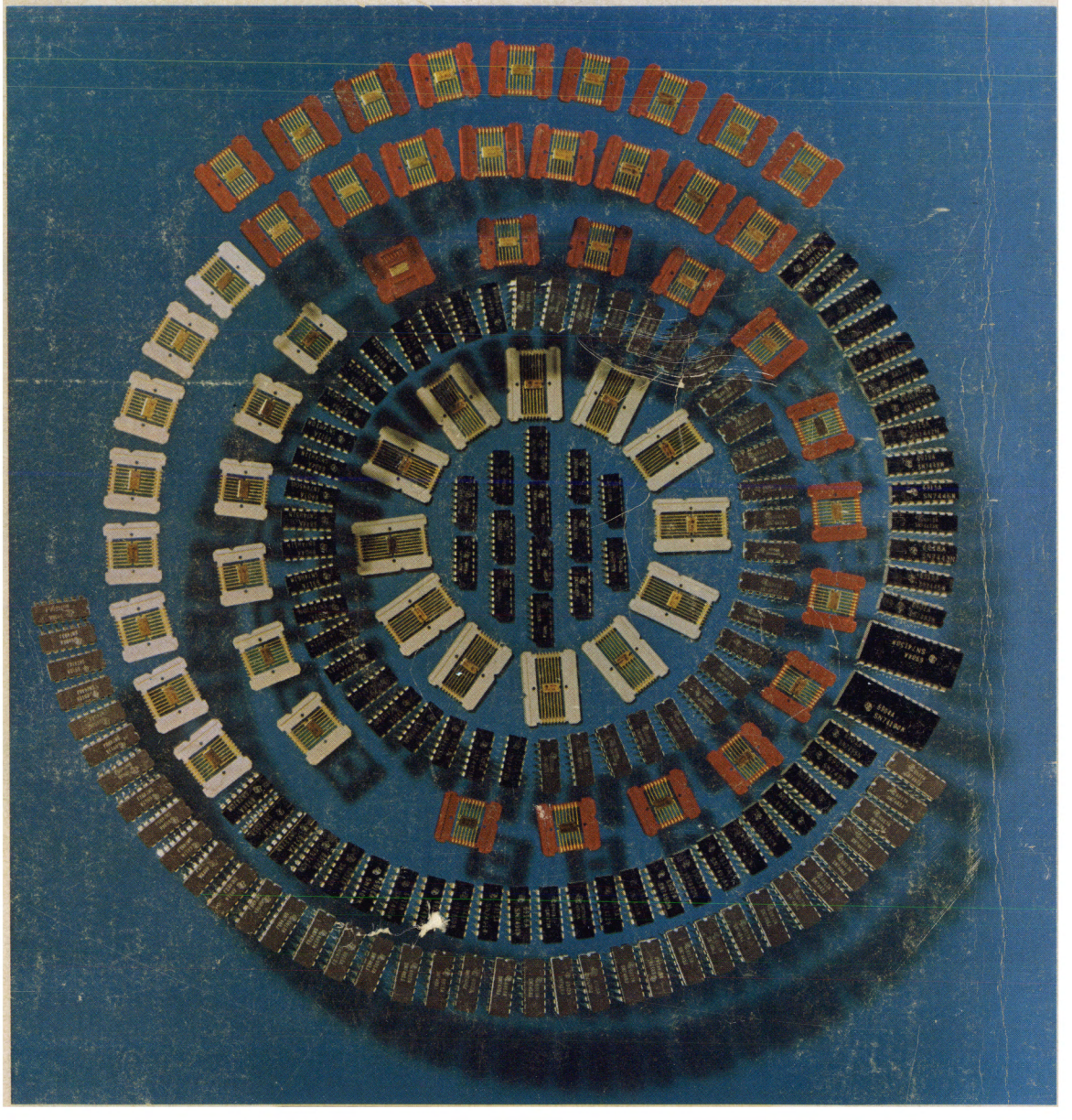
TTL Integrated Circuits Catalog from Texas Instruments



TTL
Integrated Circuits Catalog from Texas Instruments

1 August 1969

TEXAS INSTRUMENTS
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IMPORTANT NOTICES

Texas Instruments reserves the right to make changes at any time in order to improve design and to supply the best product possible.

TI cannot assume any responsibility for any circuits shown or represent that they are free from patent infringement.

YOUR TTL INTEGRATED CIRCUITS CATALOG

Texas Instruments is pleased to present important technical data for your use in evaluating and specifying Series 54/74 TTL digital integrated circuits.

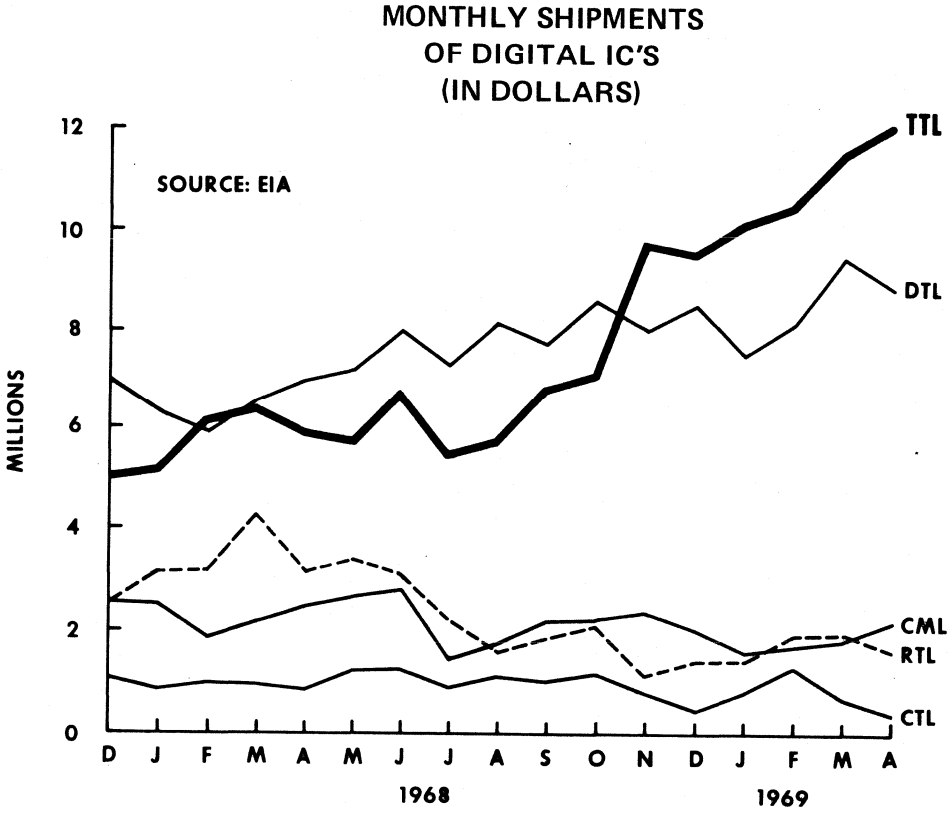
In Section A, you'll find indexes of TI TTL integrated circuits by circuit series (numerically), by functions with package choices indicated, and a cross-reference guide that lists TI's nearest pin-for-pin equivalent to competitive devices, and circuits recommended for new designs.

As the industry leader in TTL, TI has had the opportunity to help customers achieve optimum performance in their equipment and systems using TTL. As a result, TI engineers have authored a number of application reports that reflect their experience in using TTL at both design and application levels. Section B contains a description of these application reports which you may request from:

Texas Instruments Incorporated
Marketing and Information Services
P.O. Box 5012, M.S. 308
Dallas, Texas 75222

While this book contains data sheets exclusively for Series 54/74 TTL integrated circuits, we have listed in Section C the type numbers and descriptions for other popular TI integrated circuits including DTL, Linear, System Interface Circuits, MOS, and ECL. You may obtain technical information for individual circuits through our Marketing and Information Services at the address above. When ordering, please reference both type number and title for each data sheet you desire.

The following pages contain information of general interest concerning breadth-of-line, packaging, testing, and noise immunity of TTL integrated circuits from Texas Instruments.



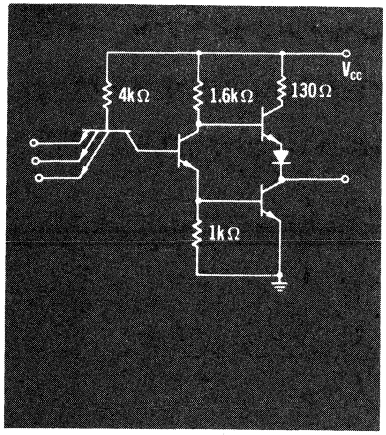
The Trend is TTL.

Series 54/74 TTL

The most complete IC logic family in the industry... and the first choice for new designs. Here's why:

- **Over 90 distinct functions to select from...including 35 MSI circuits**
- **Three compatible performance ranges**
  - **Series 54/74 standard**
  - **Series 54H/74H high speed**
  - **Series 54L/74L low power**
- **Three package configurations**
  - **Plastic dual-in-line**
  - **Ceramic dual-in-line**
  - **Metal flatpack**
- **Two temperature ranges**
  - **Series 54...−55° to +125°C**
  - **Series 74...0° to 70°C**

STANDARD SERIES 54/74 TTL

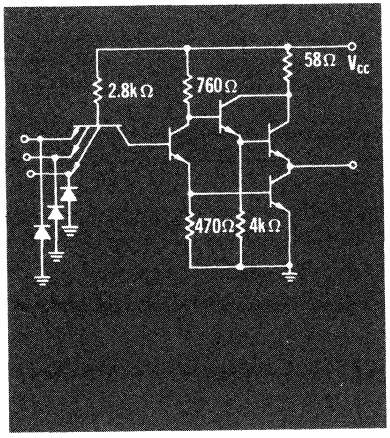


52 Standard TTL Circuits—featuring 10 ns speed and 10 mW per gate performance.
15 gate circuits
6 flip-flop circuits
1 Monostable Multivibrator
30 MSI circuits

Standard Series 54/74 integrated circuits offer a combination of speed and power dissipation best suited for most applications. At present, 52 circuits are offered in the standard line including 30 MSI functions.

Almost any type of MSI function is available, including shift registers, counters, decoders, memories, data selector circuits, and arithmetic elements. You also have a wide choice of flip-flops—single or dual, edge-triggered or master-slave, D-type or J-K inputs. A versatile one-shot is available as well as a wide variety of gate circuits, including open-collector output gates.

HIGH SPEED SERIES 54H/74H TTL



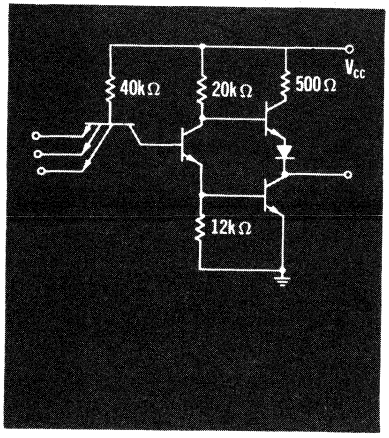
31 High–Speed TTL Circuits–featuring 6 ns speed and 22 mW per gate performance.
20 gate circuits
10 flip-flop circuits
1 MSI circuit
Diode-clamped inputs

Series 54H/74H high-speed TTL offers you six nanoseconds per gate performance. Applications include critical portions of digital systems such as high-speed computation and data processing sections.

31 circuit functions include both AND and NAND gates, plus single wire expanders so that you can design simple, less costly systems. In addition, open-collector output gates are offered to facilitate the wire-OR function.

Series 54H/74H includes five master-slave flip-flops and five edge-triggered flip-flops. The edge-triggered flip-flops will operate with clock input frequencies as high as 50 MHz.

LOW POWER SERIES 54L/74L TTL



16 Low Power TTL Circuits—featuring 1 mW and 33 ns per gate performance
8 gate circuits
4 flip-flop circuits
4 MSI functions

Series 54L/74L low-power TTL gives you the best speed/power product of any logic form today! These circuits feature power requirements less than one-tenth that of standard ICs. . .yet speeds are approximately twice as fast as other circuits with similar power dissipation. They are ideal for applications where power consumption and heat dissipation are critical. They may be combined with standard and high-speed TTL circuits to provide almost any desired speed/power combination the system designer requires.

A complete family of sixteen low-power TTL circuits are available—including dual flip-flops and MSI circuits.

GENERAL INFORMATION ABOUT TTL INTEGRATED CIRCUITS

Series 54/74 offers you the most complete IC logic family with a choice of over 90 distinct functions in three compatible performance ranges—Series 54/74, Series 54H/74H, and Series 54L/74L. These TTL families have been designed so that all three can interface directly with each other in the same system to provide your system with almost any speed/power dissipation combination. The following characteristics are common between the three families.

typical characteristics

- **Supply voltage** 5 V
- **Logical 0 output voltage** 0.2 V
- **Logical 1 output voltage** 3 V
- **Noise Immunity** 1 V
- **Temperature ranges:**
  - **Series 54/54H/54L** −55°C to 125°C
  - **Series 74/74H/74L** 0° to 70°C

Generalized loading guidelines for mixing these TTL circuits in the same system are given in Section 12.

design characteristics

Series 54/74 TTL digital integrated circuit families optimize the advantages of saturated logic circuitry and monolithic semiconductor technology, yielding improved performance in the speed/power ranges which meet the needs of current and future designs. In other forms of logic circuitry maximum use is made of lower cost passive components (diodes and resistors) instead of higher performance (and higher cost) transistors. However, in monolithic circuitry it costs very little more to build transistors than diodes or resistors; therefore, transistors are used to take advantage of the improved performance and also to buffer the fluctuations in currents that occur as resistor values change. The TTL multiple-emitter input transistor replaces conventional input diodes, and an active pull-up output transistor eliminates the slow rise times associated with passive pull-up.

Each low-capacitance emitter of the input transistor offers very little loading to the driving circuit. In addition to providing some gain when this transistor is turned on (one or more emitters at a low voltage), a low impedance path [approximately $V_{CE(sat)}$] is established to remove the base charge from and turn off the phase-splitter transistor. When compared to a passive-component input, the TTL input is considerably faster.

Another important feature which reduces overall switching time of the TTL circuit is the active pull-up output. In addition to reducing the turn-off time, the double-ended output provides a low-impedance path in both the logical 0 and logical 1 states for sourcing or sinking current to highly capacitive loads and for rejecting capacitively-coupled a-c noise.

A comparison of typical saturated digital logic family speed/power products is shown in Table 1 and Figure A.

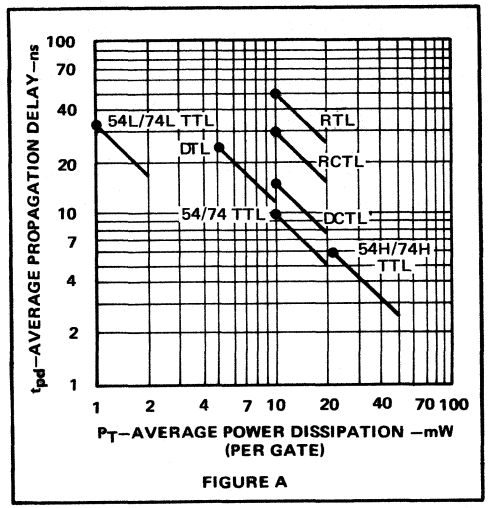


FIGURE A

TABLE 1

Circuit	Logic Type	t_{pd}(ns)	P_T (mW)	Speed/ Power Product	Typical Fan-Out
54L/74L TTL	NAND	33	1	33	10
54/74 TTL	NAND	10	10	100	10
54H/74H TTL	NAND	6	23	138	10
DTL	NAND	25	5	125	8
DCTL	NOR	15	10	150	3
RCTL	NOR	30	10	300	4
RTL	NOR	50	10	500	4

WORST-CASE TESTING

Specification sheets can be misleading unless test conditions are clearly stated. One of the most important but least apparent benefits of Series 54/74 TTL ICs is the guarantee that worst-case test conditions are used when specifications are prepared. The data sheets verify these worst-case test conditions, including supply currents which are specified at maximum supply voltages.

worst-case temperature

All d-c limits shown on the data sheet are guaranteed over the entire temperature range (−55°C to +125°C for Series 54 and 0°C to 70°C for Series 74). Texas Instruments guarantees one value over a temperature range since the designer is limited by whatever happens to be the worst value of a particular parameter regardless of the temperature at which it occurs.

worst-case loading

For a logical one output voltage test, a guaranteed fan-out of ten is simulated by drawing at least ten times the current drawn by a worst-case input.

For example: 400 μA is drawn from the output of a Series 54/74 gate. Since an input at 2.4 V can draw no more than 40 μA, the 400 μA drain represents a worst-case normalized fan-out of 10. Similarly, in the logical zero state, current equal to a worst-case fan-out of ten is "sunk" into the lower output transistor. See Figure B.

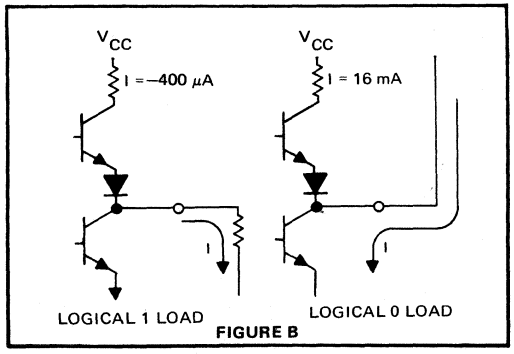


FIGURE B

worst-case supply voltage

The logical one output voltage follows changes in the supply voltage practically volt-for-volt; therefore, when measuring logical one output levels, the worst-case supply voltage is the lowest allowable: 4.5 V for Series 54 and 4.75 V for Series 74.

Similarly, the low supply voltage limit is used when a logical zero output is tested since the lower voltage reduces the base drive to the output transistor and makes it more difficult to keep the transistor in saturation. See Figure C.

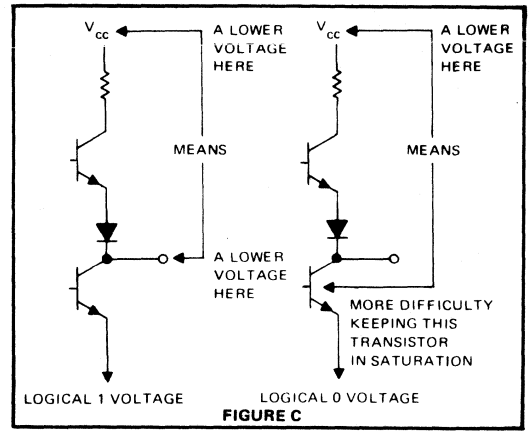


FIGURE C

Requirements are different, though, when an input is tested. Here, the high-limit power supply voltage is used . . . 5.5 V for Series 54 and 5.25 V for Series 74 since the higher voltage results in more current into and out of the input. See Figure D.

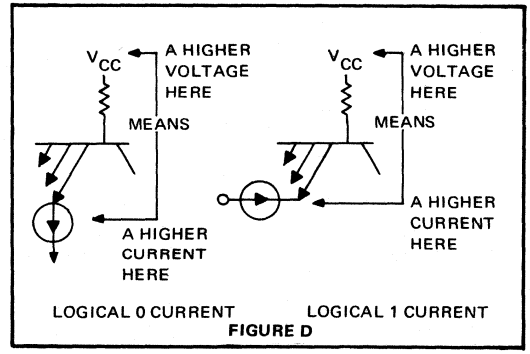


FIGURE D

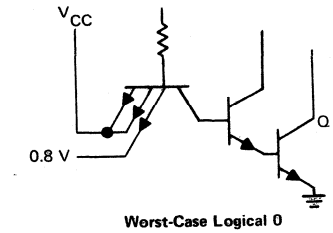
worst-case supply voltage (continued)

These tests are extreme since supply voltages remain generally constant throughout any given system, but worst-case testing here gives added assurance of reliable system operation.

worst-case conditions on unused inputs

In addition to selecting worst-case supply voltages for various output conditions, worst-case voltages are also applied to the unused inputs as shown in the illustrations.

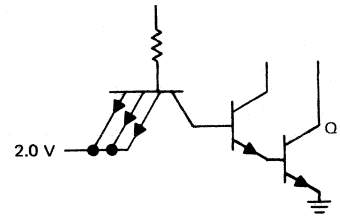
When a worst-case logical zero (0.8 V) is applied to an input—and where that voltage is required to hold the output transistor Q in the off state—unused inputs are returned to the maximum supply voltage. This represents the worst-case condition since these high voltages would tend to turn on the transistor Q if it were not for the low input. See Figure E.



Worst-Case Logical 0

FIGURE E

When a minimum logical one (2.0 V) is applied to an input to turn on the output transistor Q, the worst case is to hold all other inputs at the minimum logical one voltage which is 2.0 V. Therefore, all inputs are tied together and taken to this voltage. See Figure F.



Worst-Case Logical 1

FIGURE F

worst-case supply current

Power-supply current requirements for all Series 54/74 TTL circuits are specified as maximum current drains with power-supply voltage at V_{CC} = MAX. When power supply currents are specified at the nominal V_{CC} (5 volts), the true worst-case current drain is not obtained. I_{CC} at nominal V_{CC} is, in fact, approximately 91% of the worst-case value, and the resulting power dissipation is approximately 82% of the worst-case value.

In summary, worst-case testing of every parameter may result in figures that look less impressive than those obtained with more typical testing, but it gives you extra assurance that every circuit will perform correctly in your system, under worst-case conditions.

NOISE IMMUNITY

Noise immunity is a vital consideration when evaluating integrated circuits since noise can, under certain conditions, falsely trigger gates and introduce errors into the system.

In order to avoid confusion, it is necessary to examine and evaluate all sources of noise and to determine how they affect the performance of Series 54/74 TTL integrated circuits in actual systems. Some of the considerations include:

1. Relative importance of a-c and d-c noise
2. Impedance effects and capacitively coupled noise
3. Supply voltage noise
4. Ground noise
5. Difference between typical and guaranteed noise immunity

Let's examine each of these considerations separately.

a-c or d-c noise

It is difficult to define a-c noise and even more difficult to relate it to a specification. Generally, d-c noise is worst case. When noise immunity is plotted against pulse width, it can be shown that the circuit is more immune to noise as pulse width decreases. See Figure G.

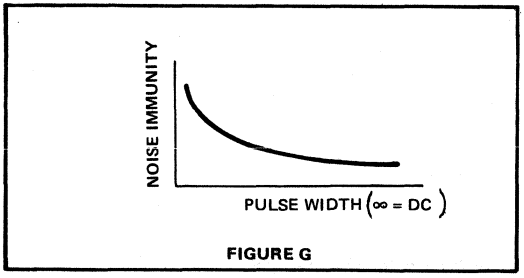


FIGURE G

When discussing a-c noise, the term "noise susceptibility" is more appropriate than "noise immunity." One of the more important advantages of Series 54/74 TTL is its . . .

. . .low logical one a-c noise susceptibility

An important feature of the design is the output configuration which both supplies current (in the logical 1 state) and sinks current (in the logical 0 state) from a low impedance. Typically, logical 0 output impedance is 12 Ω and logical 1 output impedance is 70 Ω for standard Series 54/74 circuits. See Figure H. This low output impedance in either state rejects capacitively coupled a-c pulses and ensures small R-C time constants which preserve waveshape integrity.

This means a-c noise susceptibility is far better than logic circuits which have 2000-ohm logical one output impedances.

As a result, Series 54/74 TTL is much more effective than other forms of logic at preventing noise from ever appearing at the output. In addition, it has high immunity to d-c noise from supply voltage and ground sources.

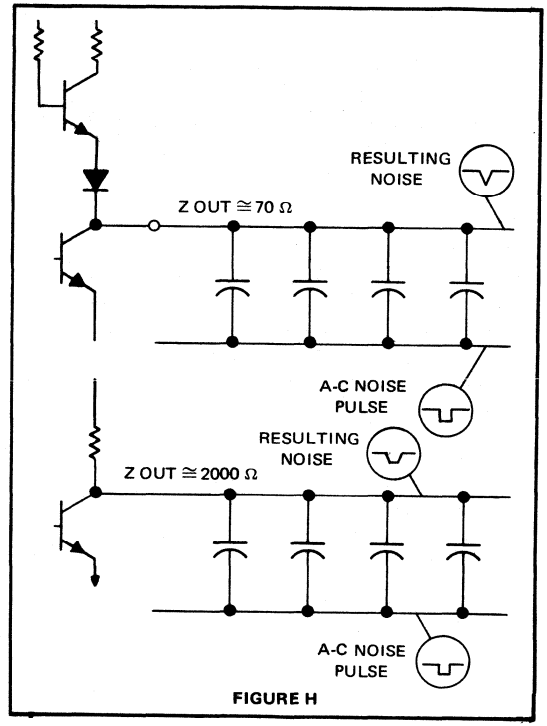


FIGURE H

supply voltage noise

Notice that the output of a Series 54/74 gate, Figure I, is similar to an emitter-follower circuit. For loads even considerably higher than fan-outs of ten, the Transistor Q_1 does not saturate when the gate is in the logical one state. Therefore:

$$V_{OUT} = V_{CC} - IR - V_{BE}(Q_1) - V_D$$

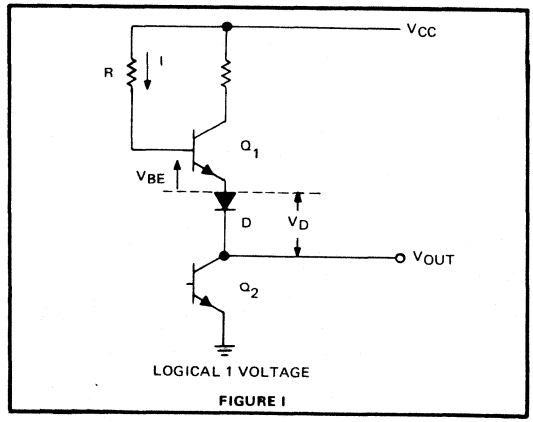


FIGURE I

As voltage changes across the resistor R, the base-emitter junction of Q_1, and the diode are small, the output voltage follows the supply voltage very closely in the logical one state. A negative voltage change on the supply line is reflected almost directly to the signal output line.

The high logical one d-c noise immunity reduces the probability of false triggering due to supply voltage variation.

ground line noise

In the logical zero state, Q_2 saturates and a positive transition on the ground line is seen on the signal line.

Therefore, both supply voltage noise and ground line noise appear as signal line noise. Thus, the treatment of d-c noise can be discussed comprehensively by concentrating on the signal line only.

typical d-c noise immunity

Series 54/74 gates change state as the changing input voltage passes through an approximate 1.4 volt threshold. The output is typically 3.3 volts in the logical one state (see Figure J) and 0.2 volt in the logical zero state. Therefore, the output can typically tolerate 1.9 volts of negative-going noise in the one state and 1.2 volts of positive-going noise in the zero state before causing the gate it is driving to falsely trigger. In both states, Series 54/74 has more than one volt typical noise immunity. See Figure K.

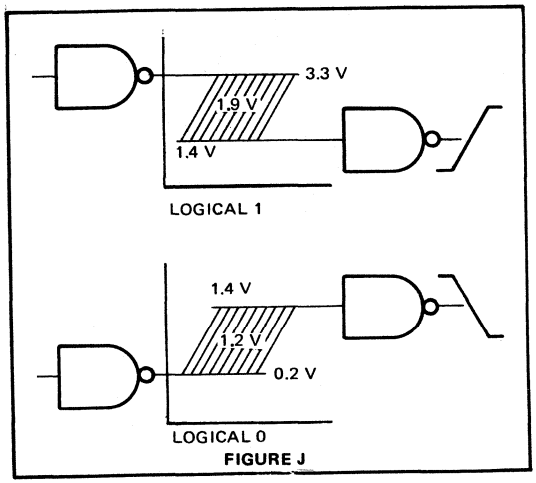


FIGURE J

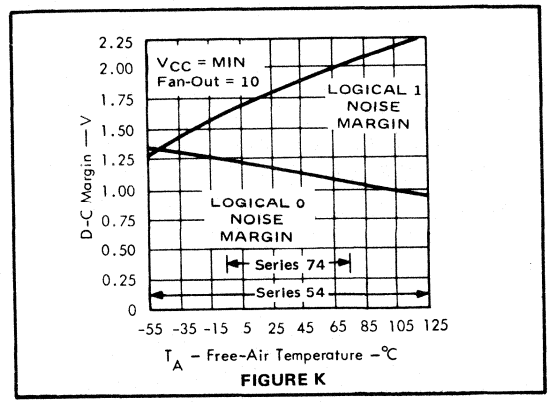


FIGURE K

guaranteed d-c noise immunity

Simply stating that a circuit will not falsely trigger is not an adequate guarantee for a design engineer. The manufacturer must also guarantee an absolute output voltage limit which will not be exceeded when noise is applied to an input. Figure L shows these guaranteed voltages.

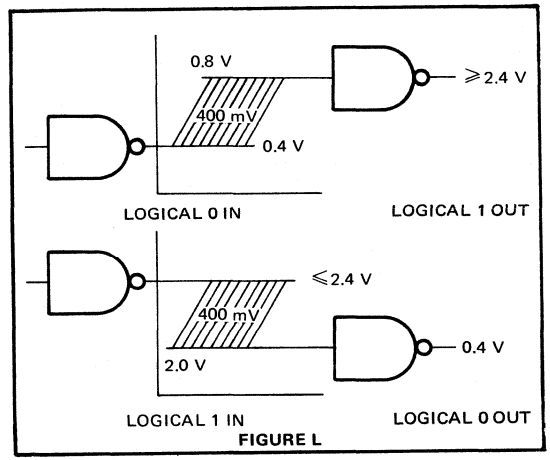


FIGURE L

The logical zero input test voltage is 0.8 volt, and TI guarantees a maximum logical zero output of 0.4 volt which gives a guaranteed noise immunity of 400 millivolts.

Likewise, the logical one input test condition is 2.0 volts which is 0.4 volt below the guaranteed minimum logical one output of 2.4 volts.

In both states, guaranteed noise immunity is 400 millivolts.

The following represent rule-of-thumb answers to questions regarding the use of TTL circuits. These should not be adhered to on an absolute basis; rather, they should be treated as guidelines.

GENERAL	
Power supply	Maintain ripple $\leq$ 5%. Maintain regulation $\leq$ 5%. R-F bypass supply primary.
Decoupling	Decouple every 5 to 10 packages with r-f capacitors of 0.01 to 0.1 μf.
Grounding	A ground plane is desirable, especially when the p-c board contains a large number of packages. If no ground plane is used, incorporate ground bus around p-c board periphery where possible. Make ground bus as wide as possible. Always return both ends of long ground bus to common point (system ground).
GATES	
Data input rise and fall times.	Reduce as driver output impedance increases. Should be no greater than 1 μsec for $Z_o \geq$ 100 ohms.
Unused inputs of AND and NAND gates and unused preset and clear inputs of flip-flops.	Tie directly to $+V_{cc}$ where V_{cc} is guaranteed to **always** be $\leq$ 5.5 v; or Tie to V_{cc} through resistor $\geq$ 1K ohms. Several unused inputs can be tied to one resistor; or Tie to used input of same gate if maximum fan-out of driving device will not be exceeded; or Tie to unused gate output where unused gate input is grounded.
Unused inputs of NOR gates.	Tie to used input of same gate if max fan-out of driving device will not be exceeded; or Tie to ground.
Unused gates.	Tie inputs of unused gates to ground for lowest power drain.
Increasing gate/buffer fan-out.	Parallel gates/buffers of same package.
Expanders.	Place expanders as close as possible to the gate being expanded and avoid capacitive loading of the expander nodes if switching speed is to be maintained.
FLIP-FLOPS	
Preset and clear pulses.	If clock pulse is present, maintain preset or clear pulse until clock pulse goes low.

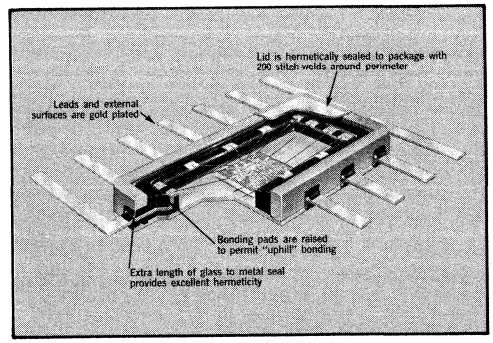
FLIP-FLOPS (Contd.)	
Clock pulse.	Rise and fall times should be less than 150 nsec to improve noise immunity.
Input data.	In general, input data of master-slave J-K flip-flops should not be changed while the clock pulse is high. Consult data sheet for possible exceptions.
LINE DRIVING AND RECEIVING	
Single-wire interconnections.	May be used up to approximately 10" without particular precaution. A ground plane is always desirable. If longer than 10", ground plane is mandatory with wire routed as close to it as possible. Use twisted pair or coax lengths exceeding 20".
Coaxial and twisted pair cables.	Design around approximately 100 ohms characteristic impedance. Higher impedances increase crosstalk while lower impedances are difficult to drive. a. coaxial cable of 93 ohms impedance (such as Microdot 293-3913) is recommended; b. for twisted pair, Nos. 26 or 28 wire with thin insulation twisted about 30 turns/foot work well.
Transmission-line ground.	Ensure that transmission-line ground returns are carried through at both transmitting and receiving ends.
Resistive pull-up.	Use 500 to 1,000 ohms resistive pull-up at **receiving** end of long cables for added noise margin and more rapid rise times.
Line termination	Reverse terminate with 27 to 47 ohms at **driving** end in series with the line to prevent negative overshoot.
Gates as line drivers.	Drive into only one transmission-line terminated with one gate input. Adverse effects from multiple loads include: a. erroneous signals due to line reflections; b. long delay times; c. excessive driver loading.
Gates as line receivers.	Use only one gate input to terminate line. Follow unused input rules for receiver gates.
Flip-flops as line drivers.	Generally unsatisfactory due to the possibility of collector commutation from reflected signals.
Decoupling.	Always decouple driving/receiving devices in addition to normal decoupling. Use 0.1 μf r-f capacitors located at V_{cc} and ground pins.

PACKAGES

In addition to over 90 different circuits, three speed ranges, and a broad selection of MSI circuits, Series 54/74 TTL is offered in three basic package configurations.

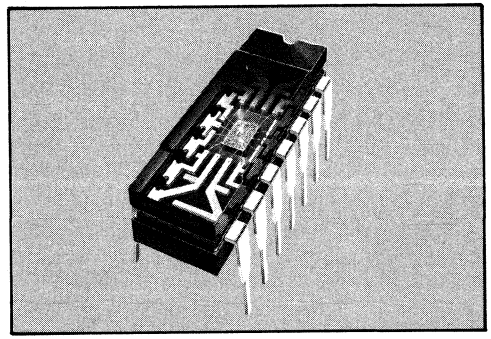
flatpack

TI's flatpacks—best for space-critical applications—are backed by ten years of service in all types of military, space, and commercial systems.



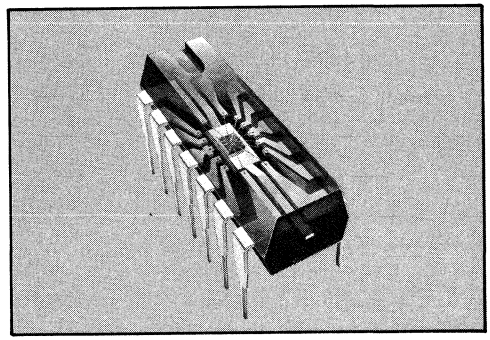
ceramic dual-in-line

Ceramic dual-in-line packages from TI provide all the benefits of hermetic packages in a design suited to automatic insertion and soldering. Ceramic packages are ideal for severe environments where specifications require hermeticity to be tested.



plastic dual-in-line

TI's plastic dual-in-line packages are rugged and low in cost. They are backed by millions of device-hours of reliability data. Series 54 plastic performance over the full temperature range (−55°C to 125°C) has been proven by customer usage in temperature-critical systems.



See Section 1 for detailed information.

NUMERIC INDEX
FULL MILITARY TEMPERATURE RANGE CIRCUITS: −55°C TO 125°C

NUMERIC INDEX
INDUSTRIAL TEMPERATURE RANGE CIRCUITS: 0°C TO 70°C

SERIES 54/74
FEATURING 10 ns SPEED AND 10 mW PER GATE PERFORMANCE
SMALL SCALE INTEGRATION (SSI)

FUNCTION	OPERATING TEMPERATURE RANGES		PACKAGES* Dual-In-Line		Flat	SEC.–PAGE
NAND/NOR GATES	–55°C to 125°C	0°C to 70°C	J	N	S	
Quadruple 2-Input Positive NAND Gates	SN5400	SN7400	•	•	•	2–5
Quadruple 2-Input Positive NAND Gates (with Open-Collector Output)	SN5401	SN7401	•	•	•	2–6
Quadruple 2-Input Positive NOR Gates	SN5402	SN7402	•	•	•	2–9
Quadruple 2-Input Positive NAND Gates (with Open-Collector Output)	SN5403	SN7403	•	•		2–10
Hex Inverters	SN5404	SN7404	•	•	•	2–11
Hex Inverters (with Open-Collector Output)	SN5405	SN7405	•	•	•	2–12
Triple 3-Input Positive NAND Gates	SN5410	SN7410	•	•	•	2–13
Dual 4-Input Positive NAND Gates	SN5420	SN7420	•	•	•	2–14
8-Input Positive NAND Gates	SN5430	SN7430	•	•	•	2–15
Dual 4-Input Positive NAND Buffers	SN5440	SN7440	•	•	•	2–16
AND-OR-INVERT GATES						
Expandable Dual 2-Wide 2-Input AND-OR-INVERT Gates	SN5450	SN7450	•	•	•	2–17
Dual 2-Wide 2-Input AND-OR-INVERT Gates	SN5451	SN7451	•	•	•	2–17
Expandable 4-Wide 2-Input AND-OR-INVERT Gates	SN5453	SN7453	•	•	•	2–19
4-Wide 2-Input AND-OR-INVERT Gates	SN5454	SN7454	•	•	•	2–19
EXPANDERS						
Dual 4-Input Expander	SN5460		•	•	•	2–21
Dual 4-Input Expander		SN7460	•	•	•	2–22
FLIP-FLOPS						
Positive Edge-Triggered J-K Flip-Flops (AND Inputs)	SN5470	SN7470	•	•	•	2–23
J-K Master Slave Flip-Flops (AND Inputs)	SN5472	SN7472	•	•	•	2–26
Dual J-K Master Slave Flip-Flops	SN5473	SN7473	•	•	•	2–29
Dual J-K Master Slave Flip-Flops (V_{CC}-14, Gnd 7)	SN54107	SN74107	•	•		2–29
Dual D-Type Edge-Triggered Flip-Flops	SN5474	SN7474	•	•	•	2–32
Dual J-K Master Slave Flip-Flops with Preset and Clear	SN5476	SN7476	•	•		2–35
Monostable Multivibrators	SN54121	SN74121	•	•	•	2–38

*For outline drawings of all packages, see Section I.

SERIES 54H/74H
FEATURING 6 ns SPEED AND 22 mW PER GATE PERFORMANCE
SMALL SCALE INTEGRATION (SSI)

*For outline drawings of all packages, see Section I.

SERIES 54H/74H
FEATURING 6 ns SPEED AND 22 mW PER GATE PERFORMANCE
SMALL SCALE INTEGRATION (SSI) (Continued)

FUNCTION	OPERATING TEMPERATURE RANGE –55°C to 125°C	OPERATING TEMPERATURE RANGE 0°C to 70°C	PACKAGES* Dual-In-Line J	PACKAGES* Dual-In-Line N	PACKAGES* Flat S	SEC.–PAGE
FLIP-FLOPS						
J-K Master-Slave Flip-Flops (AND-OR Inputs)	SN54H71	SN74H71	•	•	•	3–31
J-K Master-Slave Flip-Flops (AND Inputs)	SN54H72	SN74H72	•	•	•	3–34
Dual J-K Master-Slave Flip-Flops	SN54H73	SN74H73	•	•	•	3–37
Dual J-K Master-Slave Flip-Flops with Preset and Clear	SN54H76	SN74H76	•	•		3–40
Dual J-K Master-Slave Flip-Flops (Common Clock)	SN54H78	SN74H78	•	•	•	3–43
J-K Negative Edge-Triggered Flip-Flops with AND-OR Inputs (50 MHz)	SN54H101	SN74H101	•	•	•	3–46
J-K Negative Edge-Triggered Flip-Flops with AND Inputs (50 MHz)	SN54H102	SN74H102	•	•	•	3–49
Dual J-K Negative Edge-Triggered Flip-Flops (50 MHz)	SN54H103	SN74H103	•	•	•	3–52
Dual J-K Negative Edge-Triggered Flip-Flops (50 MHz) with Preset and Clear	SN54H106	SN74H106	•	•		3–55
Dual J-K Negative Edge-Triggered Flip-Flops (50 MHz) (Common Clock)	SN54H108	SN74H108	•	•	•	3–58

SERIES 54L/74L
FEATURING 1 mW AND 33 ns PER GATE PERFORMANCE
SMALL SCALE INTEGRATION (SSI)

FUNCTION	OPERATING TEMPERATURE RANGE –55°C to 125°C	OPERATING TEMPERATURE RANGE 0°C to 70°C	PACKAGES* Dual-In-Line J	PACKAGES* Dual-In-Line N	PACKAGES* Flat T	SEC.–PAGE
NAND/NOR GATES						
Quadruple 2-Input Positive NAND gates	SN54L00	SN74L00	•	•	•	4–4
Hex Inverters	SN54L04	SN74L04	•	•	•	4–5
Triple 3-Input Positive NAND Gates	SN54L10	SN74L10	•	•	•	4–6
Dual 4-Input Positive NAND Gates	SN54L20	SN74L20	•	•	•	4–7
8-Input Positive NAND Gates	SN54L30	SN74L30	•	•	•	4–8
AND-OR-INVERT GATES						
Dual 2-Wide AND-OR-INVERT Gates	SN54L51	SN74L51	•	•	•	4–9
4-Wide 3-2-2-3-Input AND-OR-INVERT Gates	SN54L54	SN74L54	•	•	•	4–10
2-Wide 4-Input AND-OR-INVERT Gates	SN54L55	SN74L55	•	•	•	4–11
FLIP-FLOPS						
R-S Master-Slave Flip-Flops	SN54L71	SN74L71	•	•	•	4–12
J-K Master-Slave Flip-Flops	SN54L72	SN74L72	•	•	•	4–15
Dual J-K Master-Slave Flip-Flops	SN54L73	SN74L73	•	•	•	4–18
Dual J-K Master-Slave Flip-Flops (Common Clock)	SN54L78	SN74L78	•	•	•	4–21

*For outline drawings of all packages, see Section I.

TTL
MEDIUM-SCALE INTEGRATION (MSI)

FUNCTION	OPERATING TEMPERATURE RANGE		PACKAGES*			
			Dual-In-Line		Flat	
DECODERS	–55°C to 125°C	0°C to 70°C	J	N	S	SECTION–PAGE
BCD-to-Decimal Decoder/Driver		SN7441A	•	•		5–1
BCD-to-Decimal Decoders (4-to-10 lines, 1-of-10)	SN5442	SN7442	•	•		5–7
Excess-3-to-Decimal Decoders (4-to-10 lines, 1-of-10)	SN5443	SN7443	•	•		5–7
Excess-3-Gray-to-Decimal Decoders (4-to-10-lines, 1-of-10)	SN5444	SN7444	•	•		5–7
BCD-to-Decimal Decoder/Drivers (30-V Outputs)	SN5445	SN7445	•	•		5–13
BCD-to-Decimal Decoder/Drivers (15-V Outputs)	SN54145	SN74145	•	•		5–13
BCD-to-Seven-Segment Decoder/Drivers (30-V Outputs)	SN5446	SN7446	•	•		5–19
BCD-to-Seven-Segment Decoder/Drivers (15-V Outputs)	SN5447	SN7447	•	•		5–19
BCD-to-Seven-Segment Decoder/Drivers	SN5448	SN7448	•	•		5–19
BCD-to-Seven-Segment Decoder/Drivers	SN5449	SN7449			•	5–19
MEMORIES/LATCHES						
4-Bit Bistable Latches	SN5475	SN7475	•	•		6–1
4-Bit Bistable Latches	SN5477	SN7477			•	6–1
8-Bit Bistable Latches	SN54100	SN74100		•		6–1
16-Bit Active Element Memories	SN5481	SN7481	•	•	•	6–9
16-Bit Active Element Memories	SN5484	SN7484	•	•		6–9
ARITHMETIC ELEMENTS						
Gated Full Adders	SN5480	SN7480	•	•	•	7–1
2-Bit Binary Full Adders	SN5482	SN7482	•	•	•	7–11
4-Bit Binary Full Adders	SN5483	SN7483	•	•		7–19
Quadruple 2-Input Exclusive-OR Gates	SN5486	SN7486	•	•	•	7–27
Quadruple 2-Input Exclusive-OR Gates (Low Power)	SN54L86	SN74L86	•	•	•	7–31
4-Bit True/Complement, Zero/One Element	SN54H87	SN74H87	•	•	•	7–35

*For outline drawings of all packages, see Section I.

TTL
MEDIUM-SCALE INTEGRATION (MSI) (Continued)

FUNCTION	OPERATING TEMPERATURE RANGE		PACKAGES* Dual-In-Line		Flat	
	–55°C to 125°C	0°C to 70°C	J	N	S	SECTION–PAGE
COUNTERS						
Decade Counters	SN5490	SN7490	•	•	•	8–1
Divide-by-Twelve Counters	SN5492	SN7492	•	•	•	8–7
4-Bit Binary Counters	SN5493	SN7493	•	•	•	8–13
4-Bit Binary Counters (Low Power)	SN54L93	SN74L93	•	•	•	8–19
SHIFT REGISTERS						
8-Bit Shift Registers	SN5491A	SN7491A	•	•	•	9–1
8-Bit Shift Registers (Low Power)	SN54L91	SN74L91	•	•	•	9–7
4-Bit Shift Registers (Parallel-In, Serial-Out)	SN5494	SN7494	•	•	•	9–13
4-Bit Right-Shift/Left-Shift Registers (Low Power)	SN54L95	SN74L95	•	•	•	9–17
4-Bit Right-Shift/Left-Shift Registers	SN5495	SN7495	•	•		9–25
5-Bit Shift Registers (Dual-Parallel-In, Parallel-Out)	SN5496	SN7496	•	•		9–33
DATA SELECTORS/MULTIPLEXERS						
16-Bit Data Selectors	SN54150	SN74150		•		10–1
8-Bit Data Selectors (with Strobe)	SN54151	SN74151	•	•		10–1
8-Bit Data Selectors	SN54152	SN74152			•	10–1
PARITY GENERATOR/CHECKER						
8-Bit Odd/Even Parity Generator/Checkers	SN54180	SN74180	•	•	•	11–1

*For outline drawings of all packages, see Section I.

TTL CROSS-REFERENCE GUIDE

(alphabetically by manufacturers)

Nearest TI replacements were selected on the basis of the general similarity of electrical and mechanical characteristics. Interchangeability in particular applications is not guaranteed. Before using a substitute, the user should compare the detailed specifications of the substitute device with the detailed specifications of the original device. The third column lists TI Series 54/74 TTL integrated circuits which are recommended for new designs.

TI makes no warranty as to the information furnished and buyer assumes all risk in the use thereof. No liability is assumed for damages resulting from the use of the information contained in this list.

Fairchild

Type Number	Nearest TI Replacement	Recommended for New Designs	Sec.– Page
U31900251X		SN54H00S	3-5
U31900259X		SN74H00S	3-5
U31900351X		SN54H10S	3-11
U31900359X		SN74H10S	3-11
U31900451X		SN54H20S	3-13
U31900459X		SN74H20S	3-13
U31900551X		SN54H50S	3-18
U31900559X		SN74H50S	3-18
U31900651X		SN54H60S	3-26
U31900659X		SN74H60S	3-27
U31900751X		SN54H30S	3-16
U31900759X		SN74H30S	3-16
U31900851X		SN54H53S	3-22
U31900859X		SN74H53S	3-22
U31900951X		SN54H40S	3-17
U31900959X		SN74H40S	3-17
U31901451X		SN5486S	7-27
U31901459X		SN7486S	7-27
U31901551X		SN5402S	2-9
U31901559X		SN7402S	2-9
U31901651X		SN54H04S	3-9
U31901659X		SN74H04S	3-9
U31902051X		SN54H73S	3-37
U31902059X		SN74H73S	3-37
U31902051X		SN5474S	2-32
U31902059X		SN7474S	2-32
U31960151X		SN54121S	2-38
U31960159X		SN74121S	2-38
U3L930051X		SN5495S	9-25
U3L930059X		SN7495S	9-25
U3L930451X		SN5482S	7-11
U3L930459X		SN7482S	7-11
U3L930751X		SN5449S	5-19
U3L930759X		SN7449S	5-19
U3L931251X		SN54152S	10-1
U3L931259X		SN74152S	10-1
U3L931451X		SN5477S	6-1
U3L931459X		SN7477S	6-1
U3L932651X		SN5491AS	9-1
U3L932659X		SN7491AS	9-1
U6A900251X	SN54H00J	SN54H00J	3-5
U6A900259X	SN74H00J	SN74H00J	3-5
U6A900351X	SN54H10J	SN54H10J	3-11
U6A900359X	SN74H10J	SN74H10J	3-11
U6A900451X	SN54H20J	SN54H20J	3-13
U6A900459X	SN74H20J	SN74H20J	3-13
U6A900551X	SN54H50J	SN54H50J	3-18
U6A900559X	SN74H50J	SN74H50J	3-18
U6A900651X	SN54H60J	SN54H60J	3-26
U6A900659X	SN74H60J	SN74H60J	3-27
U6A900751X	SN54H30J	SN54H30J	3-16
U6A900759X	SN74H30J	SN74H30J	3-16
U6A900851X	SN54H53J	SN54H53J	3-22
U6A900859X	SN74H53J	SN74H53J	3-22
U6A900951X	SN54H40J	SN54H40J	3-17
U6A900959J	SN74H40J	SN74H40J	3-17
U6A901451X		SN5486J	7-27
U6A901459X		SN7486J	7-27
U6A901551X		SN5402J	2-9
U6A901559X		SN7402J	2-9
U6A901651X	SN54H04J	SN54H04J	3-9
U6A901659X	SN74H04J	SN74H04J	3-9
U6A960151X		SN54121J	2-38
U6A960159X		SN74121J	2-38
U6B930051X		SN5495J	9-25
U6B930059X		SN7495J	9-25
U6B930151X		SN5442J	5-7
U6B930159X		SN7442J	5-7
U6B930251X		SN5480J	7-1
U6B930259X		SN7480J	7-1
U6B930451X		SN5482J	7-11
U6B930459X		SN7482J	7-11
U6B930751X	SN5448J	SN5446,7J	5-19
U6B930759X	SN7448J	SN7446,7J	5-19
U6B931251X		SN54151J	10-1
U6B931259X		SN74151J	10-1
U6B931451X		SN5475J	6-1
U6B931459X		SN7475J	6-1
U6B931751X	SN5446J	SN5446J	5-19
U6B931759X	SN7446J	SN7446J	5-19
U6B932851X		SN5491AJ	9-1
U6B932859X		SN7491AJ	9-1
U6N930851X		SN54100N	6-1
U6N930859X		SN74100N	6-1

Motorola

Type Number	Nearest TI Replacement†	Recommended for New Designs	Sec.–Page
MC400F	SNG42R	SN7420S	2-14
MC400P	SNG42J,N	SN7420N	2-14
MC401F	SNG52R	SN7453S	2-19
MC401P	SNG52J,N	SN7453N	2-19
MC402F	SNG62R	SN7430S	2-15
MC402P	SNG62J,N	SN7430N	2-15
MC408F	SNG142R	SN7400S	2-5
MC408P	SNG142J,N	SN7400N	2-5
MC411F	SNG182R	SN7460S	2-21
MC411P	SNG182J,N	SN7460N	2-21
MC412F	SNG192R	SN7410S	2-13
MC412P	SNG192J,N	SN7410N	2-13
MC415F	SNF52R	SN7470S	2-23
MC415P	SNF52J,N	SN7470N	2-23
MC420F	SNG72R	SN7450S	2-17
MC420P	SNG72J,N	SN7450N	2-17
MC450F	SNG43R	SN7420S	2-14
MC450P	SNG43J,N	SN7420N	2-14
MC451F	SNG53R	SN7453S	2-19
MC451P	SNG53J,N	SN7453N	2-19
MC452F	SNG63R	SN7430S	2-15
MC452P	SNG63J,N	SN7430N	2-15
MC458F	SNG143R	SN7400S	2-5
MC458P	SNG143J,N	SN7400N	2-5
MC461F	SNG183R	SN7460S	2-21
MC461P	SNG183J,N	SN7460N	2-21
MC462F	SNG193R	SN7410S	2-13
MC462P	SNG193J,N	SN7410N	2-13
MC465F	SNF53R	SN7470S	2-23
MC465P	SNF53J,N	SN7470N	2-23
MC470F	SNG73R	SN7450S	2-17
MC470P	SNG73J,N	SN7450N	2-17
MC500F	SNG40R	SN5420S	2-14
MC501F	SNG50R	SN5453S	2-19
MC502F	SNG60R	SN5430S	2-19
MC508F	SNG140R	SN5400S	2-5
MC511F	SNG180R	SN5460S	2-21
MC512F	SNG190R	SN5410S	2-13
MC515F	SNF50R	SN5470S	2-23
MC520F	SNG70R	SN5450S	2-17
MC550F	SNG41R	SN5420S	2-14
MC551F	SNG51R	SN5453S	2-19
MC552F	SNG61R	SN5430S	2-15
MC558F	SNG141R	SN5400S	2-5
MC561F	SNG181R	SN5460S	2-21
MC562F	SNG191R	SN5410S	2-13
MC565F	SNF51R	SN5470S	2-23
MC570F	SNG71R	SN5450S	2-17
MC2000F	SNG212R	SN74H55S	3-24
MC2000P	SNG212J,N	SN74H55N	3-24
MC2001F	SNG222R	SN74H00S	3-5
MC2001P	SNG222J, N	SN74H00N	3-5
MC2002P	SNG232J,N	SN74H62N	3-29
MC2003F	SNG242R	SN74H20S	3-13
MC2003P	SNG242J,N	SN74H20N	3-13
MC2004F	SNG252R	SN74H53S	3-22
MC2004P	SNG252J,N	SN74H53N	3-22
MC2005F	SNG262R	SN74H30S	3-16
MC2005P	SNG262J,N	SN74H30N	3-16
MC2006F	SNG272R	SN74H60S	3-27
MC2006P	SNG272J,N	SN74H60N	3-27
MC2007F	SNG282R	SN74H10S	3-11
MC2007P	SNG282J,N	SN74H10N	3-11
MC2010F	SNF262R	SN74H71S	3-31
MC2010P	SNF262J,N	SN74H71N	3-31
MC2013F	SNG312R	SN74H50S	3-18
MC2013P	SNG312J,N	SN74H50N	3-18
MC2050F	SNG213R	SN74H55S	3-24
MC2050P	SNG213J,N	SN74H55N	3-24
MC2051F	SNG223R	SN74H00S	3-5
MC2051P	SNG223J,N	SN74H00N	3-5
MC2052F	SNG233R	SN74H62S	3-30
MC2052P	SNG233J,N	SN74H62N	3-30
MC2053F	SNG243R	SN74H20S	3-13
MC2053P	SNG243J,N	SN74H50S	3-18
MC2054F	SNG253R	SN74H53S	3-22
MC2054P	SNG253J,N	SN74H53N	3-22
MC2055F	SNG263R	SN74H30S	3-16
MC2055P	SNG263J,N	SN74H30N	3-16
MC2056F	SNG273R	SN74H60S	3-26
MC2056P	SNG273J,N	SN74H60N	3-26
MC2057F	SNG283R	SN74H10S	3-11
MC2057P	SNG283J,N	SN74H10N	3-11
MC2060F	SNF263R	SN74H71S	3-31
MC2060P	SNF263J,N	SN74H71N	3-31
MC2063P	SNG313J,N	SN74H50N	3-18
MC2100F	SNG210R	SN54H55S	3-24
MC2101F	SNG220R	SN54H00S	3-5
MC2102F	SNG230R	SN54H62S	3-29
MC2103F	SNG240R	SN54H20S	3-13
MC2104F	SNG250R	SN54H53S	3-22
MC2105F	SNG260R	SN54H30S	3-16
MC2106F	SNG270R	SN54H60S	3-26
MC2107F	SNG280R	SN74H10S	3-11
MC2110F	SNF260R	SN54H71S	3-31
MC2110P		SN54H71N	3-31
MC2113F	SNG310R	SN54H50S	3-18
MC2150F	SNG211R	SN54H55S	3-24
MC2151F	SNG221R	SN54H00S	3-5
MC2152F	SNG231R	SN54H62S	3-29
MC2153F	SNG241R	SN54H20S	3-13
MC2154F	SNG251R	SN54H53S	3-22
MC2155F	SNG261R	SN54H30S	3-16
MC2156F	SNG271R	SN54H60S	3-26
MC2157F	SNG281R	SN74H10S	3-11
MC2160F	SNF261R	SN54H71S	3-31
MC2160P		SN54H71N	3-31
MC2163F	SNG311R	SN54H50S	3-18
MC2602F		SN74H62S	3-30
MC3000F		SN74H00S	3-5
MC3000P		SN74H00N	3-5
MC3004F		SN74H01S	3-6
MC3004P		SN74H01N	3-6
MC3005F		SN74H10S	3-11
MC3005P		SN74H10N	3-11
MC3006F		SN74H11S	3-12
MC3006P		SN74H11N	3-12
MC3010F		SN74H20S	3-13
MC3010P		SN74H20N	3-13
MC3011F		SN74H21S	3-14
MC3011P		SN74H21N	3-14
MC3012F		SN74H22S	3-15
MC3012P		SN74H22N	3-15
MC3015F		SN74H30S	3-16
MC3015P		SN74H30N	3-16
MC3020F		SN74H50S	3-18
MC3020P		SN74H50N	3-18
MC3025F		SN74H40S	3-17
MC3025P		SN74H40N	3-17
MC3030F		SN74H60S	3-27

†For a complete listing of SNF and SNG type numbers shown in this column, see Page C-1.

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Type Number	Nearest TI Replacement	Recommended for New Designs	Sec.– Page
MC3030P		SN74H60N	3-27
MC3050F		SN74H102S	3-49
MC3050P		SN74H102N	3-49
MC3061F		SN74H108S	3-58
MC3061P		SN74H108N	3-58
MC3062F		SN74H103S	3-52
MC3062P		SN74H103N	3-52
MC3100F		SN54H00S	3-5
MC3100P		SN54H00N	3-5
MC3104F		SN54H01S	3-6
MC3104P		SN54H01N	3-6
MC3105F		SN74H10S	3-11
MC3106F		SN54H11S	3-12
MC3106P		SN54H11N	3-12
MC3110F		SN54H20S	3-13
MC3110P		SN54H20N	3-13
MC3111F		SN54H21S	3-14
MC3111P		SN54H21N	3-14
MC3112F		SN54H22S	3-15
MC3112P		SN54H22N	3-15
MC3115F		SN54H30S	3-16
MC3115P		SN54H30N	3-16
MC3120F		SN54H50S	3-18
MC3120P		SN54H50N	3-18
MC3125F		SN54H40S	3-17
MC3125P		SN54H40N	3-17
MC3130		SN54H60S	3-26
MC3130P		SN54H60N	3-26
MC3150F		SN54H102S	3-49
MC3150P		SN54H102N	3-49
MC3150P		SN54H10N	3-11
MC3161P		SN54H108N	3-58
MC3162		SN54H103N	3-52
MC3162F		SN54H103S	3-52
MC5400F	SN5400F	SN5400S	2-5
MC5400P	SN5400N	SN5400N	2-5
MC5400L	SN5400J	SN5400J	2-5
MC5401F	SN5401F	SN5401S	2-6
MC5401L	SN5401J	SN5401J	2-6
MC5401P	SN5401N	SN5401N	2-6
MC5402F	SN5402F	SN5402S	2-9
MC5402L	SN5402J	SN5402J	2-9
MC5402P	SN5402N	SN5402N	2-9
MC5404F	SN5404S	SN5404S	2-11
MC5404L	SN5404J	SN5404J	2-11
MC5404P	SN5404N	SN5404N	2-11
MC5405F	SN5405S	SN5405S	2-12
MC5405L	SN5405J	SN5405J	2-12
MC5405P	SN5405N	SN5405N	2-12
MC5410F	SN5410S	SN5410S	2-13
MC5410L	SN5410J	SN5410J	2-13
MC5410P	SN5410N	SN5410N	2-13
MC5420F	SN5420S	SN5420S	2-14
MC5420L	SN5420J	SN5420J	2-14
MC5420P	SN5420N	SN5420N	2-14
MC5430F	SN5430S	SN5430S	2-15
MC5430L	SN5430J	SN5430J	2-15
MC5430P	SN5430N	SN5430N	2-15
MC5440F	SN5440S	SN5440S	2-16
MC5440F	SN5440N	SN5440N	2-16
MC5440L	SN5440J	SN5440J	2-16
MC5450F	SN5450S	SN5450S	2-17
MC5450L	SN5450J	SN5450J	2-17
MC5451F	SN5451S	SN5451S	2-17
MC5451P	SN5451N	SN5451N	2-17
MC5451L	SN5451J	SN5451J	2-17
MC5453F	SN5453S	SN5453S	2-19
MC5453L	SN5453J	SN5453J	2-19
MC5453P	SN5453N	SN5453N	2-19
MC5454F	SN5454S	SN5454S	2-19
MC5454L	SN5454J	SN5454J	2-19
MC5454P	SN5454N	SN5454N	2-19
MC5460F	SN5460S	SN5460S	2-21
MC5460P	SN5460N	SN5460N	2-21
MC5460L	SN5460J	SN5460J	2-21
MC5460P	SN5460N	SN5460N	2-21
MC5472F	SN5472S	SN5472S	2-26
MC5472L	SN5472J	SN5472J	2-26
MC5472P	SN5472N	SN5472N	2-26
MC5473F	SN5473S	SN5473S	2-29
MC5473L	SN5473J	SN5473J	2-29
MC5473P	SN5473N	SN5473N	2-29
MC5475L	SN5475J	SN5475J	6-1
MC5476L	SN5476J	SN5476J	2-35
MC5476P	SN5476N	SN5476N	2-35
MC5479F	SN5474S	SN5474S	2-32
MC5479L	SN5474J	SN5474J	2-32
MC5479P	SN5474N	SN5474N	2-32
MC5490L	SN5490J	SN5490J	8-1
MC5493L	SN5493J	SN5493J	8-13
MC7400F	SN7400S	SN7400S	2-5
MC7400L	SN7400J	SN7400J	2-5
MC7400P	SN7400N	SN7400N	2-5
MC7401F	SN7401S	SN7401S	2-6
MC7401L	SN7401J	SN7401J	2-6
MC7401P	SN7401N	SN7401N	2-6
MC7402F	SN7402S	SN7402S	2-9
MC7402L	SN7402J	SN7402J	2-9
MC7402P	SN7402N	SN7402N	2-9
MC7404F	SN7404S	SN7404S	2-11
MC7404L	SN7404J	SN7404J	2-11
MC7404P	SN7404N	SN7404N	2-11
MC7405F	SN7405S	SN7405S	2-12
MC7405L	SN7405J	SN7405J	2-12
MC7405P	SN7405N	SN7405N	2-12
MC7410F	SN7410S	SN7410S	2-13
MC7410L	SN7410J	SN7410J	2-13
MC7410P	SN7410N	SN7410N	2-13
MC7420F	SN7420S	SN7420S	2-14
MC7420L	SN7420J	SN7420J	2-14
MC7420P	SN7420N	SN7420N	2-14
MC7430F	SN7430S	SN7430S	2-15
MC7430L	SN7430J	SN7430J	2-15
MC7430P	SN7430N	SN7430N	2-15
MC7440F	SN7440S	SN7440S	2-16
MC7440L	SN7440J	SN7440J	2-16
MC7440P	SN7440N	SN7440N	2-16
MC7441AL	SN7441AJ	SN7441AJ	5-1
MC7450F	SN7450S	SN7450S	2-17
MC7450L	SN7450J	SN7450J	2-17
MC7450P	SN7450N	SN7450N	2-17
MC7451F	SN7451S	SN7451S	2-17
MC7451L	SN7451J	SN7451J	2-17
MC7451P	SN7451N	SN7451N	2-17
MC7453F	SN7453S	SN7453S	2-19
MC7453L	SN7453J	SN7453J	2-19
MC7453P	SN7453N	SN7453N	2-19
MC7454F	SN7454S	SN7454S	2-19
MC7454L	SN7454J	SN7454J	2-19
MC7454P	SN7454N	SN7454N	2-19

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MC7460F	SN7460S	SN7460S	2-22
MC7460P	SN7460N	SN7460N	2-22
MC7460L	SN7460J	SN7460J	2-22
MC7472F	SN7472S	SN7472S	2-26
MC7472L	SN7472J	SN7472J	2-26
MC7472P	SN7472N	SN7472N	2-26
MC7473F	SN7473S	SN7473S	2-29
MC7473L	SN7473J	SN7473J	2-29
MC7473P	SN7473N	SN7473N	2-29
MC7475L	SN7475J	SN7475J	6-1
MC7476L	SN7476J	SN7476J	2-35
MC7476P	SN7476N	SN7476N	2-35
MC7479F	SN7474S	SN7474S	2-32
MC7479L	SN7474J	SN7474J	2-32
MC7479P	SN7474N	SN7474N	2-32
MC7490L	SN7490J	SN7490J	8-1
MC7493L	SN7493J	SN7493J	8-13

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DM70L00F	SN54L00T	SN54L00T	4-4
DM70L10F	SN54L10T	SN54L10T	4-6
DM70L20F	SN54L20T	SN54L20T	4-7
DM70L30F	SN54L30T	SN54L30T	4-8
DM75L01F	SN54L73T	SN54L73T	4-18
DM75L78F	SN54L78T	SN54L78T	4-21
DM80L00F	SN74L00T	SN74L00T	4-4
DM80L10F	SN74L10T	SN74L10T	4-6
DM80L20F	SN74L20T	SN74L20T	4-7
DM80L30F	SN74L30T	SN74L30T	4-8
DM85L01F	SN74L73T	SN74L73T	4-18
DM85L78F	SN74L78T	SN74L78T	4-21
DM7000D	SN5400J	SN5400J	2-5
DM7001D	SN5401J	SN5401J	2-6
DM7003D	SN5403J	SN5403J	2-10
DM7010D	SN5410J	SN5410J	2-13
DM7020D	SN5420J	SN5420J	2-14
DM7030D	SN5430J	SN5430J	2-15
DM7040D	SN5440J	SN5440J	2-16
DM7050D	SN5450J	SN5450J	2-17
DM7051D	SN5451J	SN5451J	2-17
DM7053D	SN5453J	SN5453J	2-19
DM7054D	SN5454J	SN5454J	2-19
DM7060D	SN5460J	SN5460J	2-21
DM7086D	SN5486J	SN5486J	7-27
DM7220D		SN54180J	11-1
DM7500D	SN5476J	SN5476J	2-35
DM7501D	SN5473J	SN5473J	2-29
DM7510D	SN5474J	SN5474J	2-32
DM7530D	SN5490J	SN5490J	8-1
DM7532D	SN5492J	SN5492J	8-7
DM7533D	SN5493J	SN5493J	8-13
DM7550D	SN5475J	SN5475J	6-1
DM7842D	SN5442S	SN5442S	5-7
DM8000N	SN7400N	SN7400N	2-5
DM8000D	SN7400J	SN7400J	2-5
DM8001N	SN7401N	SN7401N	2-6
DM8001D	SN7401J	SN7401J	2-6
DM8003N	SN7403N	SN7403N	2-10
DM8003D	SN7403J	SN7403J	2-10
DM8010N	SN7410N	SN7410N	2-13
DM8010D	SN7410J	SN7410J	2-13
DM8020N	SN7420N	SN7420N	2-14
DM8020D	SN7420J	SN7420J	2-14
DM8030N	SN7430N	SN7430N	2-15
DM8030D	SN7430J	SN7430J	2-15
DM8040N	SN7440N	SN7440N	2-16
DM8040D	SN7440J	SN7440J	2-16
DM8050N	SN7450N	SN7450N	2-17
DM8050D	SN7450J	SN7450J	2-17
DM8051N	SN7451N	SN7451N	2-17
DM8051D	SN7451J	SN7451J	2-17
DM8053N	SN7453N	SN7453N	2-19
DM8053D	SN7453J	SN7453J	2-19
DM8054N	SN7454N	SN7454N	2-19
DM8054D	SN7454J	SN7454J	2-19
DM8060N	SN7460N	SN7460N	2-22
DM8060D	SN7460J	SN7460J	2-22
DM8086D	SN7486J	SN7486J	7-27
DM8220N		SN74180N	11-1
DM8220D		SN74180J	11-1
DM8500N	SN7476N	SN7476N	2-35
DM8500D	SN7476J	SN7476J	2-35
DM8501N	SN7473N	SN7473N	2-29
DM8501D	SN7473J	SN7473J	2-29
DM8510N	SN7474N	SN7474N	2-32
DM8510D	SN7474J	SN7474J	2-32
DM8530N	SN7490N	SN7490N	8-1
DM8530D	SN7490J	SN7490J	8-1
DM8532N	SN7492N	SN7492N	8-7
DM8532D	SN7492J	SN7492J	8-7
DM8533N	SN7493N	SN7493N	8-13
DM8533D	SN7493J	SN7493J	8-13
DM8550N	SN7475N	SN7475N	6-1
DM8550D	SN7475J	SN7475J	6-1
DM8840N	SN7441AN	SN7441AN	5-1
DM8840D	SN7441AJ	SN7441AJ	5-1
DM8842N	SN7442N	SN7442N	5-7
DM8842D	SN7442J	SN7442J	5-7
DM8550N	SN7475N	SN7475N	6-1
DM8220N	SN74180N	SN74180N	11-1

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Type Number	Nearest TI Replacement†	Recommended for New Designs	Sec.–Page
RF50D	SNF50J	SN5470J	2-23
RF50K	SNF50R	SN5470S	2-23
RF50P	SNF50N	SN5470N	2-23
RF51D	SNF51J	SN5470J	2-23
RF51K	SNF51R	SN5470S	2-23
RF51P	SNF51N	SN5470N	2-23
RF52D	SNF52J	SN7470J	2-23
RF52K	SNF52R	SN7470S	2-23
RF52P	SNF52N	SN7470N	2-23
RF53D	SNF53J	SN7470J	2-23
RF53K	SNF53R	SN7470S	2-23
RF53P	SNF53N	SN7470N	2-23
RF100D	SNF100J	SN54H73J	3-37
RF100K	SNF100R	SN54H73S	3-37
RF100P	SNF100N	SN54H73N	3-37
RF101D	SNF101J	SN54H73J	3-37
RF101K	SNF101B	SN54H73S	3-37
RF101P	SNF101N	SN54H73N	3-37
RF102D	SNF102J	SN74H73J	3-37
RF102K	SNF102R	SN74H73S	3-37
RF102P	SNF102N	SN74H73N	3-37
RF103D	SNF103J	SN74H73J	3-37
RF103K	SNF103R	SN74H73S	3-37
RF103P	SNF103N	SN74H73N	3-37
RF110D	SNF110J	SN54H78J	3-43
RF110K	SNF110R	SN54H78S	3-43
RF110P	SNF110N	SN54H78N	3-43
RF111D	SNF111J	SN54H78J	3-43
RF111K	SNF111R	SN54H78S	3-43
RF111P	SNF111N	SN54H78N	3-43
RF112D	SNF112J	SN74H78J	3-43
RF112K	SNF112R	SN74H78S	3-43
RF112P	SNF112N	SN74H78N	3-43
RF113D	SNF113J	SN74H78J	3-43
RF113K	SNF113R	SN74H78S	3-43
RF113P	SNF113N	SN74H78N	3-43
RF120D	SNF120J	SN54H103J	3-52
RF121K	SNF121R	SN54H103S	3-52
RF121P	SNF121N	SN54H103N	3-52
RF122D	SNF122J	SN74H103J	3-52
RF122K	SNF122R	SN74H103S	3-52
RF122P	SNF122N	SN74H103N	3-52
RF123K	SNF123R	SN74H103S	3-52
RF123P	SNF123N	SN74H103N	3-52
RF123D	SNF123J	SN74H103J	3-52
RF130D	SNF130J	SN54H108J	3-58
RF130K	SNF130R	SN54H108S	3-58
RF130P	SNF130N	SN54H108N	3-58
RF131D	SNF131J	SN54H108J	3-58
RF131K	SNF131R	SN54H108S	3-58
RF131P	SNF131N	SN54H108N	3-58
RF132D	SNF132J	SN74H108J	3-58
RF132K	SNG132R	SN74H108S	3-58
RF132P	SNF132N	SN74H108N	3-58
RF133D	SNF133J	SN74H108J	3-58
RF133K	SNF133R	SN74H108S	3-58
RF133P	SNF1333N	SN74H108N	3-58
RF200D	SNF200J	SN54H102J	3-49
RF200K	SNF200R	SN54H102S	3-49
RF200P	SNF200N	SN54H102N	3-49
RF201D	SNF201J	SN54H102J	3-49
RF201K	SNF201R	SN54H102S	3-49
RF201P	SNF201N	SN54H102N	3-49
RF202D	SNF202J	SN74H102J	3-49
RF202K	SNF202R	SN74H102S	3-49
RF202P	SNF202N	SN74H102N	3-49
RF203D	SNF203J	SN74H102J	3-49
RF203K	SNF203R	SN74H102S	3-49
RF203P	SNF203N	SN74H102N	3-49
RF220K		SN54H103S	3-52
RF220P		SN54H103N	3-52
RF260D	SNF260J	SN54H71J	3-31
RF260K	SNF260R	SN54H71S	3-31
RF260P	SNF260N	SN54H71N	3-31
RF261D	SNF261J	SN54H71J	3-31
RF261K	SNF261R	SN54H71S	3-31
RF261P	SNF261N	SN54H71N	3-31
RF262D	SNF262J	SN74H71J	3-31
RF262K	SNF262R	SN74H71S	3-31
RF262P	SNF262N	SN74H71N	3-31
RF263D	SNF263J	SN74H71J	3-31
RF263K	SNF263R	SN74H71S	3-31
RF263P	SNF263N	SN74H71N	3-31
RF3120D		SN54H103J	3-52
RF3120K		SN54H103S	3-52
RF3120P		SN54H103N	3-52
RF3122D		SN74H103J	3-52
RF3122K		SN74H103S	3-52
RF3122P		SN74H103N	3-52
RF3130K		SN54H108S	3-58
RF3130D		SN54H108J	3-58
RF3130P		SN54H108N	3-58
RF3132D		SN74H108J	3-58
RF3132K		SN74H108S	3-58
RF3132P		SN74H108N	3-58
RF3200D		SN54H102J	3-49
RF3200K		SN54H20S	3-13
RF3200P		SN54H102N	3-49
RF3202K		SN74H102S	3-49
RF3202D		SN74H102J	3-49
RF3202P		SN74H102N	3-49
RG40D	SNG40J	SN5420J	2-14
RG40P	SNG40N	SN5420N	2-14
RG41D	SNG41J	SN5420J	2-14
RG41K	SNG41R	SN5420S	2-14
RG41P	SNG41N	SN5420N	2-14
RG42D	SNG42J	SN7420J	2-14
RG42K	SNG42R	SN7420S	2-14
RG42P	SNG42N	SN7420N	2-14
RG43D	SNG43J	SN7420J	2-14
RG43K	SNG43R	SN7420S	2-14
RG43P	SNG43N	SN7420N	2-14
RG60K	SNG60R	SN5430S	2-15
RG60P	SNG60N	SN5430N	2-15
RG60D	SNG60J	SN5430J	2-15
RG61K	SNG61R	SN5430S	2-15
RG61D	SNG61J	SN5430J	2-15
RG61K	SNG61R	SN7430N	2-15
RG61P	SNG61N	SN5430N	2-15
RG62D	SNG62J	SN7430J	2-15
RG62K	SNG62R	SN7430S	2-15
RG62P	SNG62N	SN7430N	2-15
RG63D	SNG63J	SN7430J	2-15
RG63K	SNG63R	SN7430S	2-15
RG63P	SNG63N	SN7430N	2-15
RG90K	SNG90R	SN5420S	2-14
RG140D	SNG140J	SN5400J	2-5
RG140K	SNG140R	SN5400S	2-5
RG140P	SNG140N	SN5400N	2-5
RG141D	SNG141J	SN5400J	2-5

†For a complete listing of SNF and SNG type numbers shown in this column, see Page C-1.

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RG141K	SNG141R	SN5400S	2-5
RG141P	SNG141N	SN5400N	2-5
RG142D	SNG142J	SN7400J	2-5
RG142K	SNG142R	SN7400S	2-5
RG142P	SNG142N	SN7400N	2-5
RG143D	SNG143J	SN7400J	2-5
RG143K	SNG143R	SN7400S	2-5
RG143P	SNG143N	SN7400N	2-5
RG180D	SNG180J	SN5460J	2-21
RG180K	SNG180R	SN5460S	2-21
RG180P	SNG180N	SN5460N	2-21
RG181D	SNG181J	SN5460J	2-21
RG181K	SNG181R	SN5460S	2-21
RG181P	SNG181N	SN5460N	2-21
RG182D	SNG182J	SN7460J	2-22
RG182K	SNG182R	SN7460S	2-22
RG182P	SNG182N	SN7460N	2-22
RG183D	SNG183J	SN7460J	2-22
RG183K	SNG183R	SN7460S	2-22
RG183P	SNG183N	SN7460N	2-22
RG190D	SNG190J	SN5410J	2-13
RG190K	SNG190R	SN5410S	2-13
RG190P	SNG190N	SN5410N	2-13
RG191D	SNG191J	SN5410J	2-13
RG191K	SNG191R	SN5410S	2-13
RG191P	SNG191N	SN5410N	2-13
RG192D	SNG192J	SN7410J	2-13
RG192K	SNG192R	SN7410S	2-13
RG192P	SNG192N	SN7410N	2-13
RG193D	SNG193J	SN7410J	2-13
RG193K	SNG193R	SN7410S	2-13
RG193P	SNG193N	SN7410N	2-13
RG210D	SNG210J	SN54H55J	3-24
RG210K	SNG210R	SN54H55S	3-24
RG210P	SNG210N	SN54H55N	3-24
RG211D	SNG211J	SN54H55J	3-24
RG211K	SNG211R	SN54H55S	3-24
RG211P	SNG211N	SN54H55N	3-24
RG212D	SNG212J	SN74H55J	3-24
RG212K	SNG212R	SN74H55S	3-24
RG212P	SNG212N	SN74H55N	3-24
RG213D	SNG213J	SN74H55J	3-24
RG213K	SNG213R	SN74H55S	3-24
RG213P	SNG213N	SN74H55N	3-24
RG220D	SNG220J	SN54H00J	3-5
RG220K	SNG220R	SN54H00S	3-5
RG220P	SNG220N	SN54H00N	3-5
RG221K	SNG221R	SN54H00S	3-5
RG221P	SNG221N	SN54H00N	3-5
RG222D	SNG222J	SN74H00J	3-5
RG222K	SNG222R	SN74H00S	3-5
RG222P	SNG222N	SN74H00N	3-5
RG223D	SNG223J	SN74H00J	3-5
RG223K	SNG223R	SN74H00S	3-5
RG223P	SNG223N	SN74H00N	3-5
RG230D	SNG230J	SN54H62J	3-29
RG230K	SNG230R	SN54H62S	3-29
RG230P	SNG230N	SN54H62N	3-29
RG231D	SNG231J	SN54H62J	3-29
RG231K	SNG231R	SN54H62S	3-29
RG231P	SNG231N	SN54H62N	3-29
RG232D	SNG232J	SN74H62J	3-30
RG232K	SNG232R	SN74H62S	3-30
RG232P	SNG232N	SN74H62N	3-30
RG233D	SNG233J	SN74H62J	3-30
RG233K	SNG233R	SN74H62S	3-30
RG233P	SNG233N	SN74H62N	3-30
RG240D	SNG240J	SN54H20J	3-13
RG240K	SNG240R	SN54H20S	3-13
RG240P	SNG240N	SN54H20N	3-13
RG241D	SNG241J	SN54H20J	3-13
RG241K	SNG241R	SN54H20S	3-13
RG241P	SNG241N	SN54H20N	3-13
RG242D	SNG242J	SN74H20J	3-13
RG242K	SNG242R	SN74H20S	3-13
RG242P	SNG242N	SN74H20N	3-13
RG243D	SNG243J	SN74H20J	3-13
RG243K	SNG243R	SN74H20S	3-13
RG243P	SNG243N	SN74H20N	3-13
RG250D	SNG250J	SN54H53J	3-22
RG250K	SNG250R	SN54H53S	3-22
RG250P	SNG250N	SN54H53N	3-22
RG251D	SNG251J	SN54H53J	3-22
RG251K	SNG251R	SN54H53S	3-22
RG251P	SNG251N	SN54H53N	3-22
RG252D	SNG252J	SN74H53J	3-22
RG252K	SNG252R	SN74H53S	3-22
RG252P	SNG252N	SN74H53N	3-22
RG253D	SNG253J	SN74H53J	3-22
RG253K	SNG253R	SN74H53S	3-22
RG253P	SNG253N	SN74H53N	3-22
RG260D	SNG260J	SN54H30J	3-16
RG260K	SNG260R	SN54H30S	3-16
RG260P	SNG260N	SN54H30N	3-16
RG261D	SNG261J	SN54H30J	3-16
RG261K	SNG261R	SN54H30S	3-16
RG261P	SNG261N	SN54H30N	3-16
RG262D	SNG262J	SN74H30J	3-16
RG262K	SNG262R	SN74H30S	3-16
RG262P	SNG262N	SN74H30N	3-16
RG263D	SNG263J	SN74H30J	3-16
RG263K	SNG263R	SN74H30S	3-16
RG263P	SNG263N	SN74H30N	3-16
RG310D	SNG310J	SN54H50J	3-18
RG310K	SNG310R	SN54H50S	3-18
RG310P	SNG310N	SN54H50N	3-18
RG311D	SNG311J	SN54H50J	3-18
RG311K	SNG311R	SN54H50S	3-18
RG311P	SNG311N	SN54H50N	3-18
RG312D	SNG312J	SN54H50J	3-18
RG312K	SNG312R	SN74H50S	3-18
RG312P	SNG312N	SN74H50N	3-18
RG313D	SNG313J	SN74H50J	3-18
RG313K	SNG313R	SN74H50S	3-18
RG313P	SNG313N	SN74H50N	3-18
RG320D		SN54H10J	3-11
RG320K		SN54H10S	3-11
RG320P		SN54H10N	3-11
RG321D		SN54H10J	3-11
RG321K		SN54H10S	3-11
RG321P		SN54H10N	3-11
RG322D		SN74H10J	3-11
RG322K		SN74H10S	3-11
RG322P		SN74H10N	3-11
RG323D		SN74H10J	3-11
RG323K		SN74H10S	3-11
RG323P		SN74H10N	3-11
RG370D		SN5404J	2-11
RG370K		SN5404S	2-11
RG370P		SN5404N	2-11

†For a complete listing of SNF and SNG type numbers shown in this column, see Page C-1.

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Type Number	Nearest TI Replacement	Recommended for New Designs	Sec.–Page
RG371D		SN5404J	2-11
RG371K		SN5404S	2-11
RG371P		SN5404N	2-11
RG372P		SN7404J	2-11
RG372K		SN7404S	2-11
RG372P		SN7404N	2-11
RG373D		SN7404J	2-11
RG373K		SN7404S	2-11
RG373P		SN7404N	2-11
RG380D		SN54H04J	3-9
RG380K		SN54H04S	3-9
RG380P		SN54H04N	3-9
RG381D		SN54H04J	3-9
RG381K		SN54H04S	3-9
RG381P		SN54H04N	3-9
RG382D		SN74H04J	3-9
RG382K		SN74H04S	3-9
RG382P		SN74H04N	3-9
RG383D		SN74H04J	3-9
RG383K		SN74H04S	3-9
RG383P		SN74H04N	3-9
RG3180D		SN54H60J	3-26
RG3180K		SN54H60S	3-26
RG3180P		SN54H60N	3-26
RG3182D		SN74H60J	3-27
RG3182K		SN74H60S	3-27
RG3182P		SN74H60N	3-27
RG3210D		SN54H55J	3-24
RG3210K		SN54H55S	3-24
RG3210P		SN54H55N	3-24
RG3212D		SN74H55J	3-24
RG3212K		SN74H55S	3-24
RG3212P		SN74H55N	3-24
RG3220D		SN54H00J	3-5
RG3220K		SN54H00S	3-5
RG3220P		SN54H00N	3-5
RG3222D		SN74H00J	3-5
RG3222K		SN74H00S	3-5
RG3222P		SN74H00N	3-5
RG3230D		SN54H62J	3-29
RG3230K		SN54H62S	3-29
RG3230P		SN54H62N	3-29
RG3232D		SN74H62J	3-30
RG3232K		SN74H62S	3-30
RG3232P		SN74H62N	3-30
RG3240D		SN54H20J	3-13
RG3240K		SN54H20S	3-13
RG3240P		SN54H20N	3-13
RG3242D		SN74H20J	3-13
RG3242K		SN74H20S	3-13
RG3242P		SN74H20N	3-13
RG3250D		SN54H53J	3-22
RG3250K		SN54H53S	3-22
RG3250P		SN54H53N	3-22
RG3252D		SN74H53J	3-22
RG3252K		SN74H53S	3-22
RG3252P		SN74H53N	3-22
RG3260D		SN54H30J	3-16
RG3260K		SN54H30S	3-16
RG3260P		SN54H30N	3-16
RG3262D		SN74H30J	3-16
RG3262K		SN74H30S	3-16
RG3262P		SN74H30N	3-16
RG3310D		SN54H50J	3-18
RG3310K		SN54H50S	3-18
RG3310P		SN54H50N	3-18
RG3312D		SN74H50J	3-18
RG3312K		SN74H50S	3-18
RG3312P		SN74H50N	3-18
RG3320D		SN54H10J	3-11
RG3320K		SN54H10S	3-11
RG3320P		SN54H10N	3-11
RG3322D		SN74H10J	3-11
RG3322K		SN74H10S	3-11
RG3322P		SN74H10N	3-11
RG3380D		SN54H04J	3-9
RG3380K		SN54H04S	3-9
RG3380P		SN54H04N	3-9
RG3382D		SN74H04J	3-9
RG3382K		SN74H04S	3-9
RG3382P		SN74H04N	3-9
RG3440D		SN54H51J	3-18
RG3440K		SN54H51S	3-18
RG3440P		SN54H51N	3-18
RG3442D		SN74H51J	3-18
RG3442K		SN74H51S	3-18
RG3442P		SN74H51N	3-18
RL10D		SN5480J	7-1
RL10K		SN5480S	7-1
RL10P		SN5480N	7-1
RL11D		SN5480J	7-1
RL11K		SN5480S	7-1
RL11P		SN5480N	7-1
RL12D		SN7480J	7-1
RL12K		SN7480S	7-1
RL12P		SN7480N	7-1
RL13D		SN7480J	7-1
RL13K		SN7480S	7-1
RL13P		SN7480N	7-1

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Type Number	Nearest TI Replacement	Recommended for New Designs	Sec.–Page
LU300A		SN7460N	2-22
LU337A		SN7420N	2-14
LU356A		SN7440N	2-16
LU377A		SN7410N	2-13
LU380A		SN7402N	2-9
LU387A		SN7400N	2-5
N1283A		SN7484N	6-9
N7400A	SN7400N	SN7400N	2-5
N7400J	SN7400S	SN7400S	2-5
N7401A	SN7401N	SN7401N	2-6
N7401J	SN7401S	SN7401S	2-6
N7402A	SN7402N	SN7402N	2-9
N7402J	SN7402S	SN7402S	2-9
N7410A	SN7410N	SN7410N	2-13

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Type Number	Nearest TI Replacement	Recommended for New Designs	Sec.–Page
N7410J	SN7410S	SN7410S	2-13
N7420A	SN7420N	SN7420N	2-14
N7420J	SN7420S	SN7420S	2-14
N7430A	SN7430N	SN7430N	2-15
N7430J	SN7430S	SN7430S	2-15
N7440A	SN7440N	SN7440N	2-16
N7440J	SN7440S	SN7440S	2-16
N7441B	SN7441AN	SN7441AN	5-1
N7450A	SN7450N	SN7450N	2-17
N7450J	SN7450S	SN7450S	2-17
N7451A	SN7451N	SN7451N	2-17
N7451J	SN7451S	SN7451S	2-17
N7453A	SN7453N	SN7453N	2-19
N7453J	SN7453S	SN7453S	2-19
N7454A	SN7454N	SN7454N	2-19
N7454J	SN7454S	SN7454S	2-19
N7460A	SN7460N	SN7460N	2-22
N7460J	SN7460S	SN7460S	2-22
N7470A	SN7470N	SN7470N	2-23
N7470J	SN7470S	SN7470S	2-23
N7472A	SN7472N	SN7472N	2-26
N7472J	SN7472S	SN7472S	2-26
N7473A	SN7473N	SN7473N	2-29
N7473J	SN7473S	SN7473S	2-29
N7474A	SN7474N	SN7474N	2-32
N7474J	SN7474S	SN7474S	2-32
N7475B	SN7475N	SN7475N	6-1
N7476B	SN7475N	SN7476N	2-35
N7477J	SN7477S	SN7477S	6-1
N7477J	SN7477S	SN7477S	6-1
N7491A	SN7491AN	SN7491AN	9-1
N7491J	SN7491AS	SN7491AS	9-1
N8162J		SN74121S	2-38
N8162A		SN74121N	2-38
N8230A		SN74151N	10-1
N8230J		SN74152S	10-1
N8241A		SN7486N	7-27
N8241J		SN7486S	7-27
N8251A		SN7442N	5-7
N8268A		SN7480N	7-1
N8268J		SN7480S	7-1
N8270A		SN7495N	9-25
N8270J		SN7495S	9-25
N8271A		SN7495N	9-25
N8275B		SN7475N	6-1
N8276A		SN7491AN	9-1
N8276J		SN7491AS	9-1
N8280A		SN7490N	8-1
N8280J		SN7490S	8-1
N8281A		SN7493N	8-13
N8281J		SN7493S	8-13
N8490A		SN7404N	2-11
N8490J		SN7404S	2-11
N8806A	SN7460N	SN7460N	2-22
N8806J	SN7460S	SN7460S	2-22
N8808A	SN7430N	SN7430N	2-15
N8808J	SN7430S	SN7430S	2-15
N8816A	SN7420N	SN7420N	2-14
N8816J	SN7420S	SN7420S	2-14
N8822A		SN7473N	2-29
N8822J	SN7473S	SN7473S	2-29
N8828A	SN7474N	SN7474N	2-32
N8828J	SN7474S	SN7474S	2-32
N8829A	SN7470N	SN7470N	2-23
N8829J	SN7470S	SN7470S	2-23
N8840A	SN7450N	SN7450N	2-17
N8840J	SN7450S	SN7450S	2-17
N8848A	SN7453N	SN7453N	2-19
N8848J	SN7453S	SN7453S	2-19
N8855A		SN7440N	2-16
N8855J		SN7440S	2-16
N8870A		SN7410N	2-13
N8870J	SN7410S	SN7410S	2-13
N8880A		SN7400N	2-5
N8880J	SN7400S	SN7400S	2-5
N8881A		SN7401N	2-6
N8881J		SN7401S	2-6
N8885A		SN7402N	2-9
N8885J		SN7402S	2-9
N8H16A	SN74H20N	SN74H20N	3-13
N8H16J		SN74H20S	3-13
N8H21A		SN74H108S	3-58
N8H21J		SN54H108J	3-58
N8H70A	SN74H10N	SN74H10N	3-11
N8H70J		SN74H10S	3-11
N8H80A	SN74H00N	SN74H00N	3-5
N8H80J		SN74H00S	3-5
N8H90A		SN74H04N	3-9
N8H90J	SN74H04S	SN74H04S	3-9
N8T01B		SN7441AN	5-1
S5400A	SN5400N	SN5400N	2-5
S5400J	SN5400S	SN5400S	2-5
S5401A	SN5401N	SN5401N	2-6
S5401J	SN5401S	SN5401S	2-6
S5402A	SN5402N	SN5402N	2-9
S5402J	SN5402S	SN5402S	2-9
S5410A	SN5410N	SN5410N	2-13
S5410J	SN5410S	SN5410S	2-13
S5420A	SN5420N	SN5420N	2-14
S5420J	SN5420S	SN5420S	2-14
S5430A	SN5430N	SN5430N	2-15
S5430J	SN5430S	SN5430S	2-15
S5440A	SN5440N	SN5440N	2-16
S5440J	SN5440S	SN5440S	2-16
S5450A	SN5450N	SN5450N	2-17
S5450J	SN5450S	SN5450S	2-17
S5451A	SN5451N	SN5451N	2-17
S5451J	SN5451S	SN5451S	2-17
S5453A	SN5453N	SN5453N	2-19
S5453J	SN5453S	SN5453S	2-19
S5454A	SN5454N	SN5454N	2-19
S5454J	SN5454S	SN5454S	2-19
S5460A	SN5460N	SN5460N	2-21
S5460J	SN5460S	SN5460S	2-21
S5470A	SN5470N	SN5470N	2-23
S5470J	SN5470S	SN5470S	2-23
S5472A	SN5472N	SN5472N	2-26
S5472J	SN5472S	SN5472S	2-26
S5473A	SN5473N	SN5473N	2-29
S5473J	SN5473S	SN5473S	2-29
S5474A	SN5474N	SN5474N	2-32
S5474J	SN5474S	SN5474S	2-32
S5475B	SN5475N	SN5475N	6-1
S5476B		SN5476N	2-35
S5491A	SN5491AN	SN5491AN	9-1
S5491J	SN5491AS	SN5491AS	9-1
S8162A		SN54121N	2-38
S8162J		SN54121S	2-38
S8230A		SN54151N	10-1
S8230J		SN54152S	10-1

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Type Number	Nearest TI Replacement	Recommended for New Designs	Sec.– Page
S8241A		SN5486N	7-27
S8241J		SN5486S	7-27
S8251A		SN5442N	5-7
S8268A		SN5480N	7-1
S8268J		SN5480S	7-1
S8270A		SN5495N	9-25
S8270J		SN5495S	9-25
S8271A		SN5495N	9-25
S8275B		SN5475N	6-1
S8275J		SN5477S	6-1
S8276A		SN5491AN	9-1
S8276J		SN5491A	9-1
S8280J		SN5490N	8-1
S8280J		SN5490S	8-1
S8281A		SN5493N	8-13
S8281J		SN5493S	8-13
S8490A		SN5404N	2-11
S8490J		SN5404S	2-11
S8806A	SN5460N	SN5460N	2-21
S8806J	SN5460S	SN5460S	2-21
S8808A	SN5430N	SN5430N	2-15
S8808J	SN5430S	SN5430S	2-15
S8816A		SN5420N	2-14
S8816J	SN5420S	SN5420S	2-14
S8822A		SN5473N	2-29
S8822J	SN5473S	SN5473S	2-29
S8828A	SN5474N	SN5474N	2-32
S8828J	SN5474S	SN5474S	2-32
S8829A	SN5470N	SN5470N	2-23
S8829J	SN5470S	SN5470S	2-23
S8840A	SN5450N	SN5450N	2-17
S8840J	SN5450S	SN5450S	2-17
S8848A	SN5453N	SN5453N	2-19
S8848J	SN5453S	SN5453S	2-19
S8855A		SN5440N	2-16
S8855J		SN5440S	2-16
S8870A		SN5410N	2-13
S8870J	SN5410S	SN5410S	2-13
S8880A	SN5400N	SN5400N	2-5
S8880J	SN5400S	SN5400S	2-5
S8881A		SN5401N	2-6
S8881J		SN5401S	2-6
S8885A		SN5402N	2-9
S8885J		SN5402S	2-9
S8H16A	SN54H20N	SN54H20N	3-13
S8H16J		SN54H20S	3-13
S8H20A		SN54H103N	3-52
S8H20J		SN54H103S	3-52
S8H21A		SN54H108N	3-58
S8H21J		SN54H108S	3-58
S8H22B		SN54H106J	3-55
S8H22B		SN74H106J	3-55
S8H70A	SN54H10N	SN54H10N	3-11
S8H70J		SN54H10S	3-11
S8H80A	SN54H00N	SN54H00N	3-5
S8H80J		SN54H00S	3-5
S8H90A	SN54H04N	SN54H04N	3-9

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Type Number	Nearest TI Replacement	Recommended for New Designs	Sec.– Page
NE8162A		SN74121N	2-38
NE8162J		SN74121S	2-38
NE8251A		SN7442N	5-7
NE8806A	SN7460N	SN7460N	2-22
NE8806J	SN7460F	SN7460S	2-22
NE8808A	SN7430N	SN7430N	2-15
NE8808J	SN7430F	SN7430S	2-15
NE8816A		SN7420N	2-14
NE8816J		SN7420S	2-14
NE8822A		SN7473N	2-29
NE8822J	SN7473F	SN7473S	2-29
NE8828A	SN7474N	SN7474N	2-32
NE8828J	SN7474F	SN7474S	2-32
NE8829A	SN7470N	SN7470N	2-23
NE8829J	SN7470F	SN7470S	2-23
NE8840A	SN7450N	SN7450N	2-17
NE8840J	SN7450F	SN7450S	2-17
NE8848A	SN7453N	SN7453N	2-19
NE8855A		SN7440N	2-16
NE8855J		SN7440S	2-16
NE8870A		SN7410N	2-13
NE8870J	SN7410F	SN7410S	2-13
NE8880A		SN7400N	2-5
NE8880J	SN7400F	SN7400S	2-5
NE8881A		SN7401N	2-6
NE8881J		SN7401S	2-6
NE8885A		SN7402N	2-9
NE8885J		SN7402S	2-9
SE8162A		SN54121N	2-38
SE8162J		SN54121S	2-38
SE8251A		SN5442N	5-7
SE8806A	SN5460N	SN5460N	2-21
SE8806J	SN5460S	SN5460S	2-21
SE8808A	SN5430N	SN5430N	2-15
SE8808J	SN5430S	SN5430S	2-15
SE8816A		SN5420N	2-14
SE8816J	SN5420S	SN5420S	2-14
SE8822A		SN5473N	2-29
SE8822J	SN5473S	SN5473S	2-29
SE8828A	SN5474N	SN5474N	2-32
SE8828J	SN5474S	SN5474S	2-32
SE8829A	SN5470N	SN5470N	2-23
SE8829J	SN5470S	SN5470S	2-23
SE8840A	SN5450N	SN5450N	2-17

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Type Number	Nearest TI Replacement	Recommended for New Designs	Sec.–Page
SE8840J	SN5450S	SN5450S	2-17
SE8848A	SN5453N	SN5453N	2-19
SE8848J	SN5453S	SN5453S	2-19
SE8855A		SN5440N	2-16
SE8855J		SN5440S	2-16
SE8870A		SN5410N	2-13
SE8870J		SN5410S	2-13
SE8880A		SN5400N	2-5
SE8880J		SN5400S	2-5
SE8881A		SN5401N	2-6
SE8881J		SN5401S	2-6
SE8885A		SN5402N	2-9
SE8885J		SN5402S	2-9
USN7400A	SN7400N	SN7400N	2-5
USN7400J	SN7400S	SN7400S	2-5
USN7401A	SN7401N	SN7401N	2-6
USN7402A	SN7402N	SN7402N	2-9
USN7402J	SN7402S	SN7402S	2-9
USN7404A	SN7404N	SN7404N	2-11
USN7404J	SN7404S	SN7404S	2-11
USN7405A	SN7405N	SN7405N	2-12
USN7405J	SN7405S	SN7405S	2-12
USN7410A	SN7410N	SN7410N	2-13
USN7410J	SN7410S	SN7410S	2-13
USN7420A	SN7420N	SN7420N	2-14
USN7420J	SN7420S	SN7420S	2-14
USN7430A	SN7430N	SN7430N	2-15
USN7430J	SN7430S	SN7430S	2-15
USN7440A	SN7440N	SN7440N	2-16
USN7440J	SN7440S	SN7440S	2-16
USN7441B	SN7441AN	SN7441AN	5-1
USN7450A	SN7450N	SN7450N	2-17
USN7450J	SN7450S	SN7450S	2-17
USN7451A	SN7451N	SN7451N	2-17
USN7451J	SN7451S	SN7451S	2-17
USN7453A	SN7453N	SN7453N	2-19
USN7453J	SN7453S	SN7453S	2-19
USN7454A	SN7454N	SN7454N	2-19
USN7454J	SN7454S	SN7454S	2-19
USN7460A	SN7460N	SN7460N	2-22
USN7460J	SN7460S	SN7460S	2-22
USN7470A	SN7470N	SN7470N	2-23
USN7470J	SN7470S	SN7470S	2-23
USN7472A	SN7472N	SN7472N	2-26
USN7472J	SN7472S	SN7472S	2-26
USN7473A	SN7473N	SN7473N	2-29
USN7473J	SN7473S	SN7473S	2-29
USN7474A	SN7474N	SN7474N	2-32
USN7474J	SN7474S	SN7474S	2-32
USN7475B	SN7475N	SN7475N	6-1
USN7476B	SN7476N	SN7476N	2-35
USN7480A	SN7480N	SN7480N	7-1
USN7480J	SN7480S	SN7480S	7-1
USN7482A	SN7482N	SN7482N	7-11
USN7482J	SN7482S	SN7482S	7-11
USN7483B	SN7483N	SN7483N	7-19
USN7490A	SN7490N	SN7490N	8-1
USN7490J	SN7490S	SN7490S	8-1
USN7491A	SN7491AN	SN7491AN	9-1
USN7491J	SN7491AS	SN7491AS	9-1
USN7492A	SN7492N	SN7492N	8-7
USN7492UJ	SN7492S	SN7492S	8-7
USN7493A	SN7493N	SN7493N	8-13
USN7493J	SN7493S	SN7493S	8-13
USN74H00A	SN74H00N	SN74H00N	3-5
USN74H00J	SN74H00S	SN74H00S	3-5
USN74H10A	SN74H10N	SN74H10N	3-11
USN74H10J	SN74H10S	SN74H10S	3-11
USN74H11A	SN74H11N	SN74H11N	3-12
USN74H11J	SN74H11S	SN74H11S	3-12
USN74H20A	SN74H20N	SN74H20N	3-13
USN74H20J	SN74H20S	SN74H20S	3-13
USN74H21A	SN74H21N	SN74H21N	3-14
USN74H21J	SN74H21S	SN74H21S	3-14
USN74H30A	SN74H30N	SN74H30N	3-16
USN74H30J	SN74H30S	SN74H30S	3-16
USN74H40A	SN74H40N	SN74H40N	3-17
USN74H40J	SN74H40S	SN74H40S	3-17
USN74H50A	SN74H50N	SN74H50N	3-18
USN74H50J	SN74H50S	SN74H50S	3-18
USN74H51A	SN74H51N	SN74H51N	3-18
USN74H51J	SN74H51S	SN74H51S	3-18
USN74H52A	SN74H52N	SN74H52N	3-20
USN74H52J	SN74H52S	SN74H52S	3-20
USN74H53A	SN74H53N	SN74H53N	3-22
USN74H53J	SN74H53S	SN74H53S	3-22
USN74H54A	SN74H54N	SN74H54N	3-22
USN74H54J	SN74H54S	SN74H54S	3-22
USN74H55A	SN74H55N	SN74H55N	3-24
USN74H55J	SN74H55S	SN74H55S	3-24
USN74H60A	SN74H60N	SN74H60N	3-27
USN74H60J	SN74H60S	SN74H60S	3-27
USN74H61A	SN74H61N	SN74H61N	3-28
USN74H61J	SN74H61S	SN74H61S	3-28
USN74H62A	SN74H62N	SN74H62N	3-30
USN74H62J	SN74H62S	SN74H62S	3-30
USN74H71A	SN74H71N	SN74H71N	3-31
USN74H71J	SN74H71S	SN74H71S	3-31
USN74H72A	SN74H72N	SN74H72N	3-34
USN74H72J	SN74H72S	SN74H72S	3-34
USN74107A	SN74107N	SN74107N	2-29
USS5400A	SN5400N	SN5400N	2-5
USS5400J	SN5400S	SN5400S	2-5
USS5401A	SN5401N	SN5401N	2-6
USS5401J	SN5401S	SN5401S	2-6
USS5402A	SN5402N	SN5402N	2-9
USS5402J	SN5402S	SN5402S	2-9
USS5404A	SN5404N	SN5404N	2-11
USS5404J	SN5404S	SN5404S	2-11
USS5405A	SN5405N	SN5405N	2-12
USS5405J	SN5405S	SN5405S	2-12
USS5410A	SN5410N	SN5410N	2-13
USS5410J	SN5410S	SN5410S	2-13
USS5420A	SN5420N	SN5420N	2-14
USS5420J	SN5420S	SN5420S	2-14
USS5430A	SN5430N	SN5430N	2-15
USS5430J	SN5430S	SN5430S	2-15
USS5440A	SN5440N	SN5440N	2-16
USS5440J	SN5440S	SN5440S	2-16
USS5450A	SN5450N	SN5450N	2-17
USS5450J	SN5450S	SN5450S	2-17
USS5451A	SN5451N	SN5451N	2-17
USS5451J	SN5451S	SN5451S	2-17
USS5453A	SN5453N	SN5453N	2-19
USS5453J	SN5453S	SN5453S	2-19
USS5454A	SN5454N	SN5454N	2-19
USS5454J	SN5454S	SN5454S	2-19
USS5460A	SN5460N	SN5460N	2-21
USS5460J	SN5460S	SN5460S	2-21
USS5470A	SN5470N	SN5470N	2-23

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USS5470J	SN5470S	SN5470S	2-23
USS5472A	SN5472N	SN5472N	2-26
USS5472J	SN5472S	SN5472S	2-26
USS5473A	SN5473N	SN5473N	2-29
USS5473J	SN5473S	SN5473S	2-29
USS5474A	SN5474N	SN5474N	2-32
USS5474J	SN5474S	SN5474S	2-32
USS5476B	SN5476N	SN5476N	2-35
USS54H00A	SN54H00N	SN54H00N	3-5
USS54H00J	SN54H00S	SN54H00S	3-5
USS54H10A	SN54H10N	SN54H10N	3-11
USS54H10J	SN54H10S	SN54H10S	3-11
USS54H11A	SN54H11N	SN54H11N	3-12
USS54H11J	SN54H11S	SN54H11S	3-12
USS54H20A	SN54H20N	SN54H20N	3-13
USS54H20J	SN54H20S	SN54H20S	3-13
USS54H21A	SN54H21N	SN54H21N	3-14
USS54H21J	SN54H21S	SN54H21S	3-14
USS54H30A	SN54H30N	SN54H30N	3-16
USS54H30J	SN54H30S	SN54H30S	3-16
USS54H40A	SN54H40N	SN54H40N	3-17
USS54H40J	SN54H40S	SN54H40S	3-17
USS54H50A	SN54H50N	SN54H50N	3-18
USS54H50J	SN54H50S	SN54H50S	3-18
USS54H51A	SN54H51N	SN54H51N	3-18
USS54H51J	SN54H51S	SN54H51S	3-18
USS54H52A	SN54H52N	SN54H52N	3-20
USS54H52J	SN54H52S	SN54H52S	3-20
USS54H53A	SN54H53N	SN54H53N	3-22
USS54H53J	SN54H53S	SN54H53S	3-22
USS54H54A	SN54H54N	SN54H54N	3-22
USS54H54J	SN54H54S	SN54H54S	3-22
USS54H55A	SN54H55N	SN54H55N	3-24
USS54H55J	SN54H55S	SN54H55S	3-24
USS54H60A	SN54H60N	SN54H60N	3-26
USS54H60J	SN54H60S	SN54H60S	3-26
USS54H61A	SN54H61N	SN54H61N	3-28
USS54H61J	SN54H61S	SN54H61S	3-28
USS54H62A	SN54H62N	SN54H62N	3-29
USS54H62J	SN54H62S	SN54H62S	3-29
USS54H71A	SN54H71N	SN54H71N	3-31
USS54H71J	SN54H71S	SN54H71S	3-31
USS54H72A	SN54H72N	SN54H72N	3-34
USS54H72J	SN54H72S	SN54H72S	3-34
USS54107A	SN54107N	SN54107N	2-29

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Type Number	Nearest TI Replacement†	Recommended for New Designs	Sec.– Page
SF50-02	SNF50R	SN5470S	2-23
SF50-03	SNF50J	SN5470J	2-23
SF50-P	SNF50N	SN5470N	2-23
SF51-02	SNF51R	SN5470S	2-23
SF51-03	SNF51J	SN5470J	2-23
SF51-P	SNF51N	SN5470N	2-23
SF52-02	SNF52R	SN7470S	2-23
SF52-03	SNF52J	SN7470J	2-23
SF52-P	SNF52N	SN7470N	2-23
SF53-02	SNF53R	SN7470S	2-23
SF53-03	SNF53J	SN7470J	2-23
SF53-P	SNF53N	SN7470N	2-23
SF80-02		SN5474S	2-32
SF80-03		SN5474J	2-32
SF80-P		SN5474N	2-32
SF81-02		SN5474S	2-32
SF81-03		SN5474J	2-32
SF81-P		SN5474N	2-32
SF82-02		SN7474S	2-32
SF82-03		SN7474J	2-32
SF82-P		SN7474N	2-32
SF83-02		SN7474S	2-32
SF83-03		SN7474J	2-32
SF83-P		SN7474N	2-32
SF100-02	SNF100R	SN5473S	2-29
SF100-03	SNF100J	SN5473J	2-29
SF100-P	SNF100N	SN5473N	2-29
SF101-02	SNF101R	SN5473S	2-29
SF101-03	SNF101J	SN5473J	2-29
SF101-P	SNF101N	SN5473N	2-29
SF102-02	SNF102R	SN7473S	2-29
SF102-P	SNF102N	SN7473N	2-29
SF103-02	SNF103R	SN7473S	2-29
SF103-P		SN7473N	2-29
SF120-02	SNF120R	SN54H103S	3-52
SF120-03	SNF120J	SN54H103J	3-52
SF120-P	SNF120N	SN54H103N	3-52
SF121-02	SNF121R	SN54H103S	3-52
SF121-03	SNF121J	SN54H103J	3-52
SF121-P	SNF120N	SN54H103N	3-52
SF122-02	SNF122R	SN74H103S	3-52
SF122-03	SNF122J	SN74H103J	3-52
SF122-P	SNF122N	SN74H103N	3-52
SF123-02	SNF123R	SN74H103S	3-52
SF123-03	SNF123J	SN74H103J	3-52
SF123-P	SNF123N	SN74H103N	3-52
SF130-02	SNF130R	SN54H108S	3-58
SF130-03	SNF130J	SN54H108J	3-58
SF130-P	SNF130N	SN54H108N	3-58
SF131-02	SNF131R	SN54H108S	3-58
SF131-03	SNF131J	SN54H108J	3-58
SF131-P	SNF131N	SN54H108N	3-58
SF132-02	SNF132R	SN74H108S	3-58
SF132-03	SNF132J	SN74H108J	3-58
SF132-P	SNF132N	SN74H108N	3-58
SF133-02	SNF133R	SN74H108S	3-58
SF133-03	SNF133J	SN74H108J	3-58
SF133-P	SNF133N	SN74H108N	3-58
SF200-02	SNF200R	SN54H102S	3-49
SF200-03	SNF200J	SN54H102J	3-49

†For a complete listing of SNF and SNG type numbers shown in this column, see Page C-1.

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Type Number	Nearest TI Replacement†	Recommended for New Designs	Sec.–Page
SF200-P	SNF200N	SN54H102N	3-49
SF201-02	SNF201R	SN74H102S	3-49
SF201-03	SNF201J	SN54H102J	3-49
SF201-P	SNF201N	SN54H102N	3-49
SF202-02	SNF202R	SN54H102S	3-49
SF202-03	SNF202J	SN74H102J	3-49
SF202-P	SNF202N	SN74H102N	3-49
SF203-02	SNF203R	SN74H102S	3-49
SF203-03	SNF203J	SN74H102J	3-49
SF203-P	SNF203N	SN74H102N	3-49
SF210-02	SNF210R	SN54H101S	3-46
SF210-03	SNF210J	SN54H101J	3-46
SF210-P	SNF210N	SN54H101N	3-46
SF211-02	SNF211R	SN54H101S	3-46
SF211-03	SNF211J	SN54H101J	3-46
SF211-P	SNF211N	SN54H101N	3-46
SF212-02	SNF212R	SN74H101S	3-46
SF212-P	SNF212N	SN74H101N	3-46
SF213-02	SNF213R	SN74H101S	3-46
SF213-03	SNF213J	SN74H101J	3-46
SF213-P	SNF213N	SN74H101N	3-46
SF222-03		SN74H101J	3-46
SG40-02	SNG40R	SN5420S	2-14
SG40-03	SNG40J	SN5420J	2-14
SG40-P	SNG40N	SN5420N	2-14
SG41-02	SNG41R	SN5420S	2-14
SG41-03	SNG41J	SN5420J	2-14
SG41-P	SNG41N	SN5420N	2-14
SG42-02	SNG42R	SN7420S	2-14
SG42-03	SNG42J	SN7420J	2-14
SG42-P	SNG42N	SN7420N	2-14
SG43-02	SNG43R	SN7420S	2-14
SG43-03	SNG43J	SN7420J	2-14
SG43-P	SNG43N	SN7420N	2-14
SG50-02	SNG50R	SN5453S	2-19
SG50-P	SNG50N	SN5453N	2-19
SG51-02	SNG51R	SN5453S	2-19
SG51-03	SNG51J	SN5453J	2-19
SG51-P	SNG51N	SN5453N	2-19
SG52-02	SNG52R	SN7453S	2-19
SG52-03	SNG52J	SN7453J	2-19
SG52-P	SNG52N	SN7453N	2-19
SG53-02	SNG53R	SN7453S	2-19
SG53-03	SNG53J	SN7453J	2-19
SG53-P	SNG53N	SN7453N	2-19
SG60-02	SNG60R	SN5430S	2-15
SG60-03	SNG60J	SN5430J	2-15
SG60-P	SNG60N	SN5430N	2-15
SG61-02	SNG61R	SN5430S	2-15
SG61-03	SNG61J	SN5430J	2-15
SG61-P	SNG61N	SN5430N	2-15
SG62-02	SNG62R	SN7430S	2-15
SG62-03	SNG62J	SN7430J	2-15
SG62-P	SNG62N	SN7430N	2-15
SG63-02	SNG63R	SN7430S	2-15
SG63-03	SNG63J	SN7430J	2-15
SG63-P	SNG63N	SN7430N	2-15
SG70-02	SNG70R	SN5450S	2-17
SG70-03	SNG70J	SN5450J	2-17
SG70-P	SNG70N	SN5450N	2-17
SG71-02	SNG71R	SN5450S	2-17
SG71-03	SNG71J	SN5450J	2-17
SG71-P	SNG71N	SN5450N	2-17
SG72-02	SNG72R	SN7450S	2-17
SG72-03	SNG72J	SN7450J	2-17
SG72-P	SNG72N	SN7450N	2-17
SG73-02	SNG73R	SN7450S	2-17
SG73-03	SNG73J	SN7450J	2-17
SG73-P	SNG73N	SN7450N	2-17
SG130-02	SNG130R	SN5440S	2-16
SG130-03	SNG130J	SN5440J	2-16
SG130-P	SNG130N	SN5440N	2-16
SG131-02	SNG131R	SN5440S	2-16
SG131-03	SNG131J	SN5440J	2-16
SG131-P	SNG131N	SN5440N	2-16
SG132-02	SNG132R	SN7440S	2-16
SG132-03	SNG132J	SN7440J	2-16
SG132-P	SNG132N	SN7440N	2-16
SG133-02	SNG133R	SN7440S	2-16
SG133-03	SNG133J	SN7440J	2-16
SG133-P	SNG133N	SN7440N	2-16
SG140-02	SNG140R	SN5400S	2-5
SG140-03	SNG140J	SN5400J	2-5
SG140-P	SNG140N	SN5400N	2-5
SG141-02	SNG141R	SN5400S	2-5
SG141-03	SNG141J	SN5400J	2-5
SG141-P	SNG141N	SN5400N	2-5
SG142-02	SNG142R	SN7400S	2-5
SG142-03	SNG142J	SN7400J	2-5
SG142-P	SNG142N	SN7400N	2-5
SG143-02	SNG143R	SN7400S	2-5
SG143-03	SNG143J	SN7400J	2-5
SG143-P	SNG143N	SN7400N	2-5
SG180-02	SNG180R	SN5460S	2-21
SG180-03	SNG180J	SN5460J	2-21
SG180-P	SNG180N	SN5460N	2-21
SG181-02	SNG181R	SN5460S	2-21
SG181-03	SNG181J	SN5460J	2-21
SG181-P	SNG181N	SN5460N	2-21
SG182-02	SNG182R	SN7460S	2-22
SG182-03	SNG182J	SN7460J	2-22
SG182-P	SNG182N	SN7460N	2-22
SG183-02	SNG183R	SN7460S	2-22
SG183-03	SNG183J	SN7460J	2-22
SG183-P	SNG183N	SN7460N	2-22
SG190-02	SNG190R	SN5410S	2-13
SG190-03	SNG190J	SN5410J	2-13
SG190-P	SNG190N	SN5410N	2-13
SG191-02	SNG191R	SN5410S	2-13
SG191-03	SNG191J	SN5410J	2-13
SG191-P	SNG191N	SN5410N	2-13
SG192-03	SNG192J	SN7410J	2-13
SG192-02	SNG192R	SN7410S	2-13
SG192-P	SNG192N	SN7410N	2-13
SG193-02	SNG193R	SN7410S	2-13
SG193-03	SNG193J	SN7410J	2-13
SG193-P	SNG193N	SN7410N	2-13
SG210-02	SNG210R	SN54H55S	3-24
SG210-03	SNG210J	SN54H55J	3-24
SG210-P	SNG210N	SN54H55N	3-24
SG211-02	SNG211R	SN54H55S	3-24
SG211-03	SNG211J	SN54H55J	3-24
SG211-P	SNG211N	SN54H55N	3-24
SG212-02	SNG212R	SN74H55S	3-24
SG212-03	SNG212J	SN74H55J	3-24
SG212-P	SNG212N	SN74H55N	3-24
SG213-02	SNG213R	SN74H55S	3-24
SG213-03	SNG213J	SN74H55J	3-24
SG213-P	SNG213N	SN74H55N	3-24
SG220-02	SNG220R	SN54H00S	3-5

†For a complete listing of SNF and SNG type numbers shown in this column, see Page C-1.

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Type Number	Nearest TI Replacement†	Recommended for New Designs	Sec.–Page
SG220-03	SNG220J	SN54H00J	3-5
SG220-P	SNG220N	SN54H00N	3-5
SG221-02	SNG221R	SN54H00S	3-5
SG221-03	SNG221J	SN54H00J	3-5
SG221-P	SNG221N	SN54H00N	3-5
SG222-02	SNG222R	SN74H00S	3-5
SG222-03	SNG222J	SN74H00J	3-5
SG222-P	SNG222N	SN74H00N	3-5
SG223-02	SNG223R	SN74H00S	3-5
SG223-03	SNG223J	SN74H00J	3-5
SG223-P	SNG223N	SN74H00N	3-5
SG240-02	SNG240R	SN54H20S	3-13
SG240-03	SNG240J	SN54H20J	3-13
SG240-P	SNG240N	SN54H20N	3-13
SG241-02	SNG241R	SN54H20S	3-13
SG241-03	SNG241J	SN54H20J	3-13
SG241-P	SNG241N	SN54H20N	3-13
SG242-02	SNG242R	SN74H20S	3-13
SG242-03	SNG242J	SN74H20J	3-13
SG242-P	SNG242N	SN74H20N	3-13
SG243-02	SNG243R	SN74H20S	3-13
SG243-03	SNG243J	SN74H20J	3-13
SG243-P	SNG243N	SN74H20N	3-13
SG250-02	SNG250R	SN54H53S	3-22
SG250-03	SNG250J	SN54H53J	3-22
SG250-P	SNG250N	SN54H53N	3-22
SG251-02	SNG251R	SN54H53S	3-22
SG251-03	SNG251J	SN54H53J	3-22
SG251-P	SNG251N	SN54H53N	3-22
SG252-02	SNG252R	SN74H53S	3-22
SG252-03	SNG252J	SN74H53J	3-22
SG252-P	SNG252N	SN74H53N	3-22
SG253-02	SNG253R	SN74H53S	3-22
SG253-03	SNG253J	SN74H53J	3-22
SG253-P	SNG253N	SN74H53N	3-22
SG260-02	SNG260R	SN54H30S	3-16
SG260-03	SNG260J	SN54H30J	3-16
SG260-P	SNG260N	SN54H30N	3-16
SG261-02	SNG261R	SN54H30S	3-16
SG261-03	SNG261J	SN54H30J	3-16
SG261-P	SNG261N	SN54H30N	3-16
SG262-02	SNG262R	SN74H30S	3-16
SG262-03	SNG262J	SN74H30J	3-16
SG262-P	SNG262N	SN74H30N	3-16
SG263-02	SNG263R	SN74H30S	3-16
SG263-03	SNG263J	SN74H30J	3-16
SG263-P	SNG263N	SN74H30N	3-16
SG270-02	SNG270R	SN54H60S	3-26
SG270-03	SNG270J	SN54H60J	3-26
SG270-P	SNG270N	SN54H60N	3-26
SG271-02	SNG271R	SN54H60S	3-26
SG271-03	SNG271J	SN54H60J	3-26
SG271-P	SNG271N	SN54H60N	3-26
SG272-02	SNG272R	SN74H60S	3-27
SG272-03	SNG272J	SN74H60J	3-27
SG272-P	SNG272N	SN74H60N	3-27
SG273-02	SNG273R	SN74H60S	3-27
SG273-03	SNG273J	SN74H60J	3-27
SG273-P	SNG273N	SN74H60N	3-27
SG310-02	SNG310R	SN54H50S	3-18
SG310-03	SNG310J	SN54H50J	3-18
SG310-P	SNG310N	SN54H50N	3-18
SG311-02	SNG311R	SN54H50S	3-18
SG311-03	SNG311J,N	SN54H50J	3-18
SG311-P	SNG311N	SN54H50N	3-18
SG312-02	SNG312R	SN74H50S	3-18
SG312-03	SNG312J	SN74H50J	3-18
SG312-P	SNG312N	SN74H50N	3-18
SG313-02	SNG313R	SN74H50S	3-18
SG313-03	SNG313J	SN74H50J	3-18
SG313-P	SNG313N	SN74H50N	3-18
SG320-02		SN74H10S	3-11
SG320-03		SN54H10J	3-11
SG320-P		SN54H10N	3-11
SG321-02		SN74H10S	3-11
SG321-03		SN54H10J	3-11
SG321-P		SN54H10N	3-11
SG322-02		SN74H10S	3-11
SG322-03		SN74H10J	3-11
SG322-P		SN74H10N	3-11
SG323-02		SN74H10S	3-11
SG323-03		SN74H10J	3-11
SG323-P		SN74H10N	3-11
SM10-02		SN5480S	7-1
SM10-03		SN5480J	7-1
SM10-P		SN5480N	7-1
SM11-02		SN5480S	7-1
SM11-03		SN5480J	7-1
SM11-P		SN5480N	7-1
SM12-02		SN7480S	7-1
SM12-03		SN7480J	7-1
SM12-P		SN7480N	7-1
SM13-02		SN7480S	7-1
SM13-03		SN7480J	7-1
SM13-P		SN7480N	7-1
SM60		SN5475	6-1
SM70		SN5475	6-1
SM80-02		SN5484S	6-9
SM80-03		SN5484J	6-9
SM80-P		SN5484N	6-9
SM81-02		SN5484S	6-9
SM81-03		SN5484J	6-9
SM81-P		SN5484N	6-9
SM82-02		SN7484S	6-9
SM82-03		SN7484J	6-9
SM82-P		SN7484N	6-9
SM83-02		SN7484S	6-9
SM83-03		SN7484J	6-9
SM83-P		SN7484N	6-9
SM90		SN7490	8-1
SM110-02		SN5495S	9-25
SM110-03		SN5495J	9-25
SM110-P		SN5495N	9-25
SM111-02		SN5495S	9-25
SM111-03		SN5495J	9-25
SM111-P		SN5495N	9-25
SM112-02		SN7495S	9-25
SM112-03		SN7495J	9-25
SM112-P		SN7495N	9-25
SM113-02		SN7495S	9-25
SM113-03		SN7495J	9-25
SM113-P		SN7495N	9-25
SM120-02		SN54180S	11-1
SM120-03		SN54180J	11-1

†For a complete listing of SNF and SNG type numbers shown in this column, see Page C-1.

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Type Number	Nearest TI Replacement	Recommended for New Designs	Sec.– Page
SM120-P		SN54180N	11-1
SM121-02		SN54180S	11-1
SM121-03		SN54280J	11-1
SM121-P		SN54180N	11-1
SM122-02		SN74180S	11-1
SM122-03		SN74180J	11-1
SM122-P		SN74180N	11-1
SM123-02		SN74180S	11-1
SM123-03		SN74180J	11-1
SM123-P		SN74180N	11-1
SM130		SN5486	7-27
SM200-P		SN5446N	5-19
SM200-P		SN5447N	5-19
SM200-03		SN5447J	5-19
SM200-P		SN5448N	5-19
SM200-03		SN5448J	5-19
SM200-02		SN5449S	5-19
SM201-P		SN5446N	5-19
SM201-P		SN5447N	5-19
SM201-03		SN5447J	5-19
SM201-P		SN5448N	5-19
SM201-02		SN5449S	5-19
SM201-03		SN5448J	5-19
SM202-P		SN7447N	5-19
SM202-03		SN7447J	5-19
SM202-P		SN7448N	5-19
SM202-03		SN7448J	5-19
SM202-02		SN7449S	5-19
SM203-03		SN5446J	5-19
SM203-P		SN7447N	5-19
SM203-03		SN7447J	5-19
SM203-P		SN7448N	5-19
SM203-03		SN7448J	5-19
SM203-02		SN7449S	5-19
SM210-02		SN5415IN	10-1
SM210-03		SN74151N	10-1
SM210-P		SN54151J	10-1
SM212-02		SN74151J	10-1
SM212-03		SN74152S	10-1
SM212-P		SN54152S	10-1

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Type Number	Nearest TI Replacement†	Recommended for New Designs	Sec.– Page
TA10E		SN5480N	7-1
TA10F		SN5480S	7-1
TA10P		SN5480J	7-1
TA11E		SN5480N	7-1
TA11F		SN5480S	7-1
TA12E		SN7480N	7-1
TA12F		SN7480S	7-1
TA12P		SN7480J	7-1
TA13E		SN7480N	7-1
TA13F		SN7480S	7-1
TA13P		SN7480J	7-1
TDD1100P		SN7441AJ	5-1
TDD1101E		SN7441AN	5-1
TF50E	SNF50N	SN5470N	2-23
TF50F	SNF50R	SN5470F	2-23
TF50P	SNF50J	SN5470J	2-23
TF51E	SNF51N	SN5470N	2-23
TF51F	SNF51R	SN5470F	2-23
TF51P	SNF51J	SN5470J	2-23
TF52E	SNF52N	SN7470N	2-23
TF52P	SNF52J	SN7470J	2-23
TF52F	SNF52R	SN7470S	2-23
TF53F	SNF53R	SN7470S	2-23
TF53E	SNF53N	SN7470N	2-23
TF53P	SNF53J	SN7470J	2-23
TF120E	SNF120N	SN54H103N	3-52
TF120F	SNF120R	SN54H103S	3-52
TF120P	SNF120J	SN54H103J	3-52
TF121E	SNF121N	SN54H103N	3-52
TF121P	SNF121J	SN54H103J	3-52
TF122E	SNF122N	SN74H103N	3-52
TF122F	SNF122R	SN74H103S	3-52
TF122P	SNF122J	SN74H103J	3-52
TF123F	SNF123R	SN74H103S	3-52
TF123E	SNF123N	SN74H103N	3-52
TF123P	SNF123J	SN74H103J	3-52
TF130E	SNF130N	SN54H108N	3-58
TF131E	SNF131N	SN54H108N	3-58
TF131P	SNF131J	SN54H108J	3-58
TF132F	SNF132R	SN74H108S	3-58
TF132E	SNF132N	SN74H108N	3-58
TF132P	SNF132J	SN74H108J	3-58
TF133F	SNF133R	SN74H108S	3-58
TF133E	SNF133N	SN74H108J	3-58
TF133P	SNF133J,N	SN54H102N	3-49
TF200E	SNF200N	SN54H102J	3-49
TF200P	SNF200J	SN54H20S	3-13
TF200F	SNF200R	SN54H20S	3-13
TF201F	SNF201R	SN54H102N	3-49
TF201E	SNF201N	SN54H102J	3-49
TF201P	SNF201J	SN74H102S	3-49
TF202F	SNF202R	SN74H102J	3-49
TF202P	SNF202J	SN74H102N	3-49
TF202E	SNF202N	SN74H102J	3-49
TF203P	SNF203J	SN74H102N	3-49
TF203E	SNF203N	SN74H102S	3-49
TF203F	SNF203R	SN54H102N	3-49
TF210E	SNF210N	SN54H101S	3-46
TF210F	SNF210R	SN54H101S	3-46
TF210P	SNF210J	SN54H101N	3-46
TF211F	SNF211R	SN54H101J	3-46
TF211E	SNF211N	SN74H101J	3-46
TF211P	SNF211J	SN74H101S	3-46
TF212P	SNF212J	SN74H101N	3-46
TF212F	SNF212R	SN74H101S	3-46
TF212E	SNF212N	SN74H101J	3-46
TF213F	SNF213R	SN74H101N	3-46
TF213P	SNF213J	SN54H101J	3-46
TF213E	SNF213N	SN54H108S	3-58
TF220P		SN54H108S	3-58
TF230F		SN7472N	2-26
TF231F		SN7473N	2-29

†For a complete listing of SNF and SNG type numbers shown in this column, see Page C-1.

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Type Number	Nearest TI Replacement†	Recommended for New Designs	Sec.—Page
TF7472E		SN7474N	2-32
TF7473E		SN5470S	2-23
TF7474E		SN5470J	2-23
TFF3211F		SN7470S	2-23
TFF3211F		SN5420N	2-14
TFF3212F		SN5420S	2-14
TG40E	SNG40N	SN5420N	2-14
TG40F	SNG40R	SN5420S	2-14
TG40P	SNG40J	SN5420J	2-14
TG41E	SNG41N	SN5420N	2-14
TG41F	SNG41R	SN5420S	2-14
TG41P	SNG41J	SN5420J	2-14
TG42E	SNG42N	SN7420N	2-14
TG42F	SNG42R	SN7420S	2-14
TG42P	SNG42J	SN7420J	2-14
TG43E	SNG43N	SN7420N	2-14
TG43F	SNG43R	SN7420S	2-14
TG43P	SNG43J	SN7420J	2-14
TG60E	SNG60N	SN5430N	2-15
TG60F	SNG60R	SN5430S	2-15
TG60P	SNG60J	SN5430J	2-15
TG61E	SNG61N	SN5430N	2-15
TG61F	SNG61R	SN5430S	2-15
TG61P	SNG61J	SN5430J	2-15
TG62E	SNG62N	SN7430S	2-15
TG62F	SNG62R	SN7430J	2-15
TG62P	SNG62J,N	SN7430S	2-15
TG63E	SNG63N	SN7430J	2-15
TG63F	SNG63R	SN5400N	2-5
TG63P	SNG63J,N	SN5400S	2-5
TG140E	SNG140N	SN5400J	2-5
TG140F	SNG140R	SN5400N	2-5
TG140P	SNG140J	SN5400S	2-5
TG141E	SNG141N	SN5400J	2-5
TG141F	SNG141R	SN7400N	2-5
TG141P	SNG141J	SN7400S	2-5
TG142E	SNG142N	SN7400J	2-5
TG142F	SNG142R	SN7400N	2-5
TG142P	SNG142J	SN7400S	2-5
TG143E	SNG143N	SN7400J	2-5
TG143F	SNG143R	SN5460N	2-21
TG143P	SNG143J	SN5460S	2-21
TG180E	SNG180N	SN5460J	2-21
TG180F	SNG180R	SN5460N	2-21
TG180P	SNG180J	SN5460S	2-21
TG181E	SNG181N	SN5460J	2-21
TG181F	SNG181R	SN7460N	2-22
TG181P	SNG181J	SN7460S	2-22
TG182E	SNG182N	SN7460J	2-22
TG182F	SNG182R	SN7460N	2-22
TG182P	SNG182J	SN7460S	2-22
TG183E	SNG183N	SN7460J	2-22
TG183F	SNG183R	SN5410N	2-13
TG183P	SNG183J	SN5410S	2-13
TG190E	SNG190N	SN5410J	2-13
TG190F	SNG190R	SN5410N	2-13
TG190P	SNG190J	SN5410F	2-13
TG191E	SNG191N	SN5410J	2-13
TG191F	SNG191R	SN7410N	2-13
TG191P	SNG191J	SN7410S	2-13
TG192E	SNG192N	SN7410J	2-13
TG192F	SNG192R	SN7410N	2-13
TG192P	SNG192J	SN7410S	2-13
TG193E	SNG193N	SN7410J	2-13
TG193F	SNG193R	SN54H00N	3-5
TG193P	SNG193J	SN54H00S	3-5
TG220E	SNG220N	SN54H00J	3-5
TG220F	SNG220R	SN54H00N	3-5
TG220P	SNG220J	SN54H00S	3-5
TG221E	SNG221N	SN54H00J	3-5
TG221F	SNG221R	SN74H00N	3-5
TG221P	SNG221J	SN74H00S	3-5
TG222E	SNG222N	SN74H00J	3-5
TG222F	SNG222R	SN74H00N	3-5
TG222P	SNG222J	SN74H00S	3-5
TG223E	SNG223N	SN74H00J	3-5
TG223F	SNG223R	SN54H20N	3-13
TG223P	SNG223J	SN54H20S	3-13
TG240E	SNG240N	SN54H20J	3-13
TG240F	SNG240R	SN54H20N	3-13
TG240P	SNG240J	SN54H20S	3-13
TG241E	SNG241N	SN54H20J	3-13
TG241F	SNG241R	SN74H20N	3-13
TG241P	SNG241J	SN74H20S	3-13
TG242E	SNG242N	SN74H20J	3-13
TG242F	SNG242R	SN74H20S	3-13
TG242P	SNG242J	SN74H20J	3-13
TG243E	SNG243N	SN74H20N	3-13
TG243F	SNG243R	SN74H20S	3-13
TG243P	SNG243J	SN74H20J	3-13
TG250E	SNG250N	SN54H53N	3-22
TG250F	SNG250R	SN54H53S	3-22
TG250P	SNG250J	SN54H53J	3-22
TG251E	SNG251N	SN54H53N	3-22
TG251F	SNG251R	SN54H53S	3-22
TG252E	SNG252N	SN74H53N	3-22
TG252F	SNG252R	SN74H53S	3-22
TG252P	SNG252J	SN74H53J	3-22
TG253E	SNG253N	SN74H53N	3-22
TG253F	SNG253R	SN74H53S	3-22
TG253P	SNG253J	SN74H53J	3-22
TG260E	SNG260N	SN54H30N	3-16
TG260F	SNG260R	SN54H30S	3-16
TG260P	SNG260J	SN54H30J	3-16
TG261E	SNG261N	SN54H30N	3-16
TG261F	SNG261R	SN54H30S	3-16
TG261P	SNG261J	SN54H30J	3-16
TG262E	SNG262N	SN74H30N	3-16
TG262F	SNG262R	SN74H30S	3-16
TG262P	SNG262J	SN74H30J	3-16
TG263E	SNG263N	SN74H30N	3-16
TG263F	SNG263R	SN74H30S	3-16
TG263P	SNG263J	SN74H30J	3-16
TG270E	SNG270N	SN54H60N	3-26
TG270F	SNG270R	SN54H60S	3-26
TG270P	SNG270J	SN54H60J	3-26
TG271F	SNG271R	SN54H60S	3-26
TG272E	SNG272N	SN74H60N	3-26
TG272F	SNG272R	SN74H60S	3-27
TG272P	SNG272J	SN74H60J	3-27
TG310E	SNG310N	SN54H50N	3-18
TG310F	SNG310R	SN54H50S	3-18
TG310P	SNG310J	SN54H50J	3-18
TG311E	SNG311N	SN54H50N	3-18
TG311F	SNG311R	SN54H50S	3-18
TG311P	SNG311J	SN54H50J	3-18
TG312E	SNG312N	SN74H50N	3-18
TG312F	SNG312R	SN74H50S	3-18
TG312P	SNG312J	SN74H50J	3-18

†For a complete listing of SNF and SNG type numbers shown in this column, see Page C-1.

Transitron, Cont.

Type Number	Nearest TI Replacement†	Recommended for New Designs	Sec.–Page
TG313E	SNG313N	SN74H50N	3-18
TG313F	SNG313R	SN74H50S	3-18
TG313P	SNG313J	SN74H50J	3-18
TG320E		SN54H10N	3-11
TG320F		SN54H10S	3-11
TG320P		SN54H10J	3-11
TG321E		SN54H10N	3-11
TG321F		SN54H10S	3-11
TG321P		SN54H10J	3-11
TG322K		SN74H10S	3-11
TG322F		SN74H10N	3-11
TG322P		SN74H10J	3-11
TG323F		SN74H10N	3-11
TG323P		SN74H10J	3-11
TG333K		SN74H10S	3-11
TG7400E	SN7400N	SN7400N	3-5
TG7401E	SN7401N	SN7401N	2-6
TG7402E	SN7402N	SN7402N	2-9
TG7403E	SN7403N	SN7403N	2-10
TG7404E	SN7404N	SN7404N	2-11
TG7410E	SN7410N	SN7410N	2-13
TG7420E	SN7420N	SN7420N	2-14
TG7440E	SN7440N	SN7440N	2-16
TG7450E	SN7450N	SN7450N	2-17
TG7451E	SN7451N	SN7451N	2-17
TG7453E	SN7453N	SN7453N	2-19
TG7454E	SN7454N	SN7454N	2-19
TG7460E	SN7460N	SN7460N	2-22
TM80F		SN5484S	6-9
TM80E		SN5484N	6-9
TM80P		SN5484J	6-9
TM82E		SN7484N	6-9
TM82F		SN7484S	6-9
TM82P		SN7484J	6-9
TNG3162F		SN7484S	6-9
TNG3162P		SN7484J	6-9

†For a complete listing of SNF and SNG type numbers shown in this column, see Page C-1.

TTL APPLICATION REPORTS INDEX

To help you design with TTL, Texas Instruments produces a series of Application Reports that provide important "how-to" information for design engineers. Topics of the reports range from basic logic design through descriptions of TTL circuits to case study of design problems. Also included are other TI integrated circuits used in 54/74 TTL systems.

Listed below are descriptions of TTL and system interface application reports most often requested by customers. You may obtain copies of these reports from TI sales offices, authorized TI distributors, or from Texas Instruments, Marketing and Information Services, MS 308, P.O. Box 5012, Dallas, Texas 75222. Please reference on all requests the number and title of each report.

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TTL REPORTS

CA-102: TTL Integrated Circuits: Counters and Registers. Our MSI (medium-scale integration) standard 54/74 TTL counters and shift registers can be used along with gates and flip-flops to build even more complex, specialized computation functions. This comprehensive report provides functional analyses for the design of complex counters, shift registers, and storage registers in this fashion. More than 50 examples are shown—such as a seven-bit parallel-to-serial converter using two SN7495 packages—and many more are suggested. 41 pages. March 1968.

CA-108: Noise in 54/74 TTL Systems. Noise is a smaller problem with standard 54/74 TTL than with most other logic types, but it is still a very important design consideration. This report describes various sources of extraneous voltages and currents and shows how to deal with them. 12 pages. November 1968.

CA-112: Logic Design with Series 54/74 Gates. Many relatively complex logic operations may be performed with simple interconnections of a few 54/74 TTL gates. This report suggests with numerous examples how these NAND and NOR gates can be used to best advantage in the implementation of Boolean logic. 13 pages. October 1968.

CA-128: TTL One-Shot: SN74121. The operation of this 54/74 TTL monostable multivibrator is briefly described in this report, and three applications are shown—a pulse-delay method, a precise clock pulse generator, and a digital frequency-to-voltage converter. 4 pages. June 1969.

CA-129: TTL Design Cases and Guidelines. Seven standard 54/74 TTL "design cases" are presented here, each consisting of a problem frequently encountered and its solution (reprinted

from EDN magazine's "Customer Engineering Clinic" of January through April, 1969). Also included are rule-of-thumb answers to 21 frequently-asked questions regarding practical use of standard 54/74 TTL (reprinted from *Electronic Products* magazine, December 1968). 12 pages. June 1969.

CA-132: TTL Data Selector/Multiplexers. The SN54/74150, -151, and -152 are used basically as data selectors or multiplexers, but they fit a wide variety of other similar applications. This report describes this family of devices and shows how to use them for functions ranging from simple data selection to character generation. A section is included using Karnaugh maps to explain Boolean logic applications. 14 pages. July 1969.

CA-134: 54/74 TTL in Systems. This report analyzes the basic 54/74 TTL gate. Based on this information, precautions and procedures are explained for dealing with various threats to proper system performance (mainly various kinds of noise). Of special interest is a neat graphical way to predict and adjust transmission-line behavior. 20 pages. August 1969.

SYSTEMS-INTERFACE-CIRCUIT APPLICATION REPORTS

CA-101: Operation and Use of Series 7520N Sense Amplifiers. These versatile monolithic integrated circuits translate bipolar differential-input signals from computer magnetic memories into TTL logic levels. This report describes the operation of the devices and how best to use them in 54/74 TTL systems with various memory arrangements. 28 pages. November, 1967.

CA-107: SN75324 Monolithic Memory Driver. The SN75324 is a monolithic integrated circuit containing four fast, high-current switches controlled by seven logic inputs that are compatible with 54/74 TTL and other standard digital circuitry. It is designed for addressing and driving lines in a magnetic memory of an electronic digital computer. This report describes the SN75324 and illustrates how to apply it. 5 pages. February, 1969.

CA-122: Monolithic Interfacing in Computers. Monolithic integrated circuits are reaching further into the area of computer systems interface circuitry—that is, line drivers and receivers, memory drivers, and sense amplifiers. This report is a general survey of monolithic interface circuits produced by Texas Instruments, which are designed for use in 54/74 TTL systems. 10 pages. March, 1969.

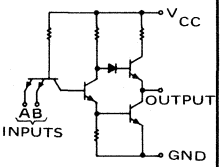
CA-130: Line Drivers and Receivers: SN55107 Series. This series of monolithic integrated circuits are designed to transmit data in 54/74 TTL systems rapidly over long lines subject to noise. Here, the operation and use of the circuits are described and many applications are outlined. 33 pages. July, 1969.

Should you desire assistance with a particular design problem not covered in these application reports, please contact the TI field sales office nearest you (listed on the back cover of this catalog) or our Applications/Design Department (MS 35, P.O. Box 5012, Dallas, Texas 75222, or telephone 214: 238-3319).

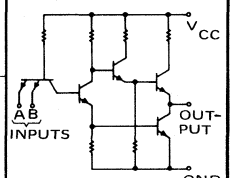
In addition to the TTL Application reports, TI offers many other reports dealing with both integrated circuit and semiconductor application—and new reports are produced on a continuing basis. To obtain a comprehensive listing of these application reports, request a copy of Bulletin CM-102, "Index to Applications Literature." Also described in this index is TI's "Microlibrary," a series of commercially available semiconductor design books used by industry and educational institutions.

SERIES SNG/SNF TTL DIGITAL

Functions	Package (See Section 1)	–55°C to 125°C J, N, and R	–55°C to 125°C J, N, and R	0°C to 75°C J, N, and R	0°C to 75°C J, N, and R
	Dual 4-Input NAND/NOR Gates	SNG40	SNG41	SNG42	SNG43
	Expandable Quadruple 2-Input OR Gates	SNG50	SNG51	SNG52	SNG53
	8-Input NAND/NOR Gates	SNG60	SNG61	SNG62	SNG63
	Expandable Dual Output, Dual 2-Input AND/NOR Gates	SNG70	SNG71	SNG72	SNG73
	Dual Pulse Shaper/Delay AND Gates	SNG80	SNG81	SNG82	SNG83
	Exclusive-OR Gates (With Complement)	SNG90	SNG91	SNG92	SNG93
	Expandable Triple 3-Input OR Gates	SNG100	SNG101	SNG102	SNG103
	Expandable Dual 4-Input OR Gates	SNG110	SNG111	SNG112	SNG113
	Expandable 8-Input NAND/NOR Gates	SNG120	SNG121	SNG122	SNG123
	High Fan-Out Dual 4-Input Drivers‡	SNG130[1]	SNG131[2]	SNG132[3]	SNG133[4]
	Quadruple 2-Input NAND/NOR Gates	SNG140	SNG141	SNG142	SNG143
	Quadruple 2-Input OR Expanders	SNG150	SNG151	SNG152	SNG153
	Triple 2-Input Bus Drivers	SNG160	SNG161	SNG162	SNG163
	Dual 4-Input OR Expanders	SNG170	SNG171	SNG172	SNG173
	Dual 4-Input AND Expanders	SNG180	SNG181	SNG182	SNG183
	Triple 3-Input NAND/NOR Gates	SNG190	SNG191	SNG192	SNG193
	Expandable 8-Input NAND/NOR Gates	SNG200	SNG201	SNG202	SNG203
	Expandable AND/NOR Gates	SNG210	SNG211	SNG212	SNG213
	Quadruple 2-Input NAND/NOR Gates	SNG220	SNG221	SNG222	SNG223
	Quadruple 2-Input AND/NOR Expanders	SNG230	SNG231	SNG232	SNG233
	Dual 4-Input NAND/NOR Gates	SNG240	SNG241	SNG242	SNG243
	Expandable AND/NOR Gates	SNG250	SNG251	SNG252	SNG253
	8-Input NAND/NOR Gates	SNG260	SNG261	SNG262	SNG263
	Dual 4-Input AND/NOR Expanders	SNG270	SNG271	SNG272	SNG273
	Expandable Dual 4-Input AND/OR Gates	SNG280	SNG281	SNG282	SNG283
	Dual 2-3-Input Expanders	SNG290	SNG291	SNG292	SNG293
	Expandable AND/NOR Gates (3-Wide, 3-Input)	SNG300	SNG301	SNG302	SNG303
	Expandable Dual AND/NOR Gates (2-Wide, 2-Input)	SNG310	SNG311	SNG312	SNG313
	Set-Reset Flip-Flops	SNF10	SNF11	SNF12	SNF13
	Set-Reset Clocked Flip-Flops	SNF20	SNF21	SNF22	SNF23
	Single-Phase S-R-T Flip-Flops	SNF30	SNF31	SNF32	SNF33
	AND Input J-K Flip-Flops	SNF50	SNF51	SNF52	SNF53
	OR Input J-K Flip-Flops	SNF60	SNF61	SNF62	SNF63
	Dual J-K Flip-Flops (Separate Clocks)	SNF100	SNF101	SNF102	SNF103
	Dual J-K Flip-Flops (Common Clock)	SNF110	SNF111	SNF112	SNF113
	Dual J-K Flip-Flops (Separate Clocks)	SNF120	SNF121	SNF122	SNF123
	Dual J-K Flip-Flops (Common Clock)	SNF130	SNF131	SNF132	SNF133
	AND Input J-K Flip-Flops	SNF200	SNF201	SNF202	SNF203
	OR Input J-K Flip-Flops	SNF210	SNF211	SNF212	SNF213
	AND Input J-K Flip-Flops	SNF250	SNF251	SNF252	SNF253
	OR Input J-K Flip-Flops	SNF260	SNF261	SNF262	SNF263



SNG140 NAND/NOR Gate



SNG220 NAND/NOR Gate

‡Recommended maximum fan-out is: [1]30; [2]15; [3]24; [4]12.

OTHER QUALITY TI INTEGRATED CIRCUITS (Cont.)

LINEAR INTEGRATED CIRCUITS

Differential/Operational Amplifiers

- Low input and output offset characteristics
- High common-mode input capability
- Most circuits are available in economical plastic dual-in-line package

Series 52 700/5510/5511 (Operating Temperature Range –55°C to 125°C)

		TYPICAL CHARACTERISTICS															
		Open-loop voltage gain A_{vs}	Bandwidth (—3 dB) BW	Input Impedance z_{in}	Input capacitance C_{in}	Differential-input offset voltage V_{IO}	Differential-input offset current I_{IO}	Differential-input offset voltage temperature coefficient α_{VIO}	Maximum common-mode input voltage range V_{CMIM}	Common-mode output offset voltage V_{CMO}	Output impedance z_{out}	Maximum peak-to-peak output voltage V_{OM}	Common-mode rejection ratio CMRR	Total power dissipation P_T	Input current I_{in}	Package (See Section 1)
		dB	kHz	kΩ	pF	mV	μA	μV/deg	V	V	Ω	V	dB	mW	μA	
SN52702	General-Purpose Op Amp	68	—	25	—	2	0.7	5	‡	—	200	10.6	80	70	4	F/L/N
SN52709	High-Performance Op Amp	93	—	400	—	3	0.05	—	±10	—	150	26	90	80	0.2	F/L/N
SN52710	Differential Comparator	64	—	—	—	2	1	5	—	—	200	—	—	110	25	F/L/N
SN52711	Dual Differential Comparator	64	—	—	—	1	0.5	5	—	—	200	—	—	130	25	F/L/N
SN5510	Wide-Band Video Amplifier	40	40,000	6	7	—	3	—	±1	3.1	35	4.5	85	165	40	F/L
SN5511	Wide-Band Diff Amp	63	3,000	5	—	1	0.6	4	±2.5	–0.2	700	5	95	165	6	F/L
Series 72 700/7510 (Operating Temperature Range 0°C to 70°C)																
SN72702	General-Purpose Op Amp	68	—	20	—	5	1.5	—	‡	—	200	10.6	80	80	5	F/L/N
SN72709	High-Performance Op Amp	93	—	250	—	2	0.1	—	±10	—	150	26	90	80	0.3	F/L/N
SN72710	Differential Comparator	62	—	—	—	2	1	7.5	—	—	200	—	—	110	25	F/L/N
SN72711	Dual Differential Comparator	64	—	—	—	1	0.5	5	—	—	200	—	—	130	25	F/L/N
SN72720	Dual Differential Comparator	62	—	—	—	2	1.8	7.5	—	—	200	—	98	220	25	N
SN7510	Wide-Band Video Amplifier	39	40,000	6	7	—	5	—	±1	3	35	4.5	85	165	50	F/L

‡0.5 to –4.

MOS INTEGRATED CIRCUITS

Type Number	Brief Description
TMS 1B 3016 LA	Dual 16-Bit Static Shift Register
TMS 7B 3000 LA	Dual 25-Bit Static Shift Register
TMS 7B 3001 LA	Dual 32-Bit Static Shift Register
TMS 7C 3002 LA	Dual 50-Bit Static Shift Register
TMS 7C 3003 LA	Dual 100-Bit Static Shift Register

Type Number	Brief Description
TMS 7A 4003 MC	256-Bit Random Access Memory
TMS 2A 4103 MH	Character Generator*
TMS 1A 6009 AA	6-Channel Analog Switch

*Part of 4100 Series — Character Generators that are programmable to customer requirements. Sample quantities are available preprogrammed.

OTHER INTEGRATED CIRCUITS

The following families of digital circuits are available, dependent on customer requirements. For information contact your TI sales engineer.

- **Series 51 and 51R† RCTL Digital**
- **Series 53 and 73 Modified-DTL Digital**
- **Series 17900L and 17800L RTL Digital**

†Series 51R are standard units that have undergone special testing and processing for severe-environmental applications.

SYSTEMS INTERFACE CIRCUITS

Series 5520 and 7520 Sense Amplifiers

- Fast overload recovery time
- Narrow threshold uncertainty region
- Transistor f_T of over 1 GHz
- Two sense channels per package (Series 7520)
- Cycle times as low as 200 ns

Series 5520 (Operating Temperature Range –55°C to 125°C)

Series 7520 (Operating Temperature Range 0°C to 70°C)

		TYPICAL CHARACTERISTICS											
		Differential-input threshold voltage V_T	Common-mode input firing voltage V_{CMF}	Logical 1 output voltage $V_{out(1)}$	Logical 0 output voltage $V_{out(0)}$	Logical 1 level input current (strobe or reset) $I_{in(1)}$	Logical 0 level input current (strobe or reset) $I_{in(0)}$	V_{CC1} supply current I_{CC1}	V_{CC2} supply current I_{CC2}	V_{ref} supply current I_{ref}	Minimum cycle time $t_{cyc(min)}$	Package (See Section 1)
		mV	V	V	V	mA	mA	mA	mA	mA	μs	
SN5524	Sense Amplifier	±5	3	4	0.25	0.005	–1	25	–15	0.03	0.2	J
SN5525	Sense Amplifier	±7	3	4	0.25	0.005	–1	25	–15	0.03	0.2	J
SN7520	Sense Amplifier (FF or Register-Type Output)	±4	3	4	0.25	0.005	–1	28	–14	0.03	0.2	N
SN7521	Sense Amplifier (FF or Register-Type Output)	±7	3	4	0.25	0.005	–1	28	–14	0.03	0.2	N
SN7522	Sense Amplifier (Open-Collector Output)	±4	3	4	0.2	0.005	–1	27	–15	0.03	0.2	N
SN7523	Sense Amplifier (Open-Collector Output)	±7	3	4	0.2	0.005	–1	27	–15	0.03	0.2	N
SN7524	Sense Amplifier (Separate AND Outputs)	±4	3	4	0.25	0.005	–1	25	–15	0.03	0.2	J/N
SN7525	Sense Amplifier (Separate AND Outputs)	±7	3	4	0.25	0.005	–1	25	–15	0.03	0.2	J/N
SN7528	Sense Amplifier (Separate AND Outputs)	±4	3	4	0.25	0.005	–1	25	–15	0.03	0.2	N
SN7529	Sense Amplifier (Separate AND Outputs)	±7	3	4	0.25	0.005	–1	25	–15	0.03	0.2	N

($15\ mV \leq V_{REF} \leq 40\ mV$)

Series 55 107/75 107 Line Circuits

- High Speed
- Standard Logic Supply Voltages
- TTL/DTL Compatible
- Dual Channels

Series 55 107 (Operating Temperature Range: –55°C to 125°C)

		V_{ID} Differential input voltage	V_{IH} High-level input voltage	V_{IL} Low-level input voltage	I_{IH} High-level input current	V_{ICM} Maximum common-mode input voltage range	P_D Total power dissipation	t_{plh}, Propagation delay time (differential inputs)	Package (See Section 1)
		mV	V	V	μA	V	mV	ns	
SN55107	Dual Line Receiver with SN5400 (TTL) Gate Output	3	—	—	30	±3	134	17	J
SN55108	Dual Line Receiver with SN5401 (Open-Collector) Gate Output	3	—	—	30	±3	134	19	J
SN55109	Dual Line Driver with 6-mA Typical Line Current	—	3.2	0.22	—	—	180	8	J
SN55110	Dual Line Driver with 12-mA Typical Line Current	—	3.2	0.22	—	—	285	9	J

Series 75 107 (Operating Temperature Range 0°C to 70°C)

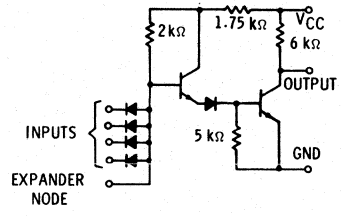
SN75107	Dual Line Receiver with SN5400 (TTL) Gate Output	3	—	—	30	±3	134	17	J/N
SN75108	Dual Line Receiver with SN5401 (Open-Collector) Gate Output	3	—	—	30	±3	134	19	J/N
SN75109	Dual Line Driver with 6-mA Typical Line Current	—	3.2	0.22	—	—	180	8	J/N
SN75110	Dual Line Driver with 12-mA Typical Line Current	—	3.2	0.22	—	—	285	9	J/N

OTHER QUALITY TI INTEGRATED CIRCUITS (Cont.)

STANDARD AND CUSTOM DTL

Series 15 930 and 15 830 DTL Digital

Typical Character.	Propagation Delay Time (Basic gate)	25 ns	
	Power Dissipation (each gate)	8 mW	
	D-c Noise Immunity	750 mV	
	Operating Temperature Range	–55°C to 125°C	0°C to 75°C
Package (See Section 1)		F, J, N, and R V_{CC} - Pin 14	Gnd - Pin 7
Functions	Dual 4-input NAND/NOR Gate	SN15930	SN15830
	Flip-flop with Set and Clear	SN15931	SN15831
	Dual 4-input NAND/NOR Buffer	SN15932	SN15832
	Dual 4-input Expander	SN15933	SN15833
	Hex Inverter	SN15936	SN15836
	Fast Rise-time Hex Inverter	SN15937	SN15837
	Dual 4-input NAND/NOR Power Gate	SN15944	SN15844
	Flip-flop with Set and Clear	SN15945	SN15845
	Quad 2-input NAND/NOR Gate	SN15946	SN15846
	Fast Rise-time Flip-flop with Set and Clear	SN15948	SN15848
	Quadruple 2-input NAND/NOR Fast Rise-time Gate	SN15949	SN15849
	Pulse-triggered Binary	SN15950	SN15850
	Monostable Multivibrator (One-shot)	SN15951	SN15851
	Dual 4-input NAND/NOR Fast Rise-time Gate	SN15961	SN15861
	Triple 3-input NAND/NOR Gate	SN15962	SN15862
	Triple 3-input NAND/NOR Fast Rise-time Gate	SN15963	SN15863
	Dual Flip-flop with Set	SN159093	SN158093
	Dual Fast Rise-time Flip-flop with Set	SN159094	SN158094
	Dual Fast Rise-time Flip-flop with Set and Clear	SN159097	SN158097
	Dual Flip-flop with Set and Clear	SN159099	SN158099



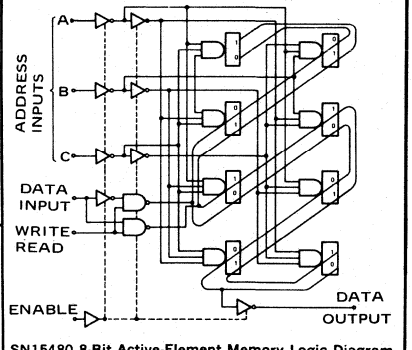
Typical Series 15930/15830 Circuit

Series 15 400 Custom Digital Logic Circuits*

• High fan-out • Improved gate-to-pin ratio • Improved a-c performance

Nominal Supply Voltage V_{CC}		4 V	
Typical Noise Immunity		1 V	
Maximum Recommended Fan-Out		43 Loads	
Functions		Package†	
	Dual 4-Input NAND/NOR Power Gate	N	SN15401
	Quadruple 2-Input Interface Gate	N	SN15402‡
	R-S Flip-Flop with Delay Control	L	SN15470
	8-Bit Active-Element Memory	L or N	SN15480
	4-Bit Register with Input and Output Clock	N	SN15490
	Dual Latch	L	SN15491

*For further information concerning these circuits, please contact DTL Product Marketing, Box 5012, M.S. 914 Dallas, Texas 75222, Phone 214-238-3081.
†See integrated circuits case outlines, (See Section 1)
‡Recommended maximum fan-out is 38.



SN15480 8-Bit Active-Element Memory Logic Diagram
Second Generation Bipolar Memory

STANDARD ECL

Series ECL2500*

TYPE	LOGIC FUNCTION	
ECL2500	Dual 4-Input	OR/NOR
ECL2501	9-Input	OR/NOR
ECL2502	Triple 2-Input	OR/NOR
ECL2503	Quad 2-Input	NOR
ECL2504	Quad Delay/Inverter	
ECL2505	Triple 3-Input	NOR
ECL2506	4-Wide 3-Input	NOR-OR
ECL2507	5-Wide 2-Input	NOR-OR
ECL2508	6-Wide 2-Input	NOR-OR
ECL2509	4-Wide 2-Input	OR-AND/NOR-OR
ECL2510	4-Wide 3–3–3–2 Input	OR-AND/NOR-OR
ECL2511	Quad 2-Input (Common Base)	OR
ECL2512	Dual 3-Wide 2-Input (Common Base)	NOR-OR
ECL2513	Dual 2-Wide 2-Input (Common Base)	OR-AND/NOR-OR
ECL2515	Four-Bit Group Carry	
ECL2516	Full Sum-Carry Adder	
ECL2517	Three-Bit Decoder with Enable	
	Multi-Output Gates (Drivers)	
ECL2520	Dual 2-Input (3 OR Outputs/Gate, 1 NOR Output/Gate)	OR/NOR
ECL2521	Dual 3-Input (3 OR Outputs/Gate)	OR
ECL2522	Dual 4-Input (2 NOR Outputs/Gate)	NOR
ECL2523	Dual 3-Input (3 NOR Outputs/Gate)	NOR
	Line Rec/Drivers	
ECL2530	Dual Differential-Amplifier Receiver	
ECL2531	Dual Line Driver	
	Converters	
ECL2536	Dual HLL/ECL	OR/NOR
ECL2537	Dual ECL/HLL	OR/NOR
	Storage	
ECL2540	Dual "D" latches	
ECL2541	Dual single-input gated clocked latch	
ECL2542	Dual 2-input gated clocked latch	
ECL2550	Active-element memory (4 word — 2 Bit)	

*ECL2500 circuits are available in the N package

ORDERING INSTRUCTIONS

Electrical characteristics presented in this catalog, unless otherwise noted, apply for circuit type(s) listed in the page heading regardless of package. The availability of a circuit function in a particular package is denoted by an alphabetical reference above the pin-connection diagram(s) of the TTL circuits described in Sections 2 through 11 and in a column of the tables (refer to Section C) listing other integrated circuits. These alphabetical designations refer to mechanical outline drawings shown in this section.

Factory orders for circuits described in this catalog should include a four-part type number as explained in the following example.

EXAMPLE: SN 54H72 S –02

1. Prefix
MUST CONTAIN TWO OR THREE LETTERS
(From Individual Data Sheet)

RSN	Radiation-Hardened Circuit
SN	Standard Prefix
SNR	Hi-Rel Processing Without Group B and C
SNT	Hi-Rel Processing With Group B and C
SNX	Experimental Circuit

2. Unique Circuit Description
MUST CONTAIN THREE TO SIX CHARACTERS
(From Individual Data Sheet)

Examples: 5410
74H10
74100
74H108
54L78

3. Package
MUST CONTAIN A SINGLE LETTER ONLY– F, H, J, L, N, R, S, or T
(From Pin-Connection Diagram On TTL Data Sheet)

4. Instructions (Dash No.)
MUST CONTAIN TWO NUMBERS
(From Dash No. Column of Following Table)

Packages	Formed Leads	Insulator	Mech-Pak Carrier	Solder-Dipped Leads	Order Dash No.
All	No	No	NA	No	00
F, R, S, T	Yes	Yes	No †	No	01
F, R, S, T	No	No	Yes	No	02
F, R, S, T	No	Yes	Yes	No	03
F, R, S, T	Yes	No	Yes	No	04
F, R, S, T	Yes	Yes	Yes	No	05
F, R, S, T	No	Yes	No †	No	06
F, R, S, T	Yes	No	No †	No	07
All	No	No	NA	Yes	10
F, R, S, T	Yes	Yes	No †	Yes	11
F, R, S, T	No	No	Yes	Yes	12
F, R, S, T	No	Yes	Yes	Yes	13
F, R, S, T	Yes	No	Yes	Yes	14
F, R, S, T	Yes	Yes	Yes	Yes	15
F, R, S, T	No	Yes	No †	Yes	16
F, R, S, T	Yes	No	No †	Yes	17

F – Flat package, metal, 0.500-inch tip-to-tip lead length, case electrically insulated from circuit
H – Flat package, electrically nonconductive ceramic, 0.750-inch tip-to-tip lead length
J – Dual-in-line package, electrically nonconductive ceramic, 0.300-inch row spacing
L – Plug-in package, metal, circular lead pattern
N – Dual-in-line package, electrically nonconductive plastic, 0.300-inch row spacing (0.600-inch row spacing for 24-pins)
R – Flat package, metal, 0.750-inch tip-to-tip lead length, case electrically insulated from circuit
S – Flat package, metal, 0.500-inch tip-to-tip lead length, case in electrical contact with circuit substrate and ground pin
T – Flat package, metal, 0.750-inch tip-to-tip lead length, case in electrical contact with circuit substrate and ground pin

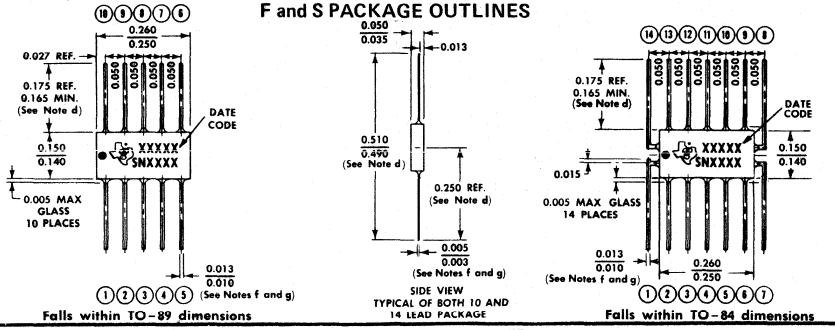
NOTE: Standard Series 54/74 SSI circuits described in Section 2 are being converted from the F package (case electrically insulated from circuit) to the S package (case in electrical contact with circuit substrate and ground pin). During this conversion period, orders for Series 54/74 SSI circuits may be filled with either F or S packages which otherwise are mechanically identical.

† These circuits are shipped in the Mech-Packette carrier.

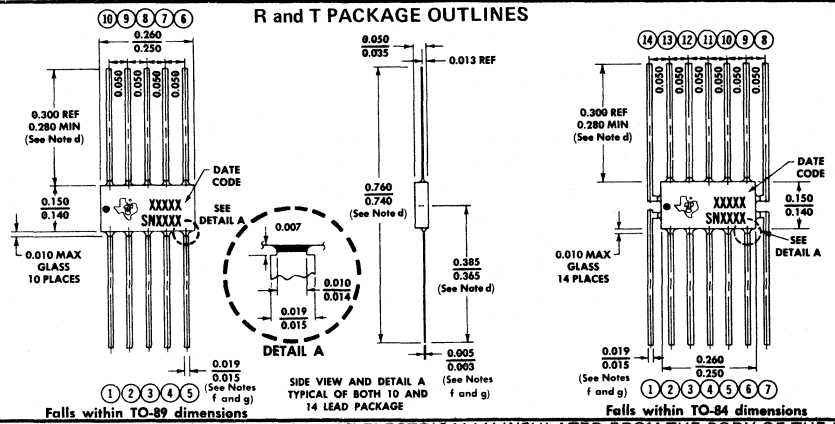
F, R, S, and T flat packages

These hermetic packages feature glass-to-metal seals and welded construction. Package body and leads are gold-plated F-15‡ glass-sealing alloy. Approximate weight is 0.1 gram. Each package is available with formed leads, insulator attached, solder-dipped leads, and/or mounted in a Mech-Pak carrier. Circuits not mounted in a Mech-Pak carrier are shipped in a Mech-Packette carrier. See Instructions (Dash No.) Table page 1-1.

F and S PACKAGE OUTLINES



R and T PACKAGE OUTLINES



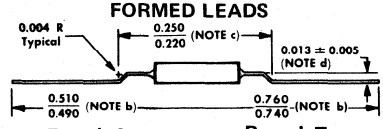
CIRCUIT SUBSTRATE AND GROUND PIN ARE ELECTRICALLY INSULATED FROM THE BODY OF THE F AND R PACKAGES. CIRCUIT SUBSTRATE IS IN ELECTRICAL CONTACT WITH THE GROUND PIN AND BODY OF THE S AND T PACKAGES.

NOTES:
a. All dimensions are in inches.
b. All decimals ± 0.005 except as noted.
c. Lead centerlines are located within ± 0.005 of their true positions relative to body centerlines. This is measured along lines located within 0.030 from (and parallel to) the sides of the package.
d. Not applicable in Mech-Pak carrier.
e. Symbolization denotes orientation of package.
f. This dimension does not apply for solder-dipped leads.
g. When solder-dipped leads are specified, dipped area of the lead extends from the lead tip to within 0.050 of the package body.

package leads

Gold-plated F-15‡ leads require no additional cleaning or processing when used in soldered or welded assembly. Solder-dipped leads are also available. Formed leads are available to facilitate planar mounting of networks on flat circuit boards. Networks can be removed from Mech-Pak carriers with lead lengths up to 0.175 inch for the F and S packages and up to 0.300 inch for the R and T packages.

FORMED LEADS



F and S R and T

NOTES:
a. All dimensions are in inches.
b. Not applicable in Mech-Pak Carrier.
c. Measured from centerline of outside bends.
d. Measured from center of lead to bottom of package where lead emerges from body.
e. When solder-dipped leads are specified, dipped area of lead extends from lead tip to outside bend (minimum).

‡F-15 is the ASTM designation for an iron-nickel-cobalt alloy containing nominally 53% iron, 29% nickel, and 17% cobalt.

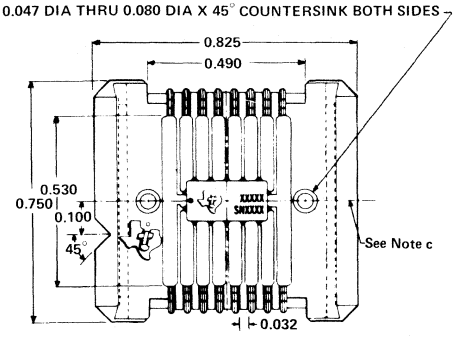
SNH-4 insulator

An SNG-4 insulator, secured to the back surface of the package, permits the mounting of networks on circuit boards which have conductors passing beneath the package. The insulator is 0.0025 inch thick and has an insulation resistance of greater than 10 megohms at 25°C.

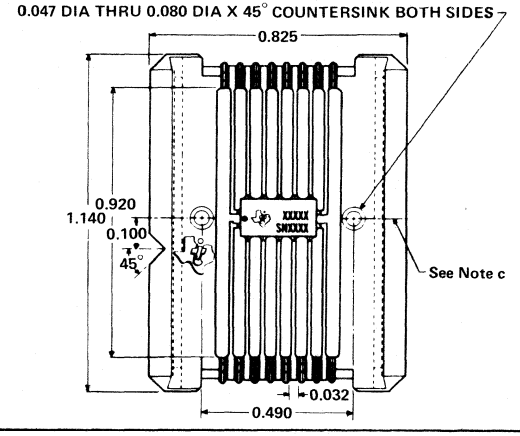
flat package mech-pak carriers

The Mech-Pak carrier facilitates handling the network and is compatible with automatic equipment used for testing and assembly. The carrier is particularly appropriate for mechanized assembly operations and will withstand temperatures up to 125°C for indefinite periods. The outline drawings below illustrate the Mech-Pak carriers for the F/S and R/T flat packages with a 14-pin package installed. These same carriers are utilized for 10-pin flat packages with the package body in the same location.

F and S PACKAGE MECH-PAK OUTLINE



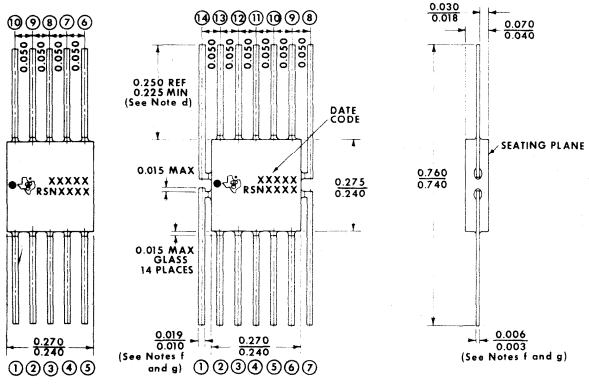
R and T PACKAGE MECH-PAK OUTLINE



NOTES: a. All dimensions are nominal in inches unless otherwise specified.
b. Overall thickness is 0.175 and nestled height is 0.150 each.
c. In the plane shown, package centerline is located within ± 0.015 of the tooling holes centerline.

H flat packages

These packages each consist of a ceramic base, ceramic cap, and a 10- or 14-lead frame. Hermetic sealing is accomplished with glass. Gold-plated leads (–00) require no additional cleaning or processing when used in welded or soldered assembly. Solder-dipped leads (–10) are also available.



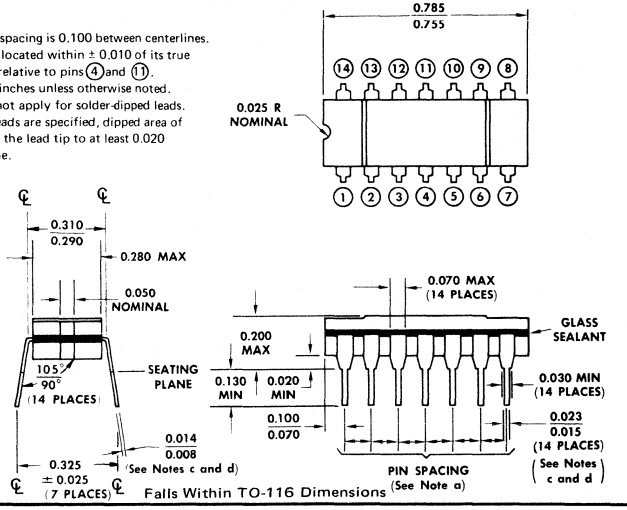
NOTES:
a. All dimensions are in inches.
b. All decimals ± 0.005 except as noted.
c. Lead centerlines are located within ± 0.005 of their true positions relative to body centerlines. This is measured along lines located within 0.030 from (and parallel to) the sides of the package.
d. Not applicable in Mech-Pak carrier.
e. Symbolization denotes orientation of package.
f. This dimension does not apply for solder-dipped leads.
g. When solder-dipped leads are specified, dipped area of the lead extends from the lead tip to within 0.050 of the package body.

J dual-in-line ceramic packages

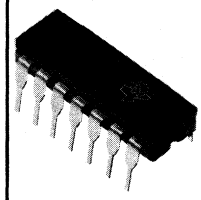
These hermetically-sealed, dual-in line packages consist of a ceramic base, ceramic cap, and a 14- or 16-lead frame. The circuit bar is alloy-mounted to the base and hermetic sealing is accomplished with glass. This package is intended for insertion in mounting-hole rows on 0.300-inch centers. Once the leads are compressed to 0.300-inch separation and inserted, sufficient tension is provided to secure the package in the board during soldering. Tin-plated ("bright-dipped") leads (–00) require no additional cleaning or processing when used in soldered assembly. Solder-dipped leads (–10) are also available.

14-PIN CERAMIC DUAL-IN-LINE J-PACKAGE OUTLINE

NOTES: a. The true-position pin spacing is 0.100 between centerlines. Each pin centerline is located within ± 0.010 of its true longitudinal position relative to pins ④ and ⑪.
b. All dimensions are in inches unless otherwise noted.
c. This dimension does not apply for solder-dipped leads.
d. When solder-dipped leads are specified, dipped area of the lead extends from the lead tip to at least 0.020 above the seating plane.

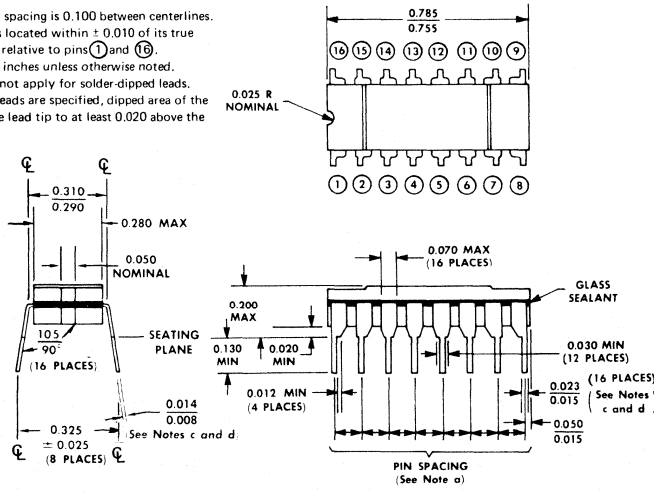


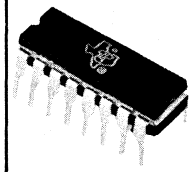
Falls Within TO-116 Dimensions



16-PIN CERAMIC DUAL-IN-LINE J-PACKAGE OUTLINE

NOTES: a. The true-position pin spacing is 0.100 between centerlines. Each pin centerline is located within ± 0.010 of its true longitudinal position relative to pins ① and ⑯.
b. All dimensions are in inches unless otherwise noted.
c. This dimension does not apply for solder-dipped leads.
d. When solder-dipped leads are specified, dipped area of the lead extends from the lead tip to at least 0.020 above the seating plane.

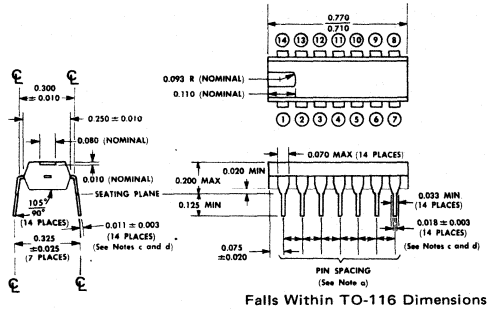




N dual-in-line plastic packages

These dual-in-line packages consist of a circuit mounted on a 14-, 16- or 24-lead frame and encapsulated within an electrically nonconductive, plastic compound. The compound will withstand soldering temperature with no deformation and circuit performance characteristics remain stable when operated in high-humidity conditions. These packages are intended for insertion in mounting-hole rows on 0.300-inch (or 0.600-inch) centers. Once the leads are compressed and inserted, sufficient tension is provided to secure the package in the board during soldering. Silver-plated leads (–00) require no additional cleaning or processing when used in solder assembly. Solder-dipped leads (–10) are also available.

14-PIN PLASTIC DUAL-IN-LINE N-PACKAGE OUTLINE



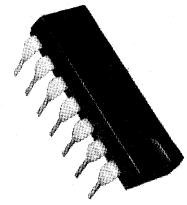
Falls Within TO-116 Dimensions

NOTES: a. The true-position pin spacing is 0.100 between centerlines. Each pin centerline is located within ±0.010 of its true longitudinal position relative to pins (4) and (11).

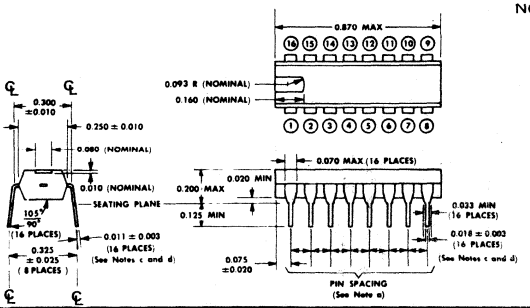
b. All dimensions are in inches unless otherwise noted.

c. This dimension does not apply for solder-dipped leads.

d. When solder-dipped leads are specified dipped area of the lead extends from the lead tip to at least 0.020 above the seating plane.



16-PIN PLASTIC DUAL-IN-LINE N-PACKAGE OUTLINE

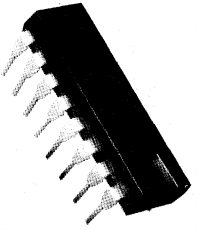


NOTES: a. The true-position pin spacing is 0.100 between centerlines. Each pin centerline is located within ±0.010 of its true longitudinal position relative to pins (1) and (16).

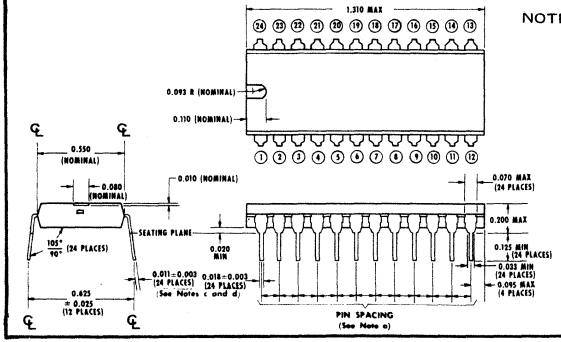
b. All dimensions are in inches unless otherwise noted.

c. This dimension does not apply for solder-dipped leads.

d. When solder-dipped leads are specified dipped area of the lead extends from the lead tip to at least 0.020 above the seating plane.



24-PIN PLASTIC DUAL-IN-LINE N-PACKAGE OUTLINE

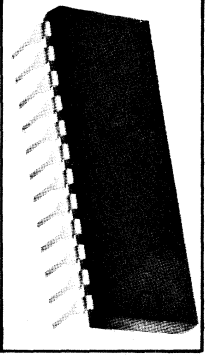


NOTES: a. The true-position pin spacing is 0.100 between centerlines. Each pin centerline is located within ±0.010 of its true longitudinal position relative to pins (1) and (24).

b. All dimensions are in inches unless otherwise noted.

c. This dimension does not apply for solder-dipped leads.

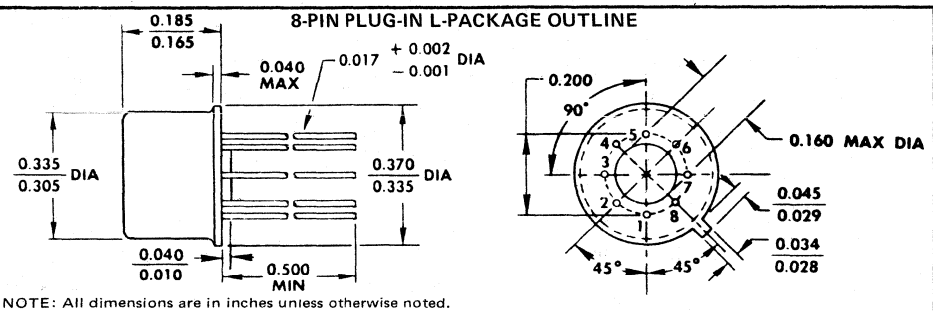
d. When solder-dipped leads are specified dipped area of the lead extends from the lead tip to at least 0.020 above the seating plane.



L plug-in packages

These hermetically sealed, plug-in packages each consist of a welded metal base and cap with individual leads secured by an insulating glass sealant. The gold-plated leads (–00) require no additional cleaning or processing when used in soldered assembly. Solder-dipped leads (–10) are also available.

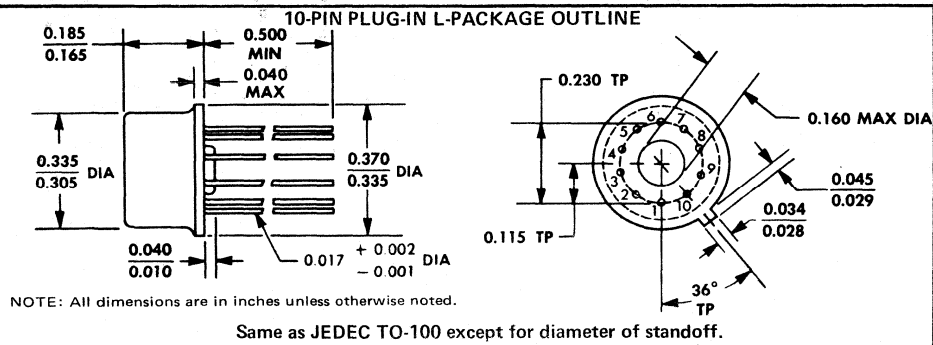
8-PIN PLUG-IN L-PACKAGE OUTLINE



NOTE: All dimensions are in inches unless otherwise noted.

Same as JEDEC TO-99 except for diameter of standoff.

10-PIN PLUG-IN L-PACKAGE OUTLINE



NOTE: All dimensions are in inches unless otherwise noted.

Same as JEDEC TO-100 except for diameter of standoff.

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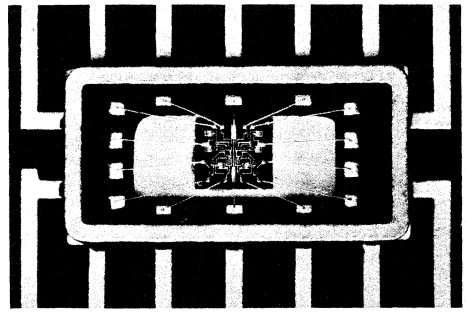
TI TTL

Integrated Circuits

HIGH-SPEED SATURATED TRANSISTOR-TRANSISTOR LOGIC CIRCUITS FOR GENERAL-PURPOSE DIGITAL SYSTEM APPLICATIONS

description



TYPE SN5400 PRIOR TO CAPPING

Series 54/74 integrated circuits are designed and characterized for high-speed, general-purpose digital applications where high d-c noise margin and relatively low power dissipation are important system considerations. This logic series includes the basic gates, flip-flop elements, and complex logic and storage elements needed to perform all functions of general-purpose digital systems. Series 54 and 74 are completely compatible with Series 54H/74H and Series 54L/74L TTL logic families. Compatibility of these three TTL families permits improved systems design as the logician is permitted the flexibility of selecting component switching speed or circuit power dissipation with respect to system requirements. Series 54H/74H high-speed TTL circuits can be selectively used to perform those functions requiring minimal propagation delay times. Series 54L/74L low-power TTL circuits can be used to reduce total power requirements. All three TTL families are designed to operate at the same supply voltages and compatible logic levels. In addition, high d-c noise margins characteristic of TTL circuits are maintained.

Definitive specifications are provided for operating characteristics over the full military temperature range of −55°C to 125°C for Series 54 circuits, and over the temperature range of 0°C to 70°C for Series 74 circuits.

features

LOW SYSTEM COST

- choice of packages — high-density flat package
  — economical dual-in-line plastic package
  — ceramic dual-in-line package
- broad selection of SSI and MSI functions — reduces package count

OPTIMUM CIRCUIT PERFORMANCE

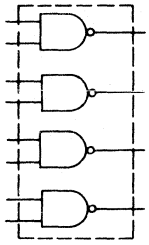
- high speed — typical gate propagation delay time of 10 ns
- high d-c noise margin — typically one volt
- low output impedance provides low a-c noise susceptibility
- waveform integrity over full range of loading and temperature conditions
- low power dissipation — 10 mW per gate at 50% duty cycle
- full fan-out 10 Series 54/74 loads
  40 Series 54L/74L loads
  8 Series 54H/74H loads
- compatible for use with other current-sinking logic families — DTL, other TTL

CONTENTS

standard line summary

NAND/NOR GATES

SN5400
SN7400
SEE PAGE 2-5



QUADRUPLE 2-INPUT
POSITIVE NAND GATES

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SN7403
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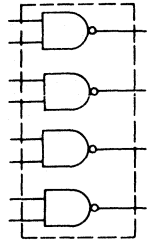

QUADRUPLE 2-INPUT
POSITIVE NAND GATES
(WITH OPEN-COLLECTOR OUTPUT)

SN5402
SN7402
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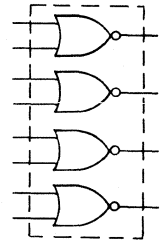

QUADRUPLE 2-INPUT
POSITIVE NAND GATES

SN5404
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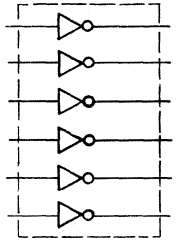

HEX INVERTERS

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SN7405
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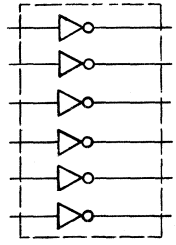

HEX INVERTERS
(WITH OPEN-COLLECTOR OUTPUT)

SN5410
SN7410
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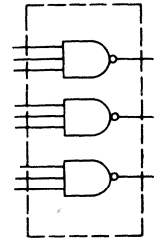

TRIPLE 3-INPUT
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SN5420
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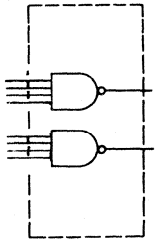

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POSITIVE NAND GATES

SN5430
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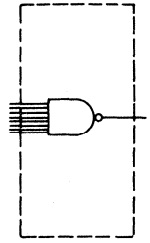

8-INPUT
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SN5440
SN7440
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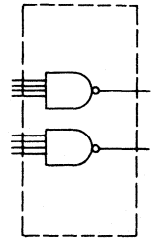

DUAL 4-INPUT
POSITIVE NAND BUFFERS

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standard line summary (continued)

AND–OR–INVERT GATES

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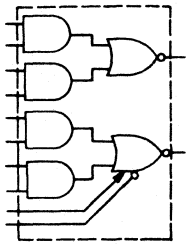
SN7450



EXPANDABLE DUAL 2-WIDE 2-INPUT AND-OR-INVERT GATES

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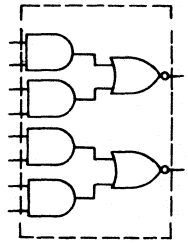

DUAL 2-WIDE 2-INPUT AND-OR-INVERT GATES

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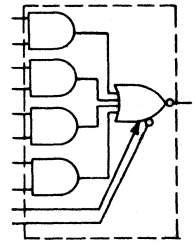
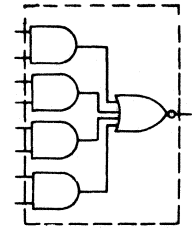


EXPANDABLE 4-WIDE 2-INPUT AND-OR-INVERT GATES

SN5454 SEE PAGE 2-19
SN7454



4-WIDE 2-INPUT AND-OR-INVERT GATES

EXPANDERS

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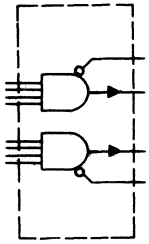

DUAL 4-INPUT EXPANDERS

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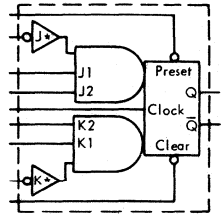
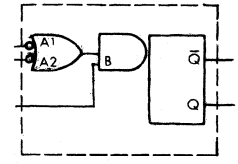


EDGE-TRIGGERED J-K FLIP-FLOPS

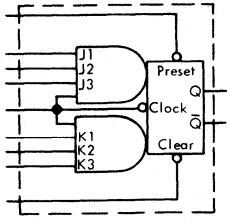
ONE-SHOTS

SN54121 SEE PAGE 2-38
SN74121



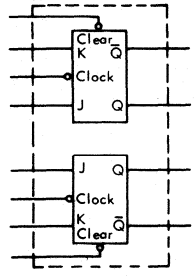
MONOSTABLE MULTIVIBRATORS

SN5472 SEE PAGE 2-26
SN7472



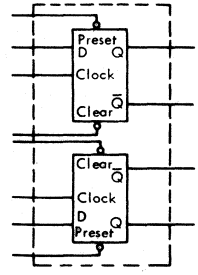
J-K MASTER-SLAVE FLIP-FLOPS

SN5473 SEE PAGE 2-29
SN7473
SN54107 SEE PAGE 2-29
SN74107



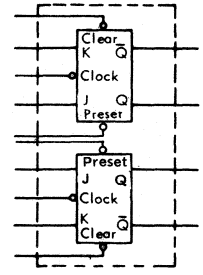
DUAL J-K MASTER-SLAVE FLIP-FLOPS

SN5474 SEE PAGE 2-32
SN7474



DUAL D-TYPE EDGE-TRIGGERED FLIP-FLOPS

SN5476 SEE PAGE 2-35
SN7476



DUAL J-K MASTER-SLAVE FLIP-FLOPS

FOR SUMMARY OF TTL MSI FUNCTIONS —

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply Voltage V_{CC} (See Note 1)	7 V
Input Voltage, V_{in} (See Notes 1 and 2)	5.5 V
Resistor Node Voltage SN54121, SN74121 (See Note 1)	−5.5 V to 7 V
Operating Free-Air Temperature Range: Series 54 Circuits	−55°C to 125°C
Series 74 Circuits	0°C to 70°C
Storage Temperature Range	−65°C to 150°C

NOTES: 1. Voltage values are with respect to network ground terminal.
2. Input signals must be zero or positive with respect to network ground terminal.

logic definition

Series 54/74 logic is defined in terms of standard POSITIVE LOGIC using the following definitions:

LOW VOLTAGE = LOGICAL 0
HIGH VOLTAGE = LOGICAL 1

input-current requirements

Input-current requirements reflect worst-case conditions over the specified recommended operating free-air temperature and V_{CC} ranges. Each input, of the multiple emitter input transistors which have a 4-kΩ base resistor, requires that no more than −1.6 mA flow out of the input at a logical 0 voltage level; therefore, one load (N = 1) is −1.6 mA maximum. Each input requires current into the input at a logical 1 voltage level. This current is 40 μA maximum for each emitter of input transistors with the 4-kΩ base resistor. Currents into the input terminals are specified as positive values. Arrows on the d-c test circuits indicate the actual direction of current flow.

fan-out capability

Fan-out reflects the ability of an output to sink current from a number of loads (N) at a logical 0 voltage level and to supply current at a logical 1 voltage level. Each standard output is capable of sinking current or supplying current to 10 loads (N = 10). The buffer gate is capable of sinking current or supplying current to 30 loads (N = 30). Load currents (out of the output terminal) are specified as negative values. Arrows on the d-c test circuits indicate the actual direction of current flow.

Series 54/74 circuits are well suited for driving Series 54H/74H high-speed TTL and Series 54L/74L low-power TTL circuits. As examples, a Series 54/74 output, rated for a fan-out of ten (N = 10), will drive eight 54H/74H loads or forty 54L/74L loads. See Section 12 for more detailed explanation of drive capabilities.

Circuit inputs requiring current drive in excess of one normalized load are indicated by shading in the electrical characteristics tables.

unused inputs

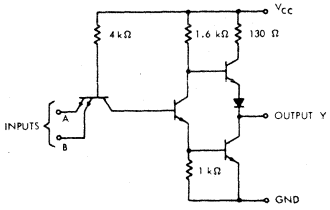
For optimum switching times and minimum noise susceptibility unused inputs should be maintained at a positive voltage greater than 2.4 V but not to exceed the absolute maximum rating of 5.5 V. This eliminates the distributed capacitance associated with the floating input-transistor emitter, bond wire, and package lead, and ensures that no degradation will occur in the propagation delay times. Some possible ways of handling input emitters are:

a. Connect unused inputs to an independent supply voltage. Preferably, this voltage should be between 2.4 V and 3.5 V.

b. Connect unused inputs to a used input if maximum fan-out of the driving output will not be exceeded. Each input presents a full load in the logical 1 state to the driving output.

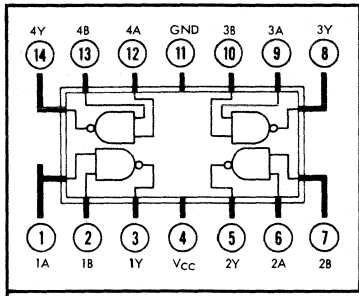
c. Connect unused inputs to V_{CC} through a 1-kΩ resistor so that if a transient which exceeds the 5.5-V maximum rating should occur, the impedance will be high enough to protect the input. One to 25 unused inputs may be connected to each 1-kΩ resistor.

schematic (each gate)

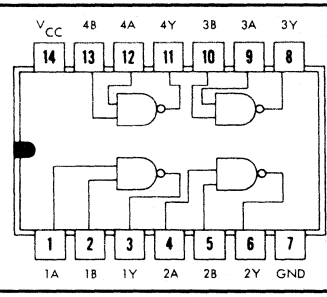


NOTE: Component values shown are nominal.

F FLAT PACKAGE
(TOP VIEW)



J OR N DUAL-IN-LINE PACKAGE
(TOP VIEW)



positive logic: $Y = \overline{AB}$

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply Voltage V_{CC}:	SN5400 Circuits	4.5	5	5.5	V
	SN7400 Circuits	4.75	5	5.25	V
Normalized Fan-Out From Each Output, N				10	
Operating Free-Air Temperature Range, T_A:	SN5400 Circuits	−55	25	125	°C
	SN7400 Circuits	0	25	70	°C

electrical characteristics (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
$V_{in(1)}$	Logical 1 input voltage required at both input terminals to ensure logical 0 level at output	1	V_{CC} = MIN		2			V
$V_{in(0)}$	Logical 0 input voltage required at either input terminal to ensure logical 1 level at output	2	V_{CC} = MIN				0.8	V
$V_{out(1)}$	Logical 1 output voltage	2	V_{CC} = MIN, V_{in} = 0.8 V, I_{load} = −400 μA		2.4	3.3		V
$V_{out(0)}$	Logical 0 output voltage	1	V_{CC} = MIN, V_{in} = 2 V, I_{sink} = 16 mA			0.22	0.4	V
$I_{in(0)}$	Logical 0 level input current (each input)	3	V_{CC} = MAX, V_{in} = 0.4 V				−1.6	mA
$I_{in(1)}$	Logical 1 level input current (each input)	4	V_{CC} = MAX, V_{in} = 2.4 V				40	μA
			V_{CC} = MAX, V_{in} = 5.5 V				1	mA
I_{OS}	Short-circuit output current§	5	V_{CC} = MAX	SN5400	−20		−55	mA
				SN7400	−18		−55	
$I_{CC(0)}$	Logical 0 level supply current	6	V_{CC} = MAX, V_{in} = 5 V			12	22	mA
$I_{CC(1)}$	Logical 1 level supply current	6	V_{CC} = MAX, V_{in} = 0			4	8	mA

switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{pd0}	Propagation delay time to logical 0 level	65	C_L = 15 pF, R_L = 400 Ω		7	15	ns
t_{pd1}	Propagation delay time to logical 1 level	65	C_L = 15 pF, R_L = 400 Ω		11	22	ns

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

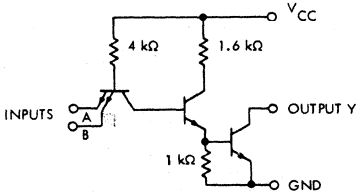
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

§ Not more than one output should be shorted at a time.

—SEE ORDERING INSTRUCTIONS PAGE 1-1—

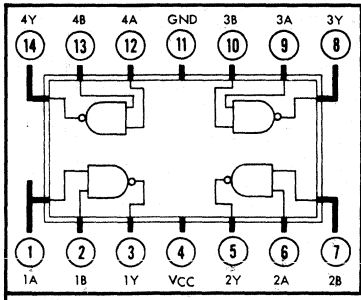
CIRCUIT TYPES SN5401, SN7401
QUADRUPLE 2-INPUT POSITIVE NAND GATES
(WITH OPEN-COLLECTOR OUTPUT)

schematic (each gate)

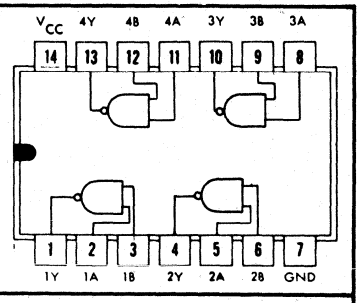


NOTE: Component values shown are nominal.

F FLAT PACKAGE
(TOP VIEW)



J OR N DUAL-IN-LINE PACKAGE
(TOP VIEW)



positive logic: $Y = \overline{AB}$

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply Voltage V_{CC}: SN5401 Circuits	4.5	5	5.5	V
SN7401 Circuits	4.75	5	5.25	V
Normalized Fan-Out From Each Output, N			10	
Operating Free-Air Temperature Range, T_A: SN5401 Circuits	−55	25	125	°C
SN7401 Circuits	0	25	70	°C

electrical characteristics (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS†	MIN	TYP‡	MAX	UNIT
$V_{in(1)}$	Logical 1 input voltage required at both input terminals to ensure logical 0 (on) level at output	1	V_{CC} = MIN	2			V
$V_{in(0)}$	Logical 0 input voltage required at either input terminal to ensure logical 1 (off) level at output	7	V_{CC} = MIN			0.8	V
$I_{out(1)}$	Output reverse current	7	V_{CC} = MIN, $V_{in(0)}$ = 0.8 V, $V_{out(1)}$ = 5.5 V			250	μA
$V_{out(0)}$	Logical 0 output voltage (on level)	1	V_{CC} = MIN, V_{in} = 2 V, I_{sink} = 16 mA			0.4	V
$I_{in(0)}$	Logical 0 level input current (each input)	3	V_{CC} = MAX, V_{in} = 0.4 V			−1.6	mA
$I_{in(1)}$	Logical 1 level input current (each input)	4	V_{CC} = MAX, V_{in} = 2.4 V			40	μA
			V_{CC} = MAX, V_{in} = 5.5 V			1	mA
$I_{CC(0)}$	Logical 0 level supply current	6	V_{CC} = MAX, V_{in} = 5 V		12	22	mA
$I_{CC(1)}$	Logical 1 level supply current	6	V_{CC} = MAX, V_{in} = 0		4	8	mA

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{pd0}	Propagation delay time to logical 0 level	65	C_L = 15 pF, R_L = 400 Ω		8	15	ns
t_{pd1}	Propagation delay time to logical 1 level	65	C_L = 15 pF, R_L = 4 kΩ		35	45	ns

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

–SEE ORDERING INSTRUCTIONS PAGE 1-1–

APPLICATION DATA

combined fan-out and wire-OR capabilities

The open-collector TTL gate, when supplied with a proper load resistor (R_L), can be paralleled with other similar TTL gates to perform the wire-OR function, and simultaneously, will drive from one to nine TTL loads. When no other open-collector gates are paralleled, this gate can be used to drive ten TTL loads. For any of these conditions an appropriate load resistor value must be determined for the desired circuit configuration. A maximum resistor value must be determined which will ensure that sufficient load current (to TTL loads) and off current (through paralleled outputs) will be available during a logical 1 level at output. A minimum resistor value must be determined which will ensure that current through this resistor and sink current from the TTL loads will not cause the output voltage to rise above the logical 0 level even if one of the paralleled outputs is sinking all the current.

In both conditions (logical 0 and logical 1) the value of R_L is determined by:

$$R_L = \frac{V_{RL}}{I_{RL}}$$

where: V_{RL} is the voltage drop in volts, and I_{RL} is the current in amperes.

logical 1 (off level) circuit calculations (see figure F)

The allowable voltage drop across the load resistor (V_{RL}) is the difference between V_{CC} applied and the $V_{out(1)}$ level required at the load:

$$V_{RL} = V_{CC} - V_{out(1)\ required}$$

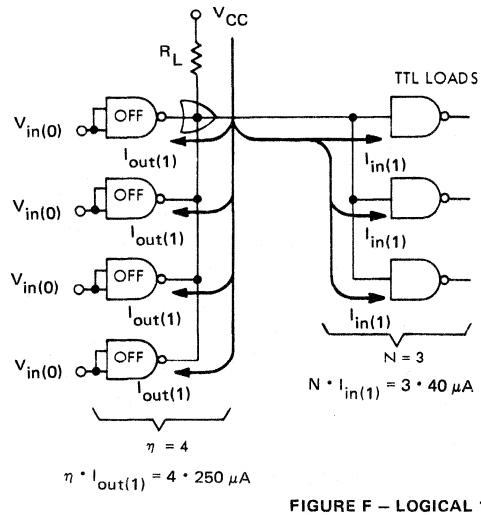
The total current through the load resistor (I_{RL}) is the sum of the load currents ($I_{in(1)}$) and off-level reverse currents ($I_{out(1)}$) through each of the wire-OR connected outputs:

$$I_{RL} = \eta \cdot I_{out(1)} + N \cdot I_{in(1)} \text{ to TTL loads}$$

Therefore, calculations for the maximum value of R_L would be:

$$R_{L(max)} = \frac{V_{CC} - V_{out(1)\ required}}{\eta \cdot I_{out(1)} + N \cdot I_{in(1)}}$$

where: η = number of gates wire-OR connected, and N = number of TTL loads.



Calculation:

$$R_{L(max)} = \frac{V_{CC} - V_{out(1)\ required}}{\eta \cdot I_{out(1)} + N \cdot I_{load}}$$

$$R_{L(max)} = \frac{5 - 2.4}{0.001 + 0.00012} = \frac{2.6}{0.00112} = 2321\ \Omega$$

FIGURE F – LOGICAL 1 CIRCUIT CONDITIONS

APPLICATION DATA

logical 0 (on level) circuit calculations (see figure G)

The current through the resistor must be limited to the maximum sink-current capability of one output transistor. Note that if several output transistors are wire-OR connected, the current through R_L may be shared by those paralleled transistors. However, unless it can be absolutely guaranteed that more than one transistor will be on during logical 0 periods, the current must be limited to 16 mA, the maximum current which will ensure a logical 0 maximum of 0.4 volts.

Also, fan-out must be considered. Part of the 16 mA will be supplied from the inputs which are being driven. This reduces the amount of current allowed through R_L.

Therefore, the equation used to determine the minimum value of R_L is:

$$R_{L(min)} = \frac{V_{CC} - V_{out(0)\ required}}{I_{sink}\ capability - I_{sink}\ from\ TTL\ loads}$$

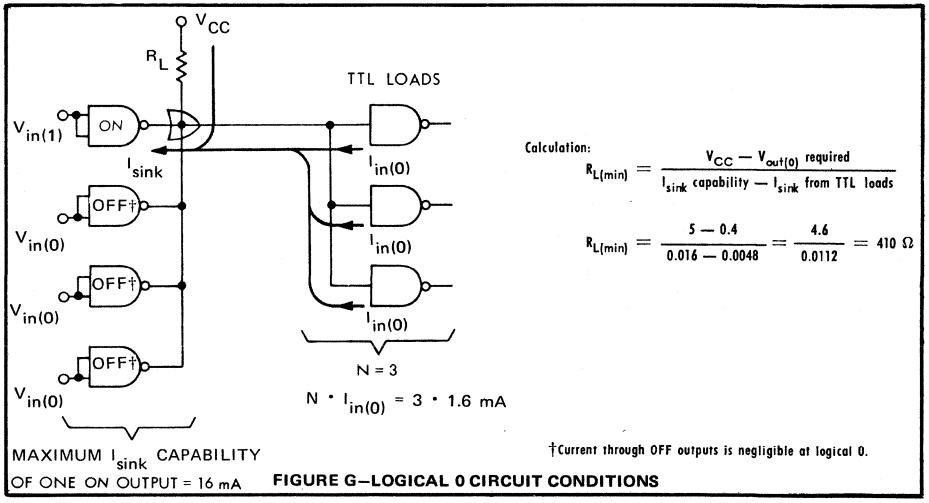


FIGURE G—LOGICAL 0 CIRCUIT CONDITIONS

driving TTL loads and combining outputs

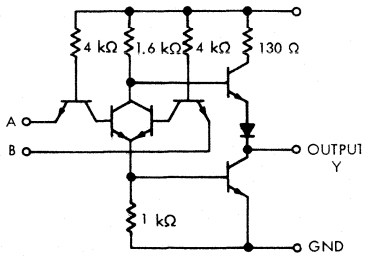
Table 1 provides minimum and maximum resistor values, calculated from equations shown above, for driving one to ten TTL loads and wire-OR connecting two to seven parallel outputs. Each value shown for one wire-OR output is determined by the fan-out plus the cutoff current of a single output transistor. Extension beyond seven wire-OR connections is permitted with fan-outs of seven or fewer if a valid minimum and maximum R_L is possible. When fanning-out to ten TTL loads, the calculation for the minimum value of R_L indicates that an infinite resistance should be used ($V_{RL} \div 0 = \infty$); however, the use of a 4 kΩ resistor in this case will satisfy the logical 1 condition and limit the logical 0 level to less than 0.43 V.

FAN-OUT TO TTL LOADS	WIRE-OR OUTPUTS							
	1	2	3	4	5	6	7	1 to 7
1	8965	4814	3291	2500	2015	1688	1452	319
2	7878	4482	3132	2407	1954	1645	1420	359
3	7027	4193	2988	2321	1897	1604	1390	410
4	6341	3939	2857	2241	1843	1566	1361	479
5	5777	3714	2736	2166	1793	1529	1333	575
6	5306	3513	2626	2096	1744	1494	1306	718
7	4905	3333	2524	2031	1699	1460	1280	958
8	4561	3170	2429	1969	1656	X	X	1437
9	4262	3023	X	X	X	X	X	2875
10	4000	X	X	X	X	X	X	4000§
	MAXIMUM							MIN

TABLE 1—LOAD RESISTOR VALUE IN OHMS

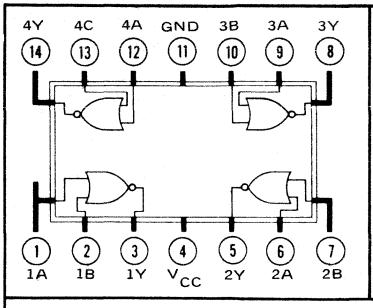
‡ All values shown in the table are based on:
Logical 1 conditions: V_{CC} = 5 V, $V_{out(1)}$ required = 2.4 V
Logical 0 conditions: V_{CC} = 5 V, $V_{out(0)}$ required = 0.4 V
§ — The theoretical value is ∞. See explanation in text.
X — Not recommended or not possible.

schematic (each gate)

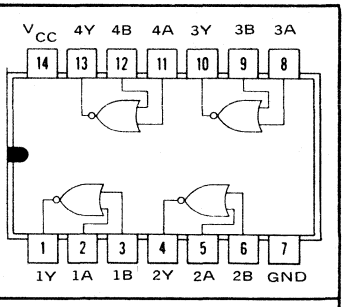


NOTE: Component values shown are nominal.

S FLAT PACKAGE
(TOP VIEW)



J OR N-DUAL-IN-LINE PACKAGE
(TOP VIEW)



positive logic: $Y = \overline{A + B}$

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply Voltage V_{CC}: SN5402 Circuits	4.5	5	5.5	V
SN7402 Circuits	4.75	5	5.25	V
Normalized Fan-Out From Each Output, N			10	
Operating Free-Air Temperature Range, T_A: SN5402 Circuits	−55	25	125	°C
SN7402 Circuits	0	25	70	°C

electrical characteristics (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
$V_{in(1)}$	Logical 1 input voltage required at either input terminal to ensure logical 0 level at output	8	V_{CC} = MIN		2			V
$V_{in(0)}$	Logical 0 input voltage required at both input terminals to ensure logical 1 level at output	9	V_{CC} = MIN				0.8	V
$V_{out(1)}$	Logical 1 output voltage	9	V_{CC} = MIN, V_{in} = 0.8 V, I_{load} = −400 μA		2.4	3.3		V
$V_{out(0)}$	Logical 0 output voltage	10	V_{CC} = MIN, V_{in} = 2 V, I_{sink} = 16 mA			0.22	0.4	V
$I_{in(0)}$	Logical 0 level input current (each input)	11	V_{CC} = MAX, V_{in} = 0.4 V				−1.6	mA
$I_{in(1)}$	Logical 1 level input current (each input)	12	V_{CC} = MAX, V_{in} = 2.4 V				40	μA
			V_{CC} = MAX, V_{in} = 5.5 V				1	mA
I_{OS}	Short-circuit output current§	13	V_{CC} = MAX	SN5402	−20		−55	mA
				SN7402	−18		−55	
$I_{CC(0)}$	Logical 0 level supply current	14	V_{CC} = MAX, V_{in} = 5 V			14	27	mA
$I_{CC(1)}$	Logical 1 level supply current	14	V_{CC} = MAX, V_{in} = 0			8	16	mA

switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{pd0}	Propagation delay time to logical 0 level	65	C_L = 15 pF, R_L = 400 Ω		8	15	ns
t_{pd1}	Propagation delay time to logical 1 level	65	C_L = 15 pF, R_L = 400 Ω		12	22	ns

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

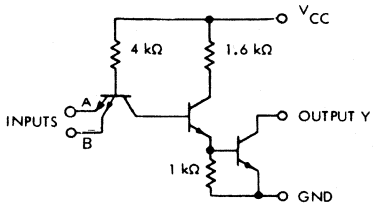
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

§ Not more than one output should be shorted at a time.

—SEE ORDERING INSTRUCTIONS PAGE 1-1—

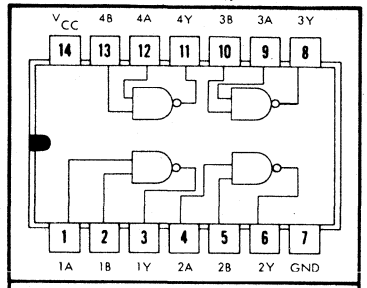
CIRCUIT TYPES SN5403, SN7403
QUADRUPLE 2-INPUT POSITIVE NAND GATES
(WITH OPEN-COLLECTOR OUTPUT)

schematic (each gate)



NOTE: Component values shown are nominal.

J OR N DUAL-IN-LINE PACKAGE
(TOP VIEW)



positive logic: $Y = \overline{AB}$

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply Voltage V_{CC}: SN5403 Circuits	4.5	5	5.5	V
SN7403 Circuits	4.75	5	5.25	V
Normalized Fan-Out From Each Output, N (and see pages 2-7 and 2-8)			10	
Operating Free-Air Temperature Range, T_A: SN5403 Circuits	−55	25	125	°C
SN7403 Circuits	0	25	70	°C

electrical characteristics (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS†	MIN	TYP‡	MAX	UNIT
$V_{in(1)}$	Logical 1 input voltage required at both input terminals to ensure logical 0 (on) level at output)	1	V_{CC} = MIN	2			V
$V_{in(0)}$	Logical 0 input voltage required at either input terminal to ensure logical 1 (off) level at output	7	V_{CC} = MIN, V_{in} = 0.8 V,			0.8	V
$I_{out(1)}$	Output reverse current	7	V_{CC} = MIN, V_{in} = 2 V, $V_{out(1)}$ = 5.5 V			250	μA
$V_{out(0)}$	Logical 0 output voltage (on level)	1	V_{CC} = MIN, I_{sink} = 16 mA			0.4	V
$I_{in(0)}$	Logical 0 level input current (each input)	3	V_{CC} = MAX, V_{in} = 0.4 V			−1.6	mA
$I_{in(1)}$	Logical 1 level input current (each input)	4	V_{CC} = MAX, V_{in} = 2.4 V			40	μA
			V_{CC} = MAX, V_{in} = 5.5 V			1	mA
$I_{CC(0)}$	Logical 0 level supply current	6	V_{CC} = MAX, V_{in} = 5 V		12	22	mA
$I_{CC(1)}$	Logical 1 level supply current	6	V_{CC} = MAX, V_{in} = 0		4	8	mA

switching characteristics, V_{CC} = 5 V, T_A = 25°C

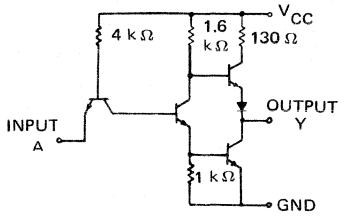
PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{pd0}	Propagation delay time to logical 0 level	65	C_L = 15 pF, R_L = 400 Ω		8	15	ns
t_{pd1}	Propagation delay time to logical 1 level	65	C_L = 15 pF, R_L = 4 kΩ		35	45	ns

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

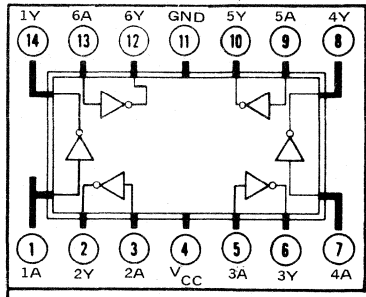
—SEE ORDERING INSTRUCTIONS PAGE 1-1—

schematic (each inverter)

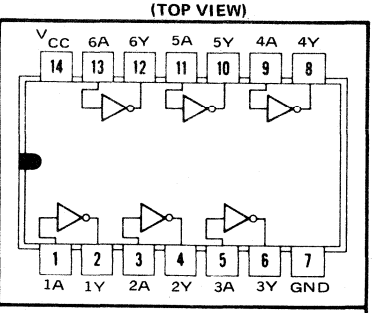


NOTE: Component values shown are nominal

S FLAT PACKAGE
(TOP VIEW)



J OR N DUAL-IN-LINE PACKAGE
(TOP VIEW)



positive logic: $Y = \overline{A}$

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply Voltage V_{CC}: SN5404 Circuits	4.5	5	5.5	V
SN7404 Circuits	4.75	5	5.25	V
Normalized Fan-Out From Each Output, N			10	
Operating Free-Air Temperature Range, T_A: SN5404 Circuits	−55	25	125	°C
SN7404 Circuits	0	25	70	°C

electrical characteristics (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
$V_{in(1)}$	Logical 1 input voltage required at input terminal to ensure logical 0 level at output	15	V_{CC} = MIN		2			V
$V_{in(0)}$	Logical 0 input voltage required at any input terminal to ensure logical 1 level at output	16	V_{CC} = MIN				0.8	V
$V_{out(1)}$	Logical 1 output voltage	16	V_{CC} = MIN, V_{in} = 0.8 V, I_{load} = −400 μA		2.4	3.3		V
$V_{out(0)}$	Logical 0 output voltage	15	V_{CC} = MIN, V_{in} = 2 V, I_{sink} = 16 mA			0.22	0.4	V
$I_{in(0)}$	Logical 0 level input current (each Logical 0 level input current	17	V_{CC} = MAX, V_{in} = 0.4 V				−1.6	mA
$I_{in(1)}$	Logical 1 level input current	18	V_{CC} = MAX, V_{in} = 2.4 V				40	μA
			V_{CC} = MAX, V_{in} = 5.5 V				1	mA
I_{OS}	Short-circuit output current§	19	V_{CC} = MAX	SN5404	−20		−55	mA
				SN7404	−18		−55	
$I_{CC(0)}$	Logical 0 level supply current	20	V_{CC} = MAX, V_{in} = 5 V			18	33	mA
$I_{CC(1)}$	Logical 1 level supply current	20	V_{CC} = MAX, V_{in} = 0			6	12	mA

switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10

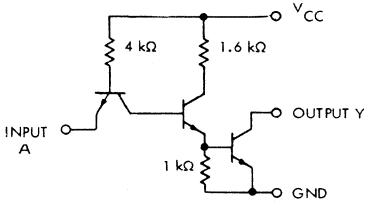
PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{pd0}	Propagation delay time to logical 0 level	65	C_L = 15 pF, R_L = 400 Ω		8	15	ns
t_{pd1}	Propagation delay time to logical 1 level	65	C_L = 15 pF, R_L = 400 Ω		12	22	ns

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ Not more than one output should be shorted at a time.

—SEE ORDERING INSTRUCTIONS PAGE 1-1—

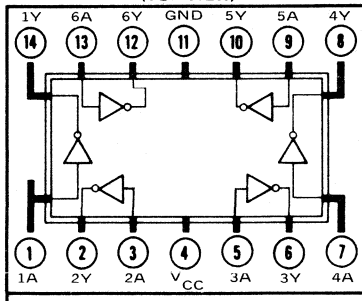
CIRCUIT TYPES SN5405, SN7405
HEX INVERTERS (WITH OPEN-COLLECTOR OUTPUT)

schematic (each inverter)

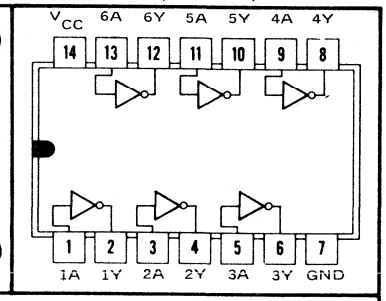


NOTE: Component values shown are nominal.

S FLAT PACKAGE
(TOP VIEW)



J OR N DUAL-IN-LINE PACKAGE
(TOP VIEW)



positive logic $Y = \overline{A}$

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply Voltage V_{CC}: SN5405 Circuits	4.5	5	5.5	V
SN7405 Circuits	4.75	5	5.25	V
Normalized Fan-Out From Each Output, N (and see pages 2-7 and 2-8)			10	
Operating Free-Air Temperature Range, T_A: SN5405 Circuits	−55	25	125	°C
SN7405 Circuits	0	25	70	°C

electrical characteristics (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS†	MIN	TYP‡	MAX	UNIT
$V_{in(1)}$	Logical 1 input voltage required at input terminal to ensure logical 0 (on) level at output	15	V_{CC} = MIN	2			V
$V_{in(0)}$	Logical 0 input voltage required at input terminal to ensure logical 1 (off) level at output	16	V_{CC} = MIN			0.8	V
$I_{out(1)}$	Output reverse current	16	V_{CC} = MIN, V_{in} = 0.8 V, $V_{out(1)}$ = 5.5 V			250	μA
$V_{out(0)}$	Logical 0 output voltage (on level)	15	V_{CC} = MIN, V_{in} = 2 V, I_{sink} = 16 mA			0.4	V
$I_{in(0)}$	Logical 0 level input current	17	V_{CC} = MAX, V_{in} = 0.4 V			−1.6	mA
$I_{in(1)}$	Logical 1 level input current	18	V_{CC} = MAX, V_{in} = 2.4 V			40	μA
			V_{CC} = MAX, V_{in} = 5.5 V			1	mA
$I_{CC(0)}$	Logical 0 level supply current	20	V_{CC} = 5 V, V_{in} = 5 V, T_A = 25°C		18	33	mA
$I_{CC(1)}$	Logical 1 level supply current	20	V_{CC} = 5 V, V_{in} = 0, T_A = 25°C		6	12	mA

switching characteristics, V_{CC} = 5 V, T_A = 25°C

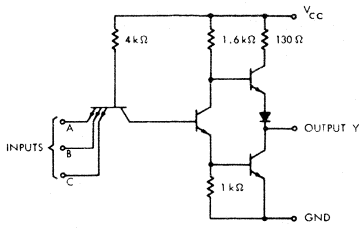
PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{pd0}	Propagation delay time to logical 0 level	65	C_L = 15 pF, R_L = 400 Ω		8	15	ns
t_{pd1}	Propagation delay time to logical 1 level	65	C_L = 15 pF, R_L = 4 kΩ		40	55	ns

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

‡ These typical values are at V_{CC} = 5 V, T_A = 25°C.

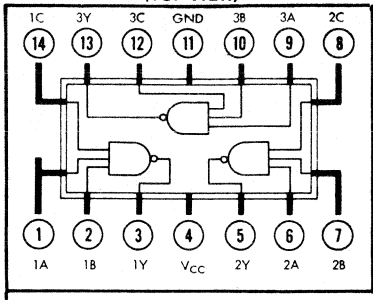
—SEE ORDERING INSTRUCTIONS PAGE 1-1—

schematic (each gate)

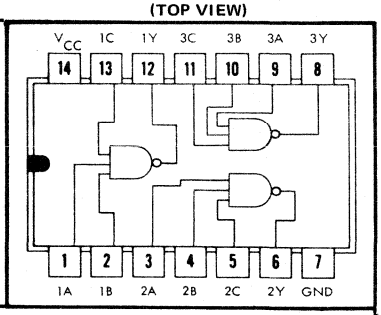


NOTE: Component values shown are nominal.

S FLAT PACKAGE
(TOP VIEW)



J OR N DUAL-IN-LINE PACKAGE
(TOP VIEW)



positive logic: $Y = \overline{ABC}$

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply Voltage V_{CC}:	SN5410 Circuits	4.5	5	5.5	V
	SN7410 Circuits	4.75	5	5.25	V
Normalized Fan-Out From Each Output, N				10	
Operating Free-Air Temperature Range, T_A:	SN5410 Circuits	−55	25	125	°C
	SN7410 Circuits	0	25	70	°C

electrical characteristics (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
$V_{in(1)}$	Logical 1 input voltage required at all input terminals to ensure logical 0 level at output	1	V_{CC} = MIN		2			V
$V_{in(0)}$	Logical 0 input voltage required at any input terminal to ensure logical 1 level at output	2	V_{CC} = MIN				0.8	V
$V_{out(1)}$	Logical 1 output voltage	2	V_{CC} = MIN, V_{in} = 0.8 V, I_{load} = −400 μA		2.4	3.3		V
$V_{out(0)}$	Logical 0 output voltage	1	V_{CC} = MIN, V_{in} = 2 V, I_{sink} = 16 mA			0.22	0.4	V
$I_{in(0)}$	Logical 0 level input current (each input)	3	V_{CC} = MAX, V_{in} = 0.4 V				−1.6	mA
$I_{in(1)}$	Logical 1 level input current (each input)	4	V_{CC} = MAX, V_{in} = 2.4 V				40	μA
			V_{CC} = MAX, V_{in} = 5.5 V				1	mA
I_{OS}	Short circuit output current§	5	V_{CC} = 5.5 V	SN5410	−20		−55	mA
				SN7410	−18		−55	
$I_{CC(0)}$	Logical 0 level supply current	6	V_{CC} = MAX, V_{in} = 5 V			9	16.5	mA
$I_{CC(1)}$	Logical 1 level supply current	6	V_{CC} = MAX, V_{in} = 0			3	6	mA

switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{pd0}	Propagation delay time to logical 0 level	65	C_L = 15 pF, R_L = 400 Ω		7	15	ns
t_{pd1}	Propagation delay time to logical 1 level	65	C_L = 15 pF, R_L = 400 Ω		11	22	ns

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

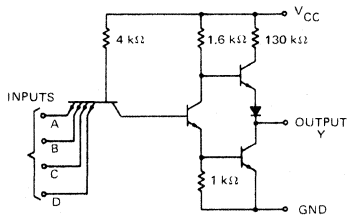
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

§ Not more than one output should be shorted at a time.

—SEE ORDERING INSTRUCTIONS PAGE 1-1—

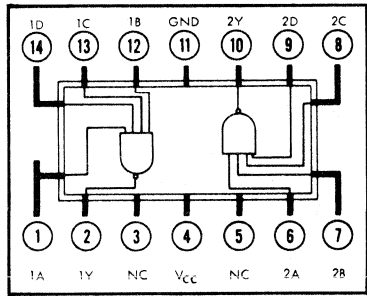
CIRCUIT TYPES SN5420, SN7420
DUAL 4-INPUT POSITIVE NAND GATES

schematic (each gate)

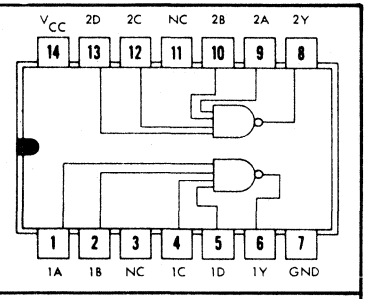


Component values shown are nominal.
NC—No Internal Connection

S FLAT PACKAGE
(TOP VIEW)



J OR N DUAL-IN-LINE PACKAGE
(TOP VIEW)



positive logic: $Y = \overline{ABCD}$

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply Voltage V_{CC}:	SN5420 Circuits	4.5	5	5.5	V
	SN7420 Circuits	4.75	5	5.25	V
Normalized Fan-Out From Each Output, N				10	
Operating Free-Air Temperature Range, T_A:	SN5420 Circuits	−55	25	125	°C
	SN7420 Circuits	0	25	70	°C

electrical characteristics (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
$V_{in(1)}$	Logical 1 input voltage required at all input terminals to ensure logical 0 level at output	1	V_{CC} = MIN		2			V
$V_{in(0)}$	Logical 0 input voltage required at any input terminal to ensure logical 1 level at output	2	V_{CC} = MIN				0.8	V
$V_{out(1)}$	Logical 1 output voltage	2	V_{CC} = MIN, V_{in} = 0.8 V, I_{load} = −400 μA		2.4	3.3		V
$V_{out(0)}$	Logical 0 output voltage	1	V_{CC} = MIN, V_{in} = 2 V, I_{sink} = 16 mA			0.22	0.4	V
$I_{in(0)}$	Logical 0 level input current (each input)	3	V_{CC} = MAX, V_{in} = 0.4 V				−1.6	mA
$I_{in(1)}$	Logical 1 level input current (each input)	4	V_{CC} = MAX, V_{in} = 2.4 V				40	μA
			V_{CC} = MAX, V_{in} = 5.5 V				1	mA
I_{OS}	Short-circuit output current§	5	V_{CC} = MAX	SN5420	−20		−55	mA
				SN7420	−18		−55	
$I_{CC(0)}$	Logical 0 level supply current	6	V_{CC} = MAX, V_{in} = 5 V			6	11	mA
$I_{CC(1)}$	Logical 1 level supply current	6	V_{CC} = MAX, V_{in} = 0			2	4	mA

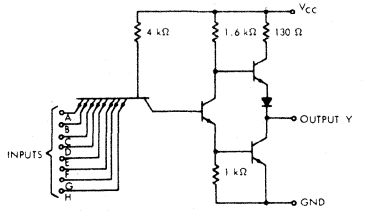
switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{pd0}	Propagation delay time to logical 0 level	65	C_L = 15 pF, R_L = 400 Ω		8	15	ns
t_{pd1}	Propagation delay time to logical 1 level	65	C_L = 15 pF, R_L = 400 Ω		12	22	ns

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ Not more than one output should be shorted at a time.

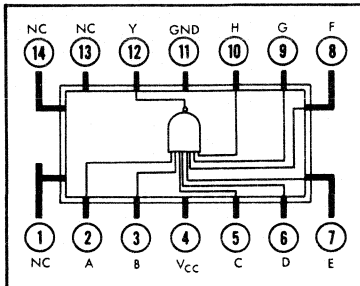
—SEE ORDERING INSTRUCTIONS PAGE 1-1—

schematic

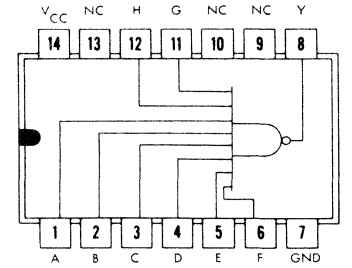


Component values shown are nominal.
NC—No Internal Connection

S FLAT PACKAGE
(TOP VIEW)



J OR N DUAL-IN-LINE PACKAGE
(TOP VIEW)



positive logic: $Y = \overline{ABCDEFGH}$

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply Voltage V_{CC}: SN5430 Circuits	4.5	5	5.5	V
SN7430 Circuits	4.75	5	5.25	V
Normalized Fan-Out From Output, N			10	
Operating Free-Air Temperature Range, T_A: SN5430 Circuits	−55	25	125	°C
SN7430 Circuits	0	25	70	°C

electrical characteristics (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
$V_{in(1)}$	Logical 1 input voltage required at all input terminals to ensure logical 0 level at output	1	V_{CC} = MIN		2			V
$V_{in(0)}$	Logical 0 input voltage required at any input terminal to ensure logical 1 level at output	2	V_{CC} = MIN				0.8	V
$V_{out(1)}$	Logical 1 output voltage	2	V_{CC} = MIN, V_{in} = 0.8 V, I_{load} = −400 μA		2.4	3.3		V
$V_{out(0)}$	Logical 0 output voltage	1	V_{CC} = MIN, V_{in} = 2 V, I_{sink} = 16 mA			0.22	0.4	V
$I_{in(0)}$	Logical 0 level input current (each input)	3	V_{CC} = MAX, V_{in} = 0.4 V				−1.6	mA
$I_{in(1)}$	Logical 1 level input current (each input)	4	V_{CC} = MAX, V_{in} = 2.4 V				40	μA
			V_{CC} = MAX, V_{in} = 5.5 V				1	mA
I_{OS}	Short-circuit output current§	5	V_{CC} = MAX	SN5430	−20		−55	mA
				SN7430	−18		−55	
$I_{CC(0)}$	Logical 0 level supply current	6	V_{CC} = MAX, V_{in} = 5 V			3	6	mA
$I_{CC(1)}$	Logical 1 level supply current	6	V_{CC} = MAX, V_{in} = 0			1	2	mA

switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10

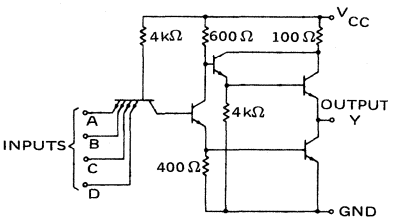
PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{pd0}	Propagation delay time to logical 0 level	65	C_L = 15 pF, R_L = 400 Ω		8	15	ns
t_{pd1}	Propagation delay time to logical 1 level	65	C_L = 15 pF, R_L = 400 Ω		13	22	ns

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ Not more than one output should be shorted at a time.

—SEE ORDERING INSTRUCTIONS PAGE 1-1—

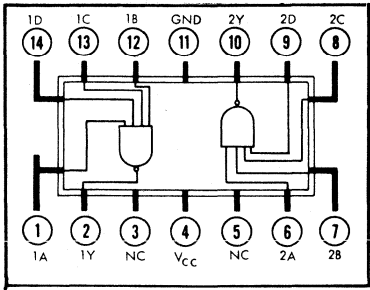
CIRCUIT TYPES SN5440, SN7440
DUAL 4-INPUT POSITIVE NAND BUFFERS

schematic (each gate)

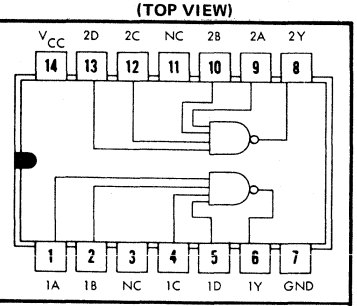


Component values shown are nominal.
NC—No Internal Connection

S FLAT PACKAGE
(TOP VIEW)



J OR N DUAL-IN-LINE PACKAGE
(TOP VIEW)



positive logic: $Y = \overline{ABCD}$

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply Voltage V_{CC}:	SN5440 Circuits	4.5	5	5.5	V
	SN7440 Circuits	4.75	5	5.25	V
Normalized Fan-Out From Output, N				10	
Operating Free-Air Temperature Range, T_A:	SN5440 Circuits	−55	25	125	°C
	SN7440 Circuits	0	25	70	°C

electrical characteristics (over recommended free-air temperature range unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
$V_{in(1)}$	Logical 1 input voltage required at all input terminals to ensure logical 0 level at output	1	V_{CC} = MIN		2			V
$V_{in(0)}$	Logical 0 input voltage required at any input terminal to ensure logical 1 level at output	2	V_{CC} = MIN				0.8	V
$V_{out(1)}$	Logical 1 output voltage	2	V_{CC} = MIN, V_{in} = 0.8 V, I_{load} = −1.2 mA		2.4	3.3		V
$V_{out(0)}$	Logical 0 output voltage	1	V_{CC} = MIN, V_{in} = 2 V, I_{sink} = 48 mA			0.28	0.4	V
$I_{in(0)}$	Logical 0 level input current (each input)	3	V_{CC} = MAX, V_{in} = 0.4 V				−1.6	mA
$I_{in(1)}$	Logical 1 level input current (each input)	4	V_{CC} = MAX, V_{in} = 2.4 V				40	μA
			V_{CC} = MAX, V_{in} = 5.5 V				1	mA
I_{OS}	Short-circuit output current §	5	V_{CC} = MAX	SN5440	−20		−70	mA
				SN7440	−18		−70	mA
$I_{CC(0)}$	Logical 0 level supply current	6	V_{CC} = MAX, V_{in} = 5 V			17	27	mA
$I_{CC(1)}$	Logical 1 level supply current	6	V_{CC} = MAX, V_{in} = 0			2	4	mA

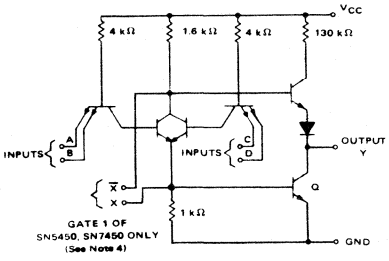
switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 30

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{pd0}	Propagation delay time to logical 0 level	65	C_L = 15 pF, R_L = 133 Ω		8	15	ns
t_{pd1}	Propagation delay time to logical 1 level	65	C_L = 15 pF, R_L = 133 Ω		13	22	ns

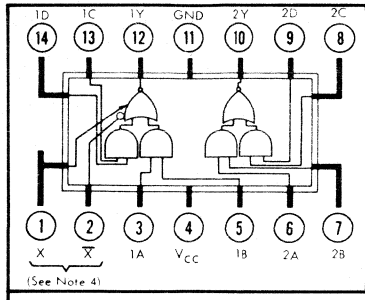
†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time.

—SEE ORDERING INSTRUCTIONS PAGE 1-1—

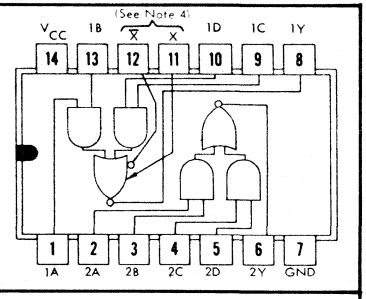
schematic (each gate)



S FLAT PACKAGE
(TOP VIEW)



J OR N DUAL-IN-LINE PACKAGE
(TOP VIEW)



positive logic: $Y = \overline{(AB) + (CD) + (X)}$
X = Output of SN5460/SN7460

NOTES: 1. Component values shown are nominal.
2. Both expander inputs are used simultaneously for expanding.
3. If expander is not used leave X and $\overline{X}$ pins open.
4. Make no external connection to X and $\overline{X}$ pins of the SN5451 and SN7451.
5. A total of four expander gates can be connected to the expander inputs.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply Voltage V_{CC}: SN5450, SN5451 Circuits	4.5	5	5.5	V
SN7450, SN7451 Circuits	4.75	5	5.25	V
Normalized Fan-Out From Each Output, N			10	
Operating Free-Air Temperature Range, T_A: SN5450, SN5451 Circuits	−55	25	125	°C
SN7450, SN7451 Circuits	0	25	70	°C

electrical characteristics (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
$V_{in(1)}$	Logical 1 input voltage required at both input terminals of either AND section to ensure logical 0 at output	21	V_{CC} = MIN		2			V
$V_{in(0)}$	Logical 0 input voltage required at one input terminal of each AND section to ensure logical 1 at output	22	V_{CC} = MIN				0.8	V
$V_{out(1)}$	Logical 1 output voltage	22	V_{CC} = MIN, V_{in} = 0.8 V, I_{load} = −400 μA		2.4	3.3		V
$V_{out(0)}$	Logical 0 output voltage	21	V_{CC} = MIN, V_{in} = 2 V, I_{sink} = 16 mA			0.22	0.4	V
$I_{in(0)}$	Logical 0 level input current (each input)	23	V_{CC} = MAX, V_{in} = 0.4 V				−1.6	mA
$I_{in(1)}$	Logical 1 level input current (each input)	24	V_{CC} = MAX, V_{in} = 2.4 V				40	μA
			V_{CC} = MAX, V_{in} = 5.5 V				1	mA
I_{OS}	Short-circuit output current§	25	V_{CC} = MAX	SN5450, SN5451	−20		−55	mA
				SN7450, SN7451	−18		−55	
$I_{CC(0)}$	Logical 0 level supply current	26	V_{CC} = MAX, V_{in} = 5 V			7.4	14	mA
$I_{CC(1)}$	Logical 1 level supply current	27	V_{CC} = MAX, V_{in} = 0			4	8	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type. Expander inputs X and $\overline{X}$ are open.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ Not more than one output should be shorted at a time.

—SEE ORDERING INSTRUCTIONS PAGE 1-1—

electrical characteristics (SN5450 circuits) using expander inputs, V_{CC} = 4.5 V, T_A = –55°C

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP‡	MAX	UNIT
I_X	Expander current	28	V_1 = 0.4 V, I_{sink} = 16 mA			2.9	mA
$V_{BE(Q)}$	Base-emitter voltage of output transistor (Q)	29	I_{sink} = 16 mA, I_1 = 0.41 mA, R_1 = 0			1	V
$V_{out(1)}$	Logical 1 output voltage	30	I_{load} = –400 μA, I_1 = 0.15 mA, I_2 = –0.15 mA	2.4	3.3		V
$V_{out(0)}$	Logical 0 output voltage	29	I_{sink} = 16 mA, I_1 = 0.3 mA, R_1 = 138 Ω		0.22	0.4	V

electrical characteristics (SN7450 circuits) using expander inputs, V_{CC} = 4.75 V, T_A = 0°C

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP‡	MAX	UNIT
I_X	Expander current	28	V_1 = 0.4 V, I_{sink} = 16 mA			3.1	mA
$V_{BE(Q)}$	Base-emitter voltage of output transistor (Q)	29	I_{sink} = 16 mA, I_1 = 0.62 mA, R_1 = 0			1	V
$V_{out(1)}$	Logical 1 output voltage	30	I_{load} = –400 μA, I_1 = 270 μA, I_2 = –270 μA	2.4	3.3		V
$V_{out(0)}$	Logical 0 output voltage	29	I_{sink} = 16 mA, I_1 = 0.43 mA, R_1 = 130 Ω		0.22	0.4	V

switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10

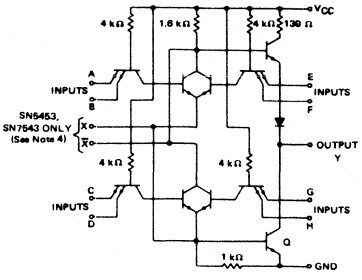
PARAMETER		TEST FIGURE	TEST CONDITIONS†	MIN	TYP	MAX	UNIT
t_{pd0}	Propagation delay time to logical 0 level	65	C_L = 15 pF, R_L = 400 Ω		8	15	ns
t_{pd1}	Propagation delay time to logical 1 level	65	C_L = 15 pF, R_L = 400 Ω		13	22	ns

†Expander pins X and $\overline{X}$ are open.

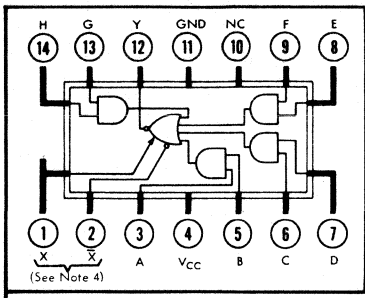
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

–SEE ORDERING INSTRUCTIONS PAGE 1-1–

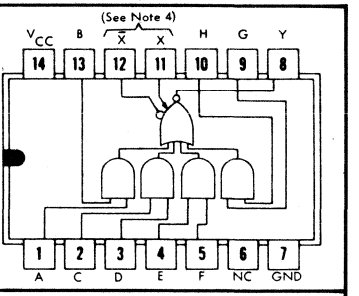
schematic



S FLAT PACKAGE
(TOP VIEW)



J OR N DUAL-IN-LINE PACKAGE
(TOP VIEW)



positive logic: $Y = \overline{(AB) + (CD) + (EF) + (GH) + (X)}$
X = Output of SN5460/SN7460

NOTES:
1. Component values shown are nominal.
2. Both expander inputs are used simultaneously for expanding.
3. If expander is not used leave X and $\overline{X}$ pins open.
4. Make no external connection to X and $\overline{X}$ pins of the SN5454 and SN7454.
5. A total of four expander gates can be connected to the expander inputs.
6. NC—No Internal Connection

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply Voltage V_{CC}: SN5453, SN5454 Circuits	4.5	5	5.5	V
SN7453, SN7454 Circuits	4.75	5	5.25	V
Normalized Fan-Out From Output, N			10	
Operating Free-Air Temperature Range, T_A: SN5453, SN5454 Circuits	−55	25	125	°C
SN7453, SN7454 Circuits	0	25	70	°C

electrical characteristics (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
$V_{in(1)}$	Logical 1 input voltage required at both input terminals of one AND section to ensure logical 0 level at output	21	V_{CC} = MIN		2			V
$V_{in(0)}$	Logical 0 input voltage required at one input terminal of each AND section to ensure logical 1 level at output	22	V_{CC} = MIN				0.8	V
$V_{out(1)}$	Logical 1 output voltage	22	V_{CC} = MIN, V_{in} = 0.8 V, I_{load} = −400 μA		2.4	3.3		V
$V_{out(0)}$	Logical 0 output voltage	21	V_{CC} = MIN, V_{in} = 2 V, I_{sink} = 16 mA			0.22	0.4	V
$I_{in(0)}$	Logical 0 level input current (each input)	23	V_{CC} = MAX, V_{in} = 0.4 V				−1.6	mA
$I_{in(1)}$	Logical 1 level input current (each input)	24	V_{CC} = MAX, V_{in} = 2.4 V				40	μA
			V_{CC} = MAX, V_{in} = 5.5 V				1	mA
I_{OS}	Short-circuit output current§	25	V_{CC} = 5.5 V	SN5453, SN5454	−20		−55	mA
				SN7453, SN7454	−18		−55	
$I_{CC(0)}$	Logical 0 level supply current	26	V_{CC} = MAX, V_{in} = 5 V			5.1	9.5	mA
$I_{CC(1)}$	Logical 1 level supply current	27	V_{CC} = MAX, V_{in} = 0			4	8	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type. Expander inputs X and $\overline{X}$ are open.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ Not more than one output should be shorted at a time.

—SEE ORDERING INSTRUCTIONS PAGE 1-1—

electrical characteristics (SN5453 circuits) using expander inputs, V_{CC} = 4.5 V, T_A = –55°C

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP‡	MAX	UNIT
I_X	Expander current	28	V_1 = 0.4 V, I_{sink} = 16 mA			2.9	mA
$V_{BE(Q)}$	Base-emitter voltage of output transistor (Q)	29	I_{sink} = 16 mA, I_1 = 0.41 mA, R_1 = 0			1	V
$V_{out(1)}$	Logical 1 output voltage	30	I_{load} = –400 μA, I_1 = 0.15 mA, I_2 = –0.15 mA	2.4	3.3		V
$V_{out(0)}$	Logical 0 output voltage	29	I_{sink} = 16 mA, I_1 = 0.3 mA, R_1 = 138 Ω		0.22	0.4	V

electrical characteristics (SN7473 circuits) using expander inputs, V_{CC} = 4.75 V, T_A = 0°C

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP‡	MAX	UNIT
I_X	Expander current	28	V_1 = 0.4 V, I_{sink} = 16 mA			3.1	mA
$V_{BE(Q)}$	Base-emitter voltage of output transistor (Q)	29	I_{sink} = 16 mA, I_1 = 0.62 mA, R_1 = 0			1	V
$V_{out(1)}$	Logical 1 output voltage	30	I_{load} = –400 μA, I_1 = 270 μA, I_2 = –270 μA	2.4	3.3		V
$V_{out(0)}$	Logical 0 output voltage	29	I_{sink} = 16 mA, I_1 = 0.43 mA, R_1 = 130 Ω		0.22	0.4	V

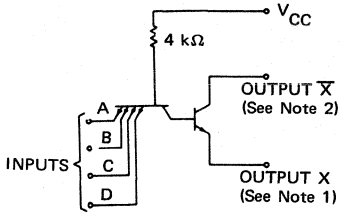
switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10

PARAMETER		TEST FIGURE	TEST CONDITIONS†	MIN	TYP	MAX	UNIT
t_{pd0}	Propagation delay time to logical 0 level	65	C_L = 15 pF, R_L = 400 Ω		8	15	ns
t_{pd1}	Propagation delay time to logical 1 level	65	C_L = 15 pF, R_L = 400 Ω		13	22	ns

† Expander inputs X and $\overline{X}$ are open.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

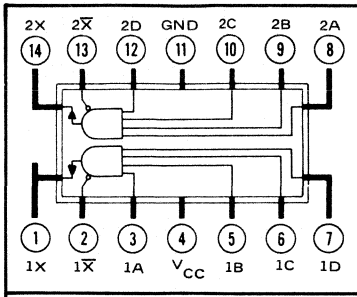
–SEE ORDERING INSTRUCTIONS PAGE 1-1–

schematic (each expander)

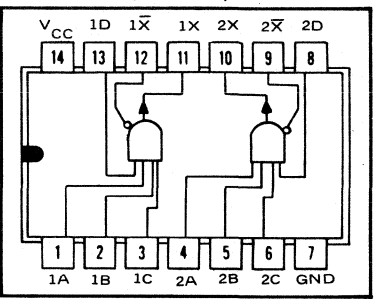


NOTES: 1. Connect to X input of SN5450 or SN5453 circuit.
2. Connect to $\overline{X}$ input of SN5450 or SN5453 circuit.
3. Component values shown are nominal.

S FLAT PACKAGE
(TOP VIEW)



J OR N DUAL-IN-LINE PACKAGE
(TOP VIEW)



positive logic: X=ABCD
when connected to X and $\overline{X}$ pins of SN5450 or SN5453 circuit.

recommended operating conditions

Supply Voltage V_{CC} . . . . . 4.5 V to 5.5 V
Maximum number of expanders that may be fanned-in to one SN5450 or one SN5453 circuit 4

electrical characteristics (unless otherwise noted T_A = −55°C to 125°C)

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP‡	MAX	UNIT
$V_{in(1)}$	Logical 1 input voltage required at all input terminals to ensure output is in the on state	31	V_{CC} = 4.5 V	2			V
$V_{in(0)}$	Logical 0 input voltage required at any input terminal to ensure output is in the off state	32	V_{CC} = 4.5 V			0.8	V
V_{on}	On-state output voltage	31	V_{CC} = 4.5 V, V_{in} = 2 V, V_1 = 1 V, R = 1.1 kΩ, T_A = −55°C			0.4	V
I_{off}	Off-state output current	32	V_{CC} = 4.5 V, V_{in} = 0.8 V, V_1 = 4.5 V, R = 1.2 kΩ, T_A = −55°C			150	μA
I_{on}	On-state output current	33	V_{CC} = 4.5 V, V_{in} = 2 V, V_1 = 1 V, T_A = −55°C	−0.7			mA
$I_{in(0)}$	Logical 0 level input current (each input)	32	V_{CC} = 5.5 V, V_{in} = 0.4 V			−1.6	mA
$I_{in(1)}$	Logical 1 level input current (each input)	34	V_{CC} = 5.5 V, V_{in} = 2.4 V			40	μA
			V_{CC} = 5.5 V, V_{in} = 5.5 V			1	mA
$I_{CC(on)}$	On-state supply current	35	V_{CC} = 5.5 V, V_{in} = 5 V, V_1 = 0.85 V		1.2	2.5	mA
$I_{CC(off)}$	Off-state supply current	35	V_{CC} = 5.5 V, V_{in} = 0, V_1 = 0.85 V		2	4	mA

switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10

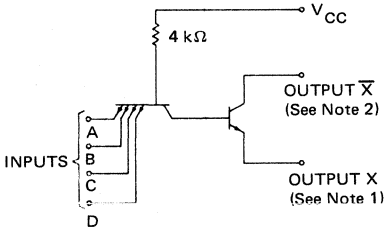
PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{pd0}	Propagation delay time to logical 0 level (through SN5450 or SN5453 circuit)	66	C_L = 15 pF, R_L = 400 Ω		10	20	ns
t_{pd1}	Propagation delay time to logical 1 level (through SN5450 or SN5453 circuit)	66	C_L = 15 pF, R_L = 400 Ω		15	30	ns

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

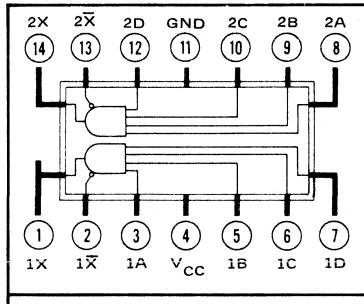
—SEE ORDERING INSTRUCTIONS PAGE 1-1—

CIRCUIT TYPE SN7460
DUAL 4-INPUT EXPANDER

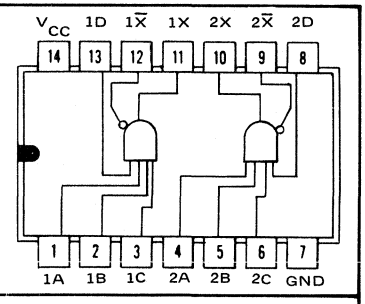
schematic (each expander)



S FLAT PACKAGE
(TOP VIEW)



J OR N DUAL-IN-LINE PACKAGE
(TOP VIEW)



positive logic: X=ABCD
when connected to X and $\overline{X}$ pins of SN7450 or SN7453 circuit.

NOTES: 1. Connect to X input of SN7450 or SN7453 circuit.
2. Connect to $\overline{X}$ input of SN7450 or SN7453 circuit.
3. Component values shown are nominal.

recommended operating conditions

Supply Voltage V_{CC} . . . . . 4.75 V to 5.25 V
Maximum number of expanders that may be fanned-in to one SN7450 or one SN7453 Circuit 4

electrical characteristics (unless otherwise noted T_A = 0°C to 70°C)

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP‡	MAX	UNIT
$V_{in(1)}$	Logical 1 input voltage required at all input terminals is in the on state	31	V_{CC} = 4.75 V	2			V
$V_{in(0)}$	Logical 0 input voltage required at any input terminal is in the off state	32	V_{CC} = 4.75 V			0.8	V
V_{on}	On-state output voltage	31	V_{CC} = 4.75 V, V_{in} = 2 V, V_1 = 1 V, R = 1.1 kΩ, T_A = 0°C			0.4	V
I_{off}	Off-state output current	32	V_{CC} = 4.75 V, V_{in} = 0.8 V, V_1 = 4.5 V, R = 1.2 kΩ T_A = 0°C			270	μA
I_{on}	On-state output current	33	V_{CC} = 4.75 V, V_{in} = 2 V, V_1 = 1 V	−0.43			mA
$I_{in(0)}$	Logical 0 level input current (each input)	32	V_{CC} = 5.25 V, V_{in} = 0.4 V			−1.6	mA
$I_{in(1)}$	Logical 1 level input current (each input)	34	V_{CC} = 5.25 V, V_{in} = 2.4 V			40	μA
			V_{CC} = 5.25 V, V_{in} = 5.5 V			1	mA
$I_{CC(on)}$	On-state supply current	35	V_{CC} = 5.25 V, V_{in} = 5 V, V_1 = 0.85 V		1.2	2.5	mA
$I_{CC(off)}$	Off-state supply current	35	V_{CC} = 5.25 V, V_{in} = 0, V_1 = 0.85 V		2	4	mA

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{pd0}	Propagation delay time to logical 0 level (through SN7450 or SN7453)	66	C_L = 15 pF, R_L = 400 Ω		10	20	ns
t_{pd1}	Propagation delay time to logical 1 level (through SN7450 or SN7453)	66	C_L = 15 pF, R_L = 400 Ω		15	30	ns

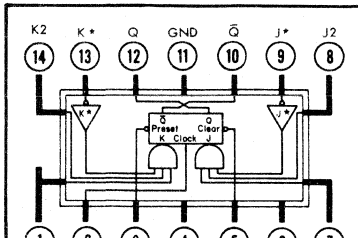
— SEE ORDERING INSTRUCTIONS PAGE 1-1 —

logic

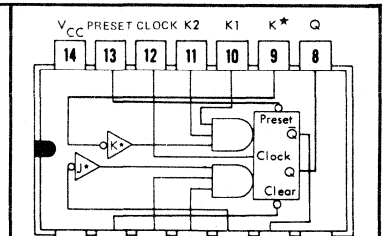
TRUTH TABLE		
t_n		t_{n+1}
J	K	Q
0	0	Q_n
0	1	0
1	0	1
1	1	$\overline{Q}_n$

NOTES: 1. $J = J1 \cdot J2 \cdot \overline{J^*}$
2. $K = K1 \cdot K2 \cdot \overline{K^*}$.
3. t_n = Bit time before clock pulse.
4. t_{n+1} = Bit time after clock pulse.
5. If inputs J* or K* are not used they must be grounded.
6. NC - No Internal Connection

S FLAT PACKAGE
(TOP VIEW)



J OR N DUAL-IN-LINE PACKAGE
(TOP VIEW)



positive logic: Low input to preset sets Q to logical 1
Low input to clear sets Q to logical 0
Preset or clear function can occur only when clock input is low.

description

These monolithic, edge-triggered J-K flip-flops feature gated inputs, direct clear and preset inputs, and complementary Q and $\overline{Q}$ outputs. Input information is transferred to the outputs on the positive edge of the clock pulse.

Direct-coupled clock triggering occurs at a specific voltage level of the clock pulse, and after the clock input threshold voltage has been passed, the gated inputs are locked out.

These flip-flops are ideally suited for medium- to high-speed applications and can result in a significant saving in system power dissipation and package count where input gating is required.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply Voltage V_{CC}: SN5470 Circuits	4.5	5	5.5	V
SN7470 Circuits	4.75	5	5.25	V
Operating Free-Air Temperature Range, T_A: SN5470 Circuits	−55	25	125	°C
SN7470 Circuits	0	25	70	°C
Normalized Fan-Out From Each Output, N			10	
Clock Pulse Transition Time to Logical 1 Level, $t_{1(clock)}$ (See Figure 68)			150	ns
Width of Clock Pulse, $t_{p(clock)}$ (See Figure 68)	20			ns
Width of Preset Pulse, $t_{p(preset)}$ (See Figure 67)	25			ns
Width of Clear Pulse, $t_{p(clear)}$ (See Figure 67)	25			ns

—SEE ORDERING INSTRUCTIONS PAGE 1-1—

electrical characteristics (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS†			MIN	TYP‡	MAX	UNIT
$V_{in(1)}$	Input voltage required to ensure logical 1 at any input terminal	36 and 37	V_{CC} = MIN			2			V
$V_{in(0)}$	Input voltage required to ensure logical 0 at any input terminal	36 and 37	V_{CC} = MIN					0.8	V
$V_{out(1)}$	Logical 1 output voltage	36	V_{CC} = MIN,	I_{load} = −400 μA		2.4	3.5		V
$V_{out(0)}$	Logical 0 output voltage	37	V_{CC} = MIN,	I_{sink} = 16 mA			0.22	0.4	V
$I_{in(0)}$	Logical 0 level input current at J1, J2, J*, J1, K2, K*, or clock	38	V_{CC} = MAX,	V_{in} = 0.4 V				−1.6	mA
$I_{in(0)}$	Logical 0 level input current at preset or clear	38	V_{CC} = MAX,	V_{in} = 0.4 V				−3.2	mA
$I_{in(1)}$	Logical 1 level input current at J1, J2, J*, K1, K2, K*, or clock	39	V_{CC} = MAX,	V_{in} = 2.4 V				40	μA
			V_{CC} = MAX,	V_{in} = 5.5 V				1	mA
$I_{in(1)}$	Logical 1 level input current at preset or clear	39	V_{CC} = MAX,	V_{in} = 2.4 V				80	μA
			V_{CC} = MAX,	V_{in} = 5.5 V				1	mA
I_{OS}	Short-circuit output current§	40	V_{CC} = MAX,	V_{in} = 0	SN5470	−20		−57	mA
					SN7470	−18		−57	
I_{CC}	Supply current	39	V_{CC} = MAX,	V_{in} = 5 V			13	26	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

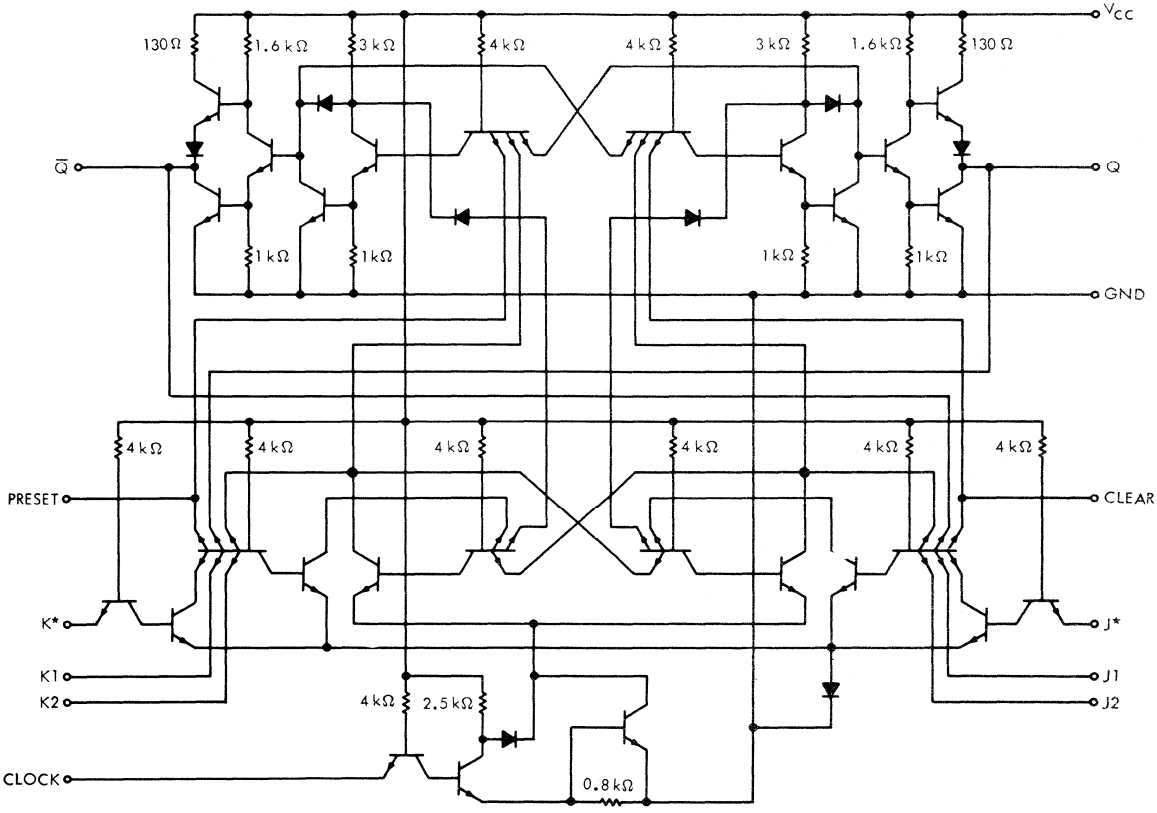
§ Not more than one output should be shorted at a time.

switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10

PARAMETER		TEST FIGURE	TEST CONDITIONS		MIN	TYP	MAX	UNIT
f_{clock}	Maximum clock frequency	68	C_L = 15 pF,	R_L = 400 Ω	20	35		MHz
t_{setup}	Minimum input setup time	68	C_L = 15 pF,	R_L = 400 Ω		10	20	ns
t_{hold}	Minimum input hold time	68	C_L = 15 pF,	R_L = 400 Ω		0	5	ns
t_{pd1}	Propagation delay time to logical 1 level from clear or preset to output	67	C_L = 15 pF,	R_L = 400 Ω			50	ns
t_{pd0}	Propagation delay time to logical 0 level from clear or preset to output	67	C_L = 15 pF,	R_L = 400 Ω			50	ns
t_{pd1}	Propagation delay time to logical 1 level from clock to output	68	C_L = 15 pF,	R_L = 400 Ω	10	27	50	ns
t_{pd0}	Propagation delay time to logical 0 level from clock to output	68	C_L = 15 pF,	R_L = 400 Ω	10	18	50	ns

—SEE ORDERING INSTRUCTIONS PAGE 1-1—

schematic



NOTE: Component values shown are nominal.

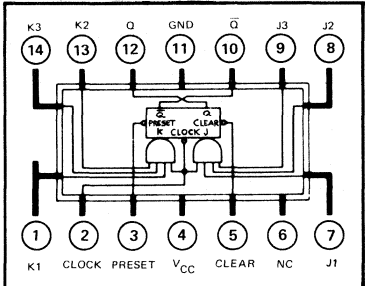
CIRCUIT TYPES SN5472, SN7472
J-K MASTER-SLAVE FLIP-FLOPS

logic

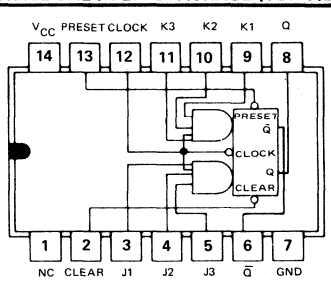
TRUTH TABLE		
t_n		t_{n+1}
J	K	Q
0	0	Q_n
0	1	0
1	0	1
1	1	$\overline{Q}_n$

NOTES: 1. J = J1 • J2 • J3
2. K = K1 • K2 • K3
3. t_n = Bit time before clock pulse.
4. t_{n+1} = Bit time after clock pulse.
5. NC = No Internal Connection.

S FLAT PACKAGE (TOP VIEW)



J OR N DUAL-IN-LINE PACKAGE (TOP VIEW)

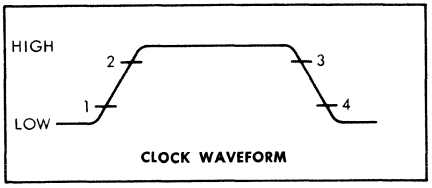


positive logic: Low input to preset sets Q to logical 1
Low input to clear sets Q to logical 0
Preset and clear are independent of clock

description

These J-K flip-flops are based on the master-slave principle and each has AND gate inputs for entry into the master section which are controlled by the clock pulse. The clock pulse also regulates the state of the coupling transistors which connect the master and slave sections. The sequence of operation is as follows:

1. Isolate slave from master
2. Enter information from AND gate inputs to master
3. Disable AND gate inputs
4. Transfer information from master to slave.



CLOCK WAVEFORM

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply Voltage V_{CC}: SN5472 Circuits	4.5	5	5.5	V
SN7472 Circuits	4.75	5	5.25	V
Operating Free-Air Temperature Range, T_A: SN5472 Circuits	−55	25	125	°C
SN7472 Circuits	0	25	70	°C
Normalized Fan-Out From Each Output, N			10	
Width of Clock Pulse, $t_{p(clock)}$ (See figure 69)	20			ns
Width of Preset Pulse, $t_{p(preset)}$ (See figure 70)	25			ns
Width of Clear Pulse, $t_{p(clear)}$ (See figure 70)	25			ns
Input Setup Time, t_{setup} (See figure 69)	$\geq t_{p(clock)}$			
Input Hold Time, t_{hold}	0			

—SEE ORDERING INSTRUCTIONS PAGE 1-1—

electrical characteristics (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
$V_{in(1)}$	Input voltage required to ensure logical 1 at any input terminal	41 and 42	V_{CC} = MIN		2			V
$V_{in(0)}$	Input voltage required to ensure logical 0 at any input terminal	41 and 42	V_{CC} = MIN				0.8	V
$V_{out(1)}$	Logical 1 output voltage	41	V_{CC} = MIN, I_{load} = −400 μA		2.4	3.5		V
$V_{out(0)}$	Logical 0 output voltage	42	V_{CC} = MIN, I_{sink} = 16 mA			0.22	0.4	V
$I_{in(0)}$	Logical 0 level input current at J1, J2, J3, K1, K2, or K3	43	V_{CC} = MAX, V_{in} = 0.4 V				−1.6	mA
$I_{in(0)}$	Logical 0 level input current at preset, clear, or clock	43	V_{CC} = MAX, V_{in} = 0.4 V				−3.2	mA
$I_{in(1)}$	Logical 1 level input current at J1, J2, J3, K1, K2, or K3	44	V_{CC} = MAX, V_{in} = 2.4 V				40	μA
			V_{CC} = MAX, V_{in} = 5.5 V				1	mA
$I_{in(1)}$	Logical 1 level input current at preset, clear, or clock	44	V_{CC} = MAX, V_{in} = 2.4 V				80	μA
			V_{CC} = MAX, V_{in} = 5.5 V				1	mA
I_{OS}	Short-circuit output current§	45	V_{CC} = MAX, V_{in} = 0	SN5472	−20		−57	mA
				SN7472	−18		−57	
I_{CC}	Supply current	44	V_{CC} = MAX, V_{in} = 5 V			10	20	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

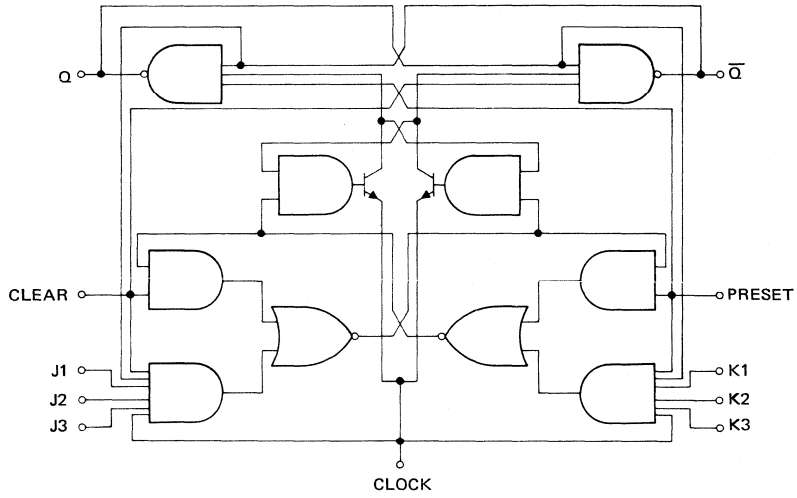
§ Not more than one output should be shorted at a time.

switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10

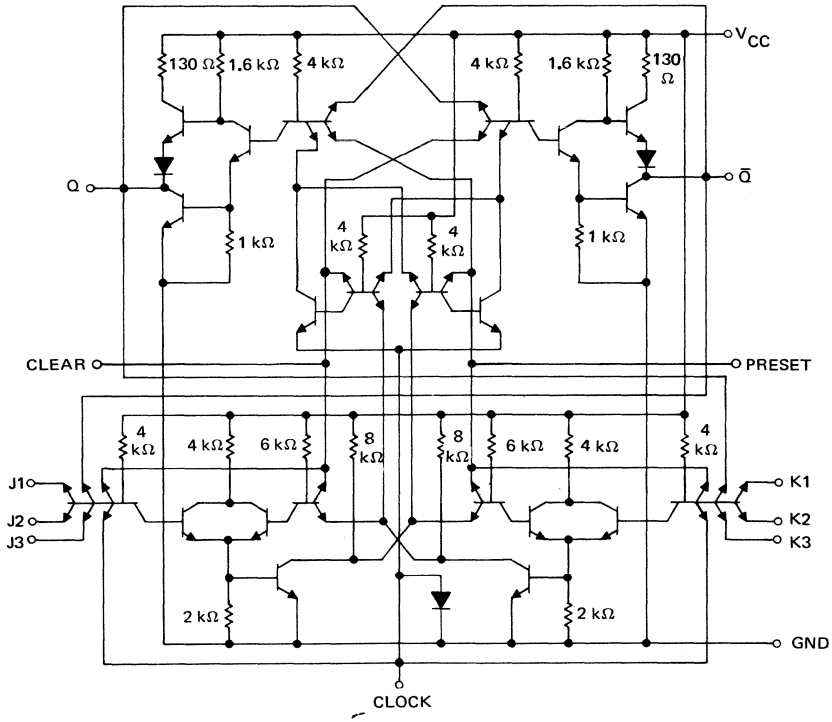
PARAMETER		TEST FIGURE	TEST CONDITIONS		MIN	TYP	MAX	UNIT
f_{clock}	Maximum clock frequency	69	C_L = 15 pF, R_L = 400 Ω		15	20		MHz
t_{pd1}	Propagation delay time to logical 1 level from clear or preset to output	70	C_L = 15 pF, R_L = 400 Ω			16	25	ns
t_{pd0}	Propagation delay time to logical 0 level from clear or preset to output	70	C_L = 15 pF, R_L = 400 Ω			25	40	ns
t_{pd1}	Propagation delay time to logical 1 level from clock to output	69	C_L = 15 pF, R_L = 400 Ω		10	16	25	ns
t_{pd0}	Propagation delay time to logical 0 level from clock to output	69	C_L = 15 pF, R_L = 400 Ω		10	25	40	ns

—SEE ORDERING INSTRUCTIONS PAGE 1-1—

functional block diagram

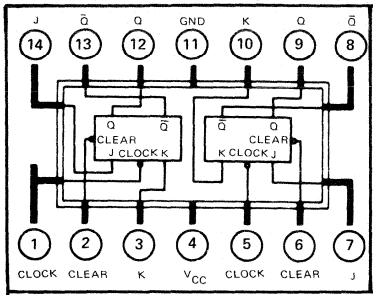


schematic

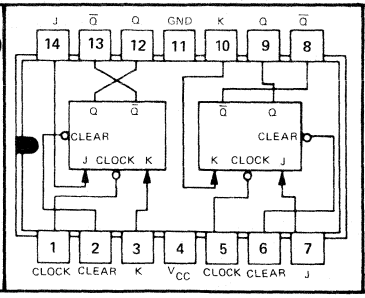


NOTES: Component values shown are nominal.

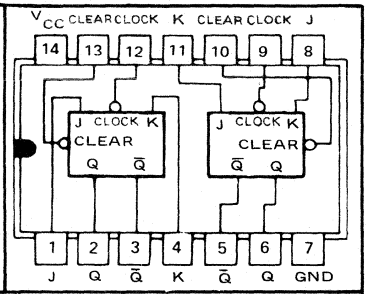
SN5473, SN7473
S FLAT PACKAGE
(TOP VIEW)



SN5473, SN7473
J OR N DUAL-IN-LINE PACKAGE
(TOP VIEW)



SN54107, SN74107
J OR N DUAL-IN-LINE PACKAGE
(TOP VIEW)



positive logic: Low input to clear sets Q to logical 0.
Clear is independent of clock.

description

These J-K flip-flops are based on the master-slave principle. Inputs to the master section are controlled by the clock pulse. The clock pulse also regulates the state of the coupling transistors which connect the master and slave sections. The sequence of operation is as follows: (See waveform on page 2-26)

1. Isolate slave from master
2. Enter information from J and K inputs to master
3. Disable J and K inputs
4. Transfer information from master to slave.

logic

TRUTH TABLE (Each Flip-Flop)		
t_n		t_{n+1}
J	K	Q
0	0	Q_n
0	1	0
1	0	1
1	1	$\bar{Q}_n$

NOTES: 1. t_n = Bit time before clock pulse.
2. t_{n+1} = Bit time after clock pulse.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply Voltage V_{CC}: SN5473, SN54107 Circuits	4.5	5	5.5	V
SN7473, SN74107 Circuits	4.75	5	5.25	V
Operating Free-Air Temperature Range, T_A: SN5473, SN54107 Circuits	−55	25	125	°C
SN7473, SN74107 Circuits	0	25	70	°C
Normalized Fan-Out From Each Output, N			10	
Width of Clock Pulse, $t_{p(clock)}$ (See Figure 69)	20			ns
Width of Clear Pulse, $t_{p(clear)}$ (See Figure 70)	25			ns
Input Setup Time, t_{setup} (See Figure 69)	$\geq t_{p(clock)}$			
Input Hold Time, t_{hold}	0			

—SEE ORDERING INSTRUCTIONS PAGE 1-1—

electrical characteristics (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS†			MIN	TYP‡	MAX	UNIT
$V_{in(1)}$	Input voltage required to ensure logical 1 at any input terminal	46 and 47	V_{CC} = MIN			2			V
$V_{in(0)}$	Input voltage required to ensure logical 0 at any input terminal	46 and 47	V_{CC} = MIN					0.8	V
$V_{out(1)}$	Logical 1 output voltage	46	V_{CC} = MIN,	I_{load} = −400 μA		2.4	3.5		V
$V_{out(0)}$	Logical 0 output voltage	47	V_{CC} = MIN,	I_{sink} = 16 mA			0.22	0.4	V
$I_{in(0)}$	Logical 0 level input current at J or K	48	V_{CC} = MAX,	V_{in} = 0.4 V				−1.6	mA
$I_{in(0)}$	Logical 0 level input current at clear or clock	48	V_{CC} = MAX,	V_{in} = 0.4 V				−3.2	mA
$I_{in(1)}$	Logical 1 level input current at J or K	49	V_{CC} = MAX,	V_{in} = 2.4 V				40	μA
			V_{CC} = MAX,	V_{in} = 5.5 V				1	mA
$I_{in(1)}$	Logical 1 level input current at clear or clock	49	V_{CC} = MAX,	V_{in} = 2.4 V				80	μA
			V_{CC} = MAX,	V_{in} = 5.5 V				1	mA
I_{OS}	Short-circuit output current§	50	V_{CC} = MAX,	V_{in} = 0	SN5473, SN54107	−20		−57	mA
					SN7473, SN74107	−18		−57	
I_{CC}	Supply current	49	V_{CC} = MAX,	V_{in} = 5 V			20	40	mA

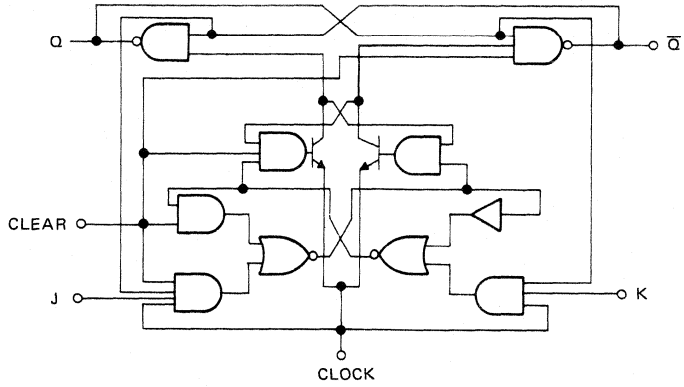
† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ Not more than one output should be shorted at a time.

switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10

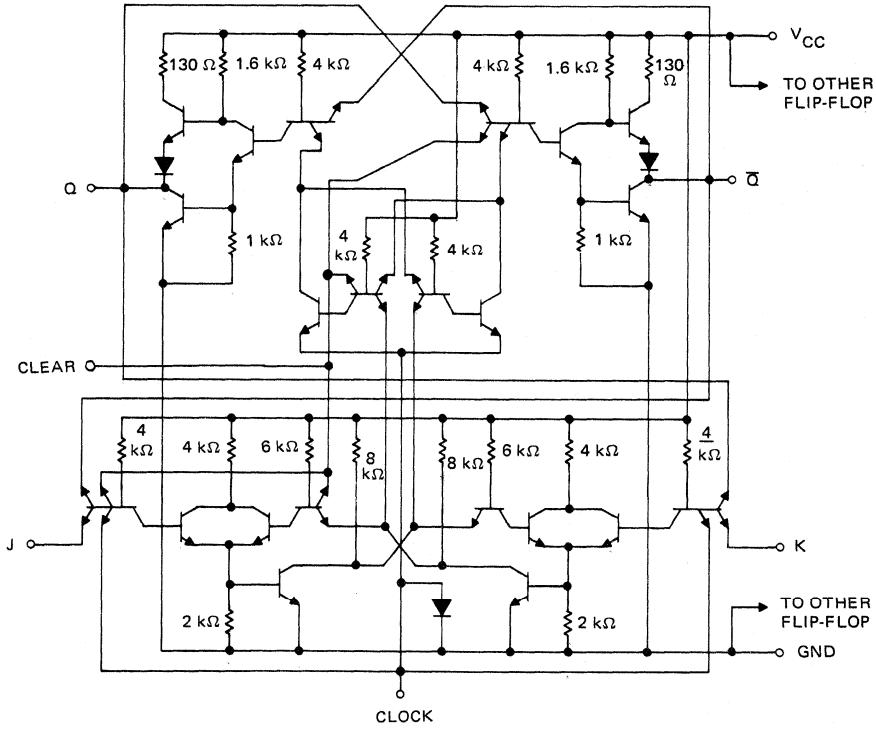
PARAMETER		TEST FIGURE	TEST CONDITIONS		MIN	TYP	MAX	UNIT
f_{clock}	Maximum clock frequency	69	C_L = 15 pF,	R_L = 400 Ω	15	20		MHz
t_{pd1}	Propagation delay time to logical 1 level from clear to output	70	C_L = 15 pF,	R_L = 400 Ω		16	25	ns
t_{pd0}	Propagation delay time to logical 0 level from clear to output	70	C_L = 15 pF,	R_L = 400 Ω		25	40	ns
t_{pd1}	Propagation delay time to logical 1 level from clock to output	69	C_L = 15 pF,	R_L = 400 Ω	10	16	25	ns
t_{pd0}	Propagation delay time to logical 0 level from clock to output	69	C_L = 15 pF,	R_L = 400 Ω	10	25	40	ns

—SEE ORDERING INSTRUCTIONS PAGE 1-1—

functional block diagram (each flip-flop)



schematic (each flip-flop)



NOTE: Component values shown are nominal.

CIRCUIT TYPES SN5474, SN7474
DUAL D-TYPE EDGE-TRIGGERED FLIP-FLOPS

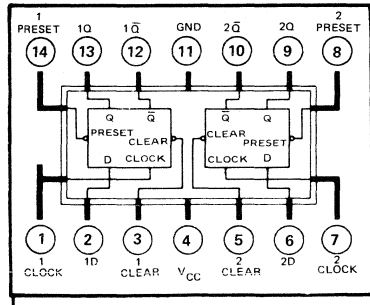
logic

TRUTH TABLE (Each Flip-Flop)

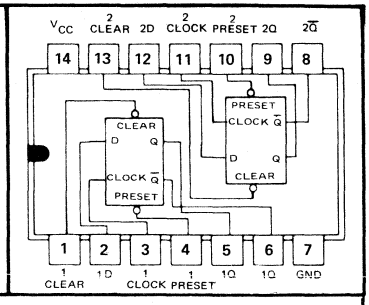
t_n	t_{n+1}	
INPUT	OUTPUT	OUTPUT
D	Q	$\overline{Q}$
0	0	1
1	1	0

NOTES: 1. t_n = bit time before clock pulse.
2. t_{n+1} = bit time after clock pulse.

S FLAT PACKAGE
(TOP VIEW)



J OR N DUAL-IN-LINE PACKAGE
(TOP VIEW)



positive logic: Low input to preset sets Q to logical 1
Low input to clear sets Q to logical 0
Preset and clear are independent of clock

description

These monolithic, dual, D-type, edge-triggered flip-flops feature direct clear and preset inputs and complementary Q and $\overline{Q}$ outputs. Input information is transferrred to the outputs on the positive edge of the clock pulse.

Clock triggering occurs at a voltage level of the clock pulse and is not directly related to the transition time of the positive going pulse. After the clock input threshold voltage has been passed, the data input (D) is locked out.

These dual flip-flops have the same clocking characteristics as the SN5470/SN7470 gated (edge-triggered) flip-flop circuits, and both are ideally suited for medium- to-high-speed applications. They can result in a significant saving in system power dissipation and package count in applications where input gating is not required.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply Voltage V_{CC}: SN5474 Circuits	4.5	5	5.5	V
SN7474 Circuits	4.75	5	5.25	V
Operating Free-Air Temperature Range, T_A: SN5474 Circuits	−55	25	125	°C
SN7474 Circuits	0	25	70	°C
Normalized Fan-Out From Each Output, N			10	
Width of Clock Pulse, $t_{p(clock)}$ (See figure 71)	30			ns
Width of Preset Pulse, $t_{p(preset)}$ (See figure 67)	30			ns
Width of Clear Pulse, $t_{p(clear)}$ (See figure 67)	30			ns

–SEE ORDERING INSTRUCTIONS PAGE 1-1–

electrical characteristics (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
$V_{in(1)}$	Input voltage required to ensure logical 1 at any input terminal	52 and 53	V_{CC} = MIN		2			V
$V_{in(0)}$	Input voltage required to ensure logical 0 at any input terminal	52 and 53	V_{CC} = MIN				0.8	V
$V_{out(1)}$	Logical 1 output voltage	52	V_{CC} = MIN,	I_{load} = −400 μA	2.4	3.5		V
$V_{out(0)}$	Logical 0 output voltage	53	V_{CC} = MIN,	I_{sink} = 16 mA		0.22	0.4	V
$I_{in(0)}$	Logical 0 level input current at preset or D	54	V_{CC} = MAX,	V_{in} = 0.4 V			−1.6	mA
$I_{in(0)}$	Logical 0 level input current at clear or clock	54	V_{CC} = MAX,	V_{in} = 0.4 V			−3.2	mA
$I_{in(1)}$	Logical 1 level input current at D	55	V_{CC} = MAX,	V_{in} = 2.4 V			40	μA
			V_{CC} = MAX,	V_{in} = 5.5 V			1	mA
$I_{in(1)}$	Logical 1 level input current at preset or clock	55	V_{CC} = MAX,	V_{in} = 2.4 V			80	μA
			V_{CC} = MAX,	V_{in} = 5.5 V			1	mA
$I_{in(1)}$	Logical 1 level input current at clear	55	V_{CC} = MAX,	V_{in} = 2.4 V			120	μA
			V_{CC} = MAX,	V_{in} = 5.5 V			1	mA
I_{OS}	Short-circuit output current§	56	V_{CC} = MAX,	V_{in} = 0, SN5474	−20		−57	mA
				V_{in} = 0, SN7474	−18		−57	
I_{CC}	Supply current	55	V_{CC} = MAX,	V_{in} = 5 V		17	30	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

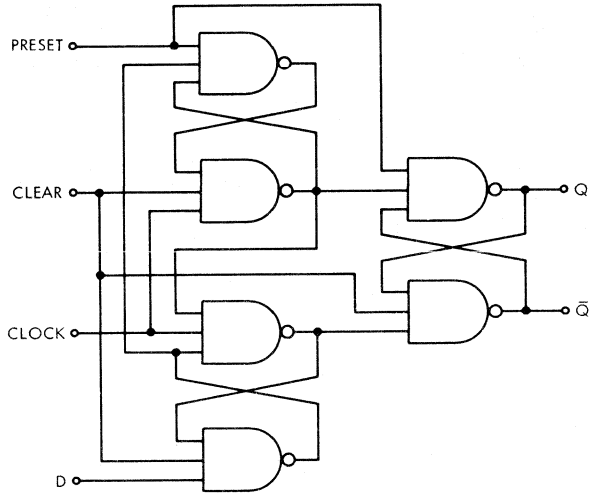
§ Not more than one output should be shorted at a time.

switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10

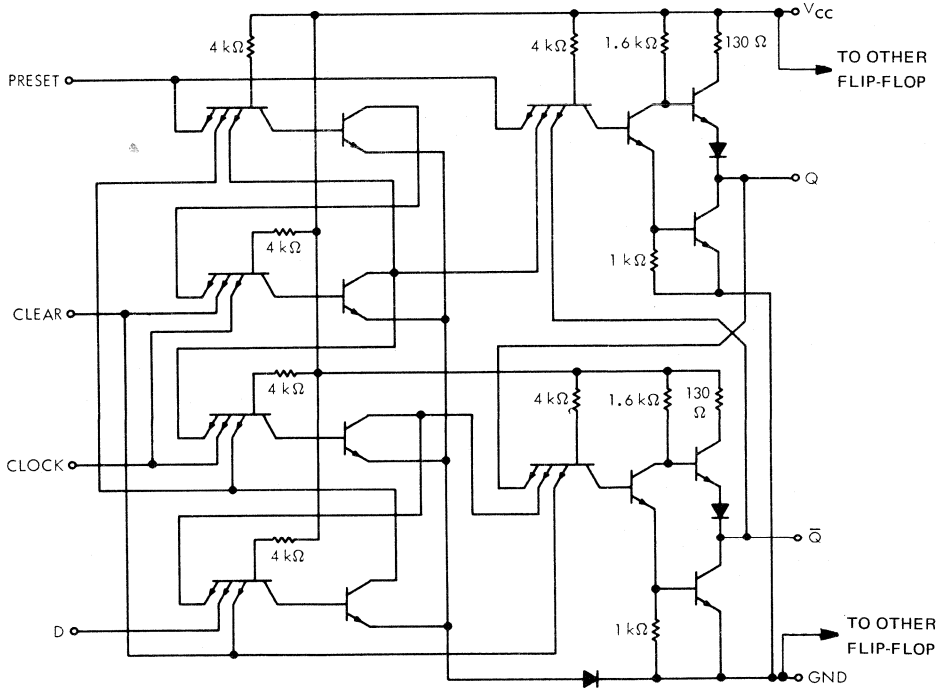
PARAMETER		TEST FIGURE	TEST CONDITIONS		MIN	TYP	MAX	UNIT
f_{clock}	Maximum clock frequency	71	C_L = 15 pF,	R_L = 400 Ω	15	25		MHz
t_{setup}	Minimum input setup time	71	C_L = 15 pF,	R_L = 400 Ω		15	20	ns
t_{hold}	Minimum input hold time	71	C_L = 15 pF,	R_L = 400 Ω		2	5	ns
t_{pd1}	Propagation delay time to logical 1 level from clear or preset to output	67	C_L = 15 pF,	R_L = 400 Ω			25	ns
t_{pd0}	Propagation delay time to logical 0 level from clear or preset to output	67	C_L = 15 pF,	R_L = 400 Ω			40	ns
t_{pd1}	Propagation delay time to logical 1 level from clock to output	71	C_L = 15 pF,	R_L = 400 Ω	10	14	25	ns
t_{pd0}	Propagation delay time to logical 0 level from clock to output	71	C_L = 15 pF,	R_L = 400 Ω	10	20	40	ns

–SEE ORDERING INSTRUCTIONS PAGE 1-1–

functional block diagram (each flip-flop)



schematic (each flip-flop)



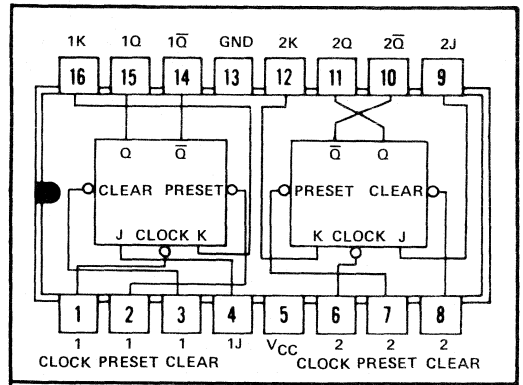
NOTE: Component values shown are nominal.

logic

TRUTH TABLE (Each Flip-Flop)		
t_n		t_{n+1}
J	K	Q
0	0	Q_n
0	1	0
1	0	1
1	1	$\overline{Q}_n$

NOTES: 1. t_n = Bit time before clock pulse.
2. t_{n+1} = Bit time after clock pulse.

J OR N DUAL-IN-LINE PACKAGE
(TOP VIEW)

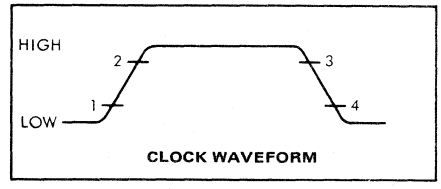


positive logic: Low input to preset sets Q to logical 1
Low input to clear sets Q to logical 0
Clear and preset are independent from clock

description

The SN7476 J-K flip-flop is based on the master-slave principle. Inputs to the master section are controlled by the clock pulse. The clock pulse also regulates the state of the coupling transistors which connect the master and slave sections. The sequence of operation is as follows:

1. Isolate slave from master
2. Enter information from J and K inputs to master
3. Disable J and K inputs
4. Transfer information from master to slave.



CLOCK WAVEFORM

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply Voltage V_{CC}: SN5476 Circuits	4.5	5	5.5	V
SN7476 Circuits	4.75	5	5.25	V
Operating Free-Air Temperature Range, T_A: SN5476 Circuits	−55	25	125	°C
SN7476 Circuits	0	25	70	°C
Normalized Fan-Out From Each Output, N			10	
Width of Clock Pulse, $t_{p(clock)}$ (See figure 69)	20			ns
Width of Preset Pulse, $t_{p(preset)}$ (See figure 70)	25			ns
Width of Clear Pulse, $t_{p(clear)}$ (See figure 70)	25			ns
Input Setup Time, t_{setup} (See figure 69)	$\geq t_{p(clock)}$			
Input Hold Time, t_{hold}	0			

—SEE ORDERING INSTRUCTIONS PAGE 1-1—

electrical characteristics, T_A = 0°C to 70°C (unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
$V_{in(1)}$	Input voltage required to ensure logical 1 at any input terminal	46 and 47	V_{CC} = MIN		2			V
$V_{in(0)}$	Input voltage required to ensure logical 0 at any input terminal	46 and 47	V_{CC} = MIN				0.8	V
$V_{out(1)}$	Logical 1 output voltage	46	V_{CC} = MIN, I_{load} = −400 μA		2.4	3.5		V
$V_{out(0)}$	Logical 0 output voltage	47	V_{CC} = MIN, I_{sink} = 16 mA			0.22	0.4	V
$I_{in(0)}$	Logical 0 level input current at J or K	48	V_{CC} = MAX, V_{in} = 0.4 V				−1.6	mA
$I_{in(0)}$	Logical 0 level input current at clear, preset, or clock	48	V_{CC} = MAX, V_{in} = 0.4 V				−3.2	mA
$I_{in(1)}$	Logical 1 level input current at J or K	49	V_{CC} = MAX, V_{in} = 2.4 V				40	μA
			V_{CC} = MAX, V_{in} = 5.5 V				1	mA
$I_{in(1)}$	Logical 1 level input current at clear, preset, or clock	49	V_{CC} = MAX, V_{in} = 2.4 V				80	μA
			V_{CC} = MAX, V_{in} = 5.5 V				1	mA
I_{OS}	Short-circuit output current§	51	V_{CC} = MAX, V_{in} = 0	SN5476	−20		−57	mA
				SN7476	−18		−57	
I_{CC}	Supply current (each flip-flop)	49	V_{CC} = MAX, V_{in} = 5 V			20	40	mA

switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{clock}	Maximum clock frequency	69	C_L = 15 pF, R_L = 400 Ω	15	20		MHz
t_{pd1}	Propagation delay time to logical 0 level from clear or preset to output	70	C_L = 15 pF, R_L = 400 Ω		16	25	ns
t_{pd0}	Propagation delay time to logical 1 level from clear or preset to output	70	C_L = 15 pF, R_L = 400 Ω		25	40	ns
t_{pd1}	Propagation delay time to logical 1 level from clock to output	69	C_L = 15 pF, R_L = 400 Ω	10	16	25	ns
t_{pd0}	Propagation delay time to logical 0 level from clock to output	69	C_L = 15 pF, R_L = 400 Ω	10	25	40	ns

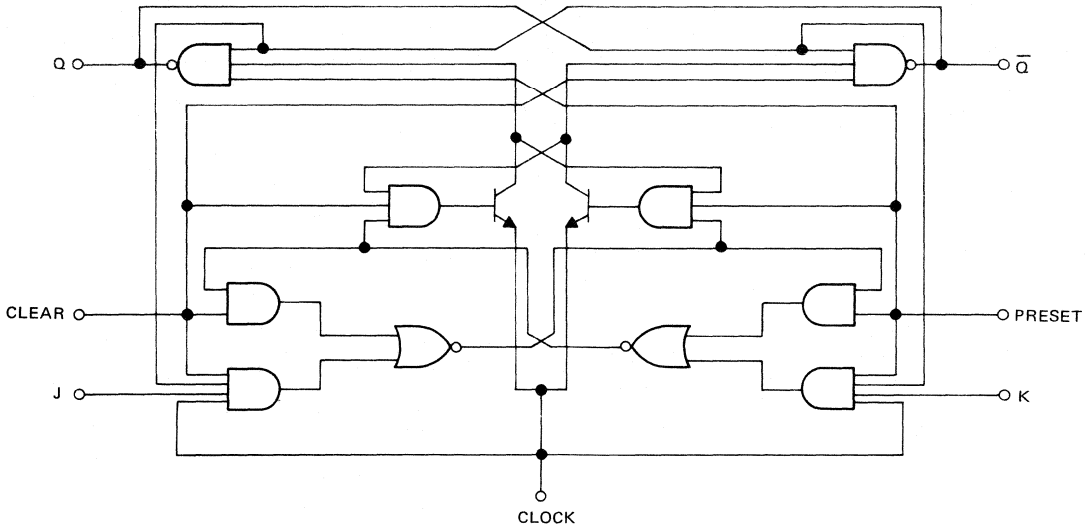
†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

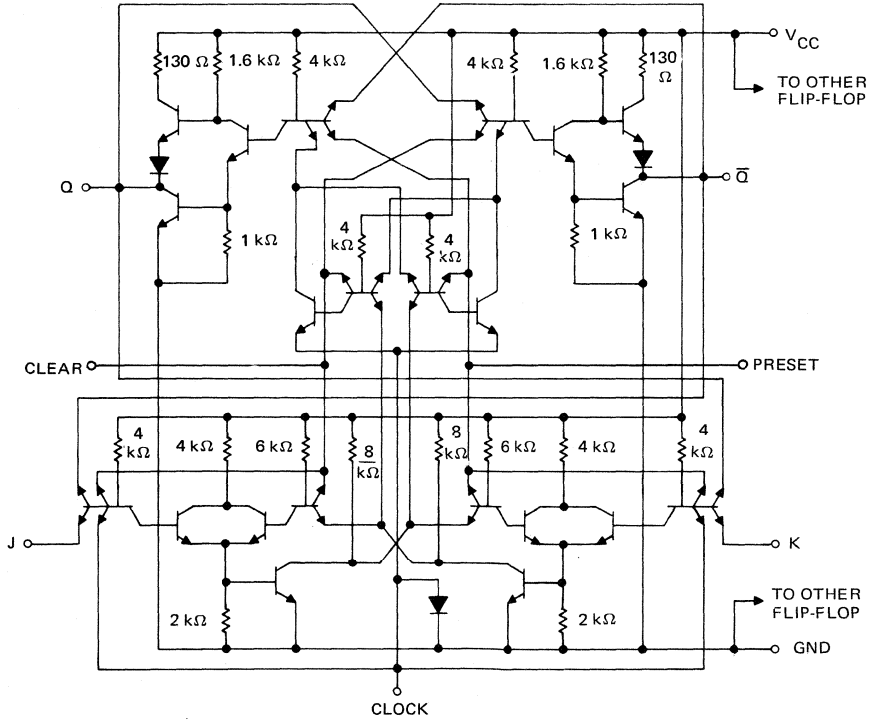
§Not more than one output should be shorted at a time.

—SEE ORDERING INSTRUCTIONS PAGE 1-1—

functional block diagram (each flip-flop)



schematic (each flip-flop)



NOTE: Component values shown are nominal.

logic

TRUTH TABLE (See Notes 1 thru 3)

t_n INPUT			t_{n+1} INPUT			OUTPUT
A1	A2	B	A1	A2	B	
1	1	0	1	1	1	Inhibit
0	X	1	0	X	0	Inhibit
X	0	1	X	0	0	Inhibit
0	X	0	0	X	1	One Shot
X	0	0	X	0	1	One Shot
1	1	1	X	0	1	One Shot
1	1	1	0	X	1	One Shot
X	0	0	X	1	0	Inhibit
0	X	0	1	X	0	Inhibit
X	0	1	1	1	1	Inhibit
0	X	1	1	1	1	Inhibit
1	1	0	X	0	0	Inhibit
1	1	0	0	X	0	Inhibit

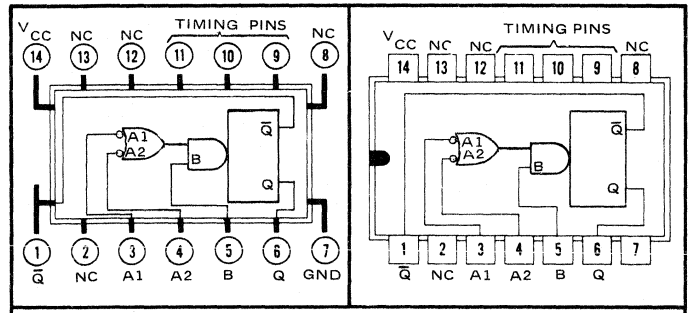
$1 = V_{in(1)} \geq 2\ V$

$0 = V_{in(0)} \leq 0.8\ V$

NOTES: 1. t_n = time before input transition.
2. t_{n+1} = time after input transition.
3. X indicates that either a logical 0 or 1, may be present.
4. NC = No Internal Connection.

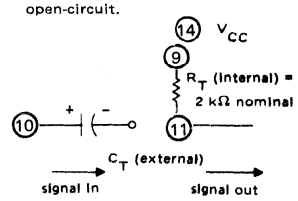
S FLAT PACKAGE
(TOP VIEW)
(SEE NOTES 6 THRU 9)

J OR N DUAL-IN-LINE PACKAGE
(TOP VIEW)
(SEE NOTES 6 THRU 9)



positive logic: see truth table and notes 5 and 6

5. A1 and A2 are negative-edge-triggered-logic inputs, and will trigger the one shot when either or both go to logical 0 with B at logical 1.
6. B is a positive Schmitt-trigger input for slow edges or level detection, and will trigger the one shot when B goes to logical 1 with either A1 or A2 at logical 0. (See Truth Table)
7. External timing capacitor may be connected between pin (10) (positive) and pin (11). With no external capacitance, an output pulse width of typically 30 ns is obtained.
8. To use the internal timing resistor (2 kΩ nominal), connect pin (9) to pin (14).
9. To obtain variable pulse width connect external variable resistance between pin (9) and pin (14). No external current limiting is needed.
10. For accurate repeatable pulse widths connect an external resistor between pin (11) and pin (14) with pin (9) open-circuit.



description

This monolithic TTL monostable multivibrator features d-c triggering from positive or gated negative-going inputs with inhibit facility. Both positive and negative-going output pulses are provided with full fan-out to 10 normalized loads.

Pulse triggering occurs at a particular voltage level and is not directly related to the transition time of the input pulse. Schmitt-trigger input circuitry (TTL compatible and featuring temperature-independent backlash, See Figure L) for the B input allows jitter-free triggering from inputs with transition times as slow as 1 volt/second, providing the circuit with an excellent noise immunity of typically 1.2 volts. A high immunity to V_{CC} noise of typically 1.5 volts is also provided by internal latching circuitry.

Once fired, the outputs are independent of further transitions on the inputs and are a function only of the timing components. Input pulses may be of any duration relative to the output pulse. Output pulse lengths may be varied from 40 nanoseconds to 40 seconds by choosing appropriate timing components. With no external timing components (i.e., pin (9) connected to pin (14), pins (10), (11) open) an output pulse of typically 30 nanoseconds is achieved which may be used as a d-c triggered reset signal. Output rise and fall times are TTL compatible and independent of pulse length.

Pulse width is achieved through internal compensation and is virtually independent of V_{CC} and temperature. In most applications, pulse stability will only be limited by the accuracy of external timing components.

–SEE ORDERING INSTRUCTIONS PAGE 1-1–

description (continued)

Jitter-free operation is maintained over the full temperature and V_{CC} range for more than six decades of timing capacitance (10 pF to 10 μF) and more than one decade of timing resistance (2 kΩ to 40 kΩ). Throughout these ranges, pulse width is defined by the relationship $t_{p(out)} = C_T R_T \log_e 2$.

Circuit performance is achieved with a nominal power dissipation of 90 milliwatts at 5 volts (50% duty cycle) and a quiescent dissipation of typically 65 milliwatts.

Duty cycles as high as 90% are achieved when using R_T = 40 kΩ. Higher duty cycles are achievable if a certain amount of pulse-width jitter is allowed.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply Voltage V_{CC}: SN54121 Circuits	4.5	5	5.5	V
SN74121 Circuits	4.75	5	5.25	V
Normalized Fan-Out From Each Output, N			10	
Input Pulse Rise/Fall Time: Schmitt Input (B)			1	V/s
Logic Inputs (A1, A2)			1	V/μs
Input Pulse Width	50			ns
External Timing Resistance Between Pins ⑪ and ⑭ (Pin ⑨ open)	1.4			kΩ
External Timing Resistance: SN54121			30	kΩ
SN74121			40	kΩ
Timing Capacitance	0		1000	μF
Output Pulse Width			40	s
Duty Cycle: R_T = 2 kΩ			67%	
R_T = 30 kΩ (SN54121) or R_T = 40 kΩ (SN74121)			90%	

—SEE ORDERING INSTRUCTIONS PAGE 1-1—

electrical characteristics over operating free-air temperature range

PARAMETER		TEST FIGURE	TEST CONDITIONS†		MIN	TYP‡	MAX	UNITS
V_{T+}	Positive-going threshold voltage at A input	57	V_{CC} = MIN			1.4	2	V
V_{T-}	Negative-going threshold voltage at A input	57	V_{CC} = MIN		0.8	1.4		V
V_{T+}	Positive-going threshold voltage at B input	57	V_{CC} = MIN			1.55	2	V
V_{T-}	Negative-going threshold voltage at B input	57	V_{CC} = MIN		0.8	1.35		V
$V_{out(0)}$	Logical 0 output voltage	57	V_{CC} = MIN, I_{sink} = 16 mA			0.22	0.4	V
$V_{out(1)}$	Logical 1 output voltage	57	V_{CC} = MIN, I_{load} = −400 μA		2.4	3.3		V
$I_{in(0)}$	Logical 0 level input current at A1 or A2	58	V_{CC} = MAX, V_{in} = 0.4 V			−1	−1.6	mA
$I_{in(0)}$	Logical 0 level input current at B	59	V_{CC} = MAX, V_{in} = 0.4 V			−2	−3.2	mA
$I_{in(1)}$	Logical 1 level input current at A1 or A2	60	V_{CC} = MAX, V_{in} = 2.4 V			2	40	μA
			V_{CC} = MAX, V_{in} = 5.5 V			0.05	1	mA
$I_{in(1)}$	Logical 1 level input current at B	61	V_{CC} = MAX, V_{in} = 2.4 V			4	80	μA
			V_{CC} = MAX, V_{in} = 5.5 V			0.05	1	mA
I_{OS}	Short circuit output current at Q or $\overline{Q}$§	62 and 63	V_{CC} = MAX	SN54121	−20	−25	−55	mA
				SN74121	−18	−25	−55	
I_{CC}	Power supply current in quiescent (unfired) state	64	V_{CC} = MAX			13	25	mA
I_{CC}	Power supply current in fired state	64	V_{CC} = MAX			23	40	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST FIGURE	TEST CONDITIONS		MIN	TYP	MAX	UNITS
t_{pd1}	Propagation delay time to logical 1 level from B input to Q output	72	C_L = 15 pF,	C_T = 80 pF	15	35	55	ns
t_{pd1}	Propagation delay time to logical 1 level from A1/A2 inputs to Q output				25	45	70	ns
t_{pd0}	Propagation delay time to logical 0 level from B input to $\overline{Q}$ output	72	C_L = 15 pF,	C_T = 80 pF	20	40	65	ns
t_{pd0}	Propagation delay time to logical 0 level from A1/A2 inputs to $\overline{Q}$ output				30	50	80	ns
$t_{p(out)}$	Pulse width obtained using internal timing resistor	73	C_L = 15 pF, R_T = Open,	C_T = 80 pF, Pin ⑨ to V_{CC}	70	110	150	ns
$t_{p(out)}$	Pulse width obtained with zero timing capacitance	73	C_L = 15 pF, R_T = Open,	C_T = 0, Pin ⑨ to V_{CC}	20	30	50	ns
$t_{p(out)}$	Pulse width obtained using external timing resistor	73	C_L = 15 pF, R_T = 10 kΩ,	C_T = 100 pF, Pin ⑨ Open	600	700	800	ns
			C_L = 15 pF, R_T = 10 kΩ,	C_T = 1 μF, Pin ⑨ Open	6	7	8	ms
t_{hold}	Minimum duration of trigger pulse	73	C_L = 15 pF, R_T = Open,	C_T = 80 pF, Pin ⑨ to V_{CC}		30	50	ns

—SEE ORDERING INSTRUCTIONS PAGE 1-1—

TYPICAL CHARACTERISTICS§

DISTRIBUTION OF UNITS
for
OUTPUT PULSE WIDTH

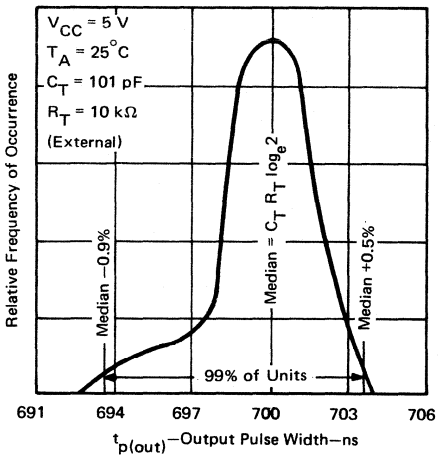


FIGURE H

VARIATION IN INTERNAL TIMING RESISTOR VALUE
vs
FREE-AIR TEMPERATURE

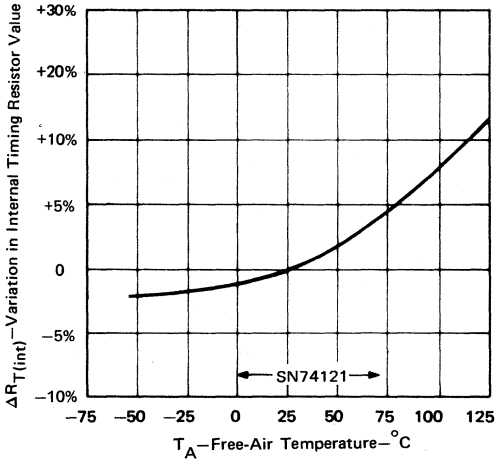


FIGURE I

VARIATION IN OUTPUT PULSE WIDTH
vs
SUPPLY VOLTAGE

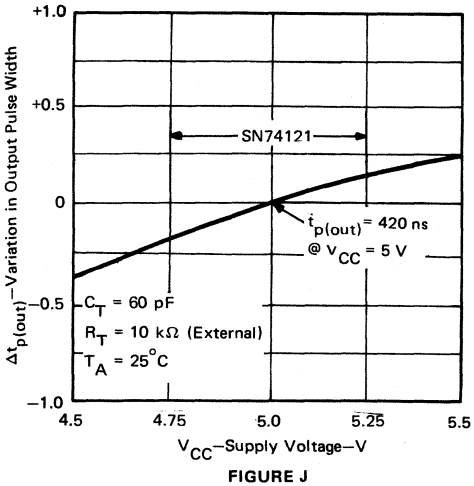


FIGURE J

VARIATION IN OUTPUT PULSE WIDTH
vs
FREE-AIR TEMPERATURE

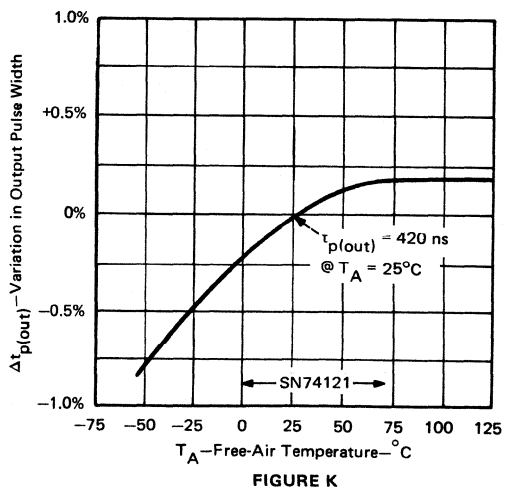


FIGURE K

§ Unless otherwise noted data is applicable for SN54121 and SN74121.

TYPICAL CHARACTERISTICS §

SCHMITT TRIGGER THRESHOLD VOLTAGE
vs
FREE-AIR TEMPERATURE

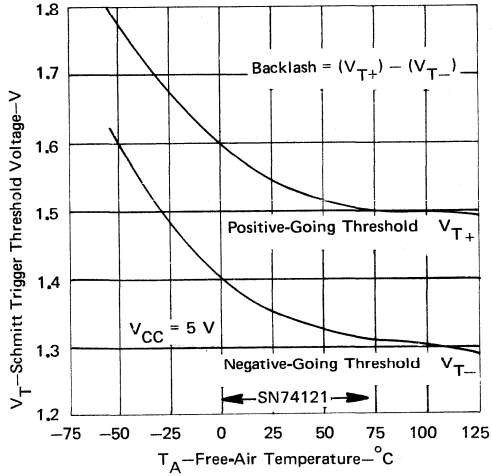


FIGURE L

PROPAGATION DELAY TIME TO LOGICAL 1 LEVEL
(B INPUT TO Q OUTPUT)
vs
FREE-AIR TEMPERATURE

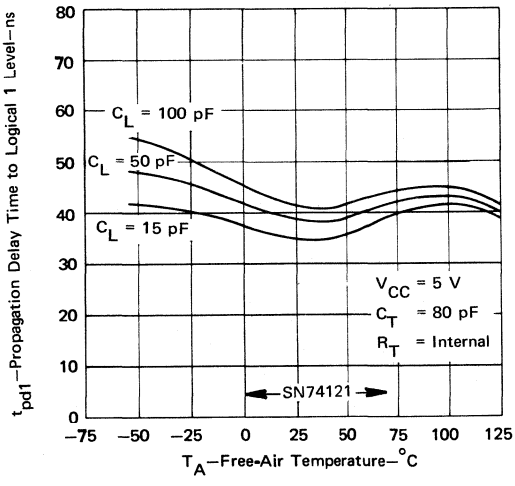


FIGURE M

PROPAGATION DELAY TIME TO LOGICAL 0 LEVEL
(B INPUT TO $\overline{Q}$ OUTPUT)
vs
FREE-AIR TEMPERATURE

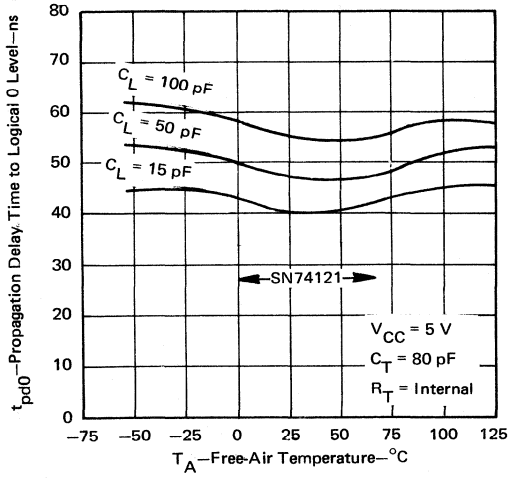


FIGURE N

§ Unless otherwise noted data is applicable for SN54121 and SN74121.

TYPICAL CHARACTERISTICS §

OUTPUT PULSE WIDTH
vs
TIMING RESISTOR VALUE

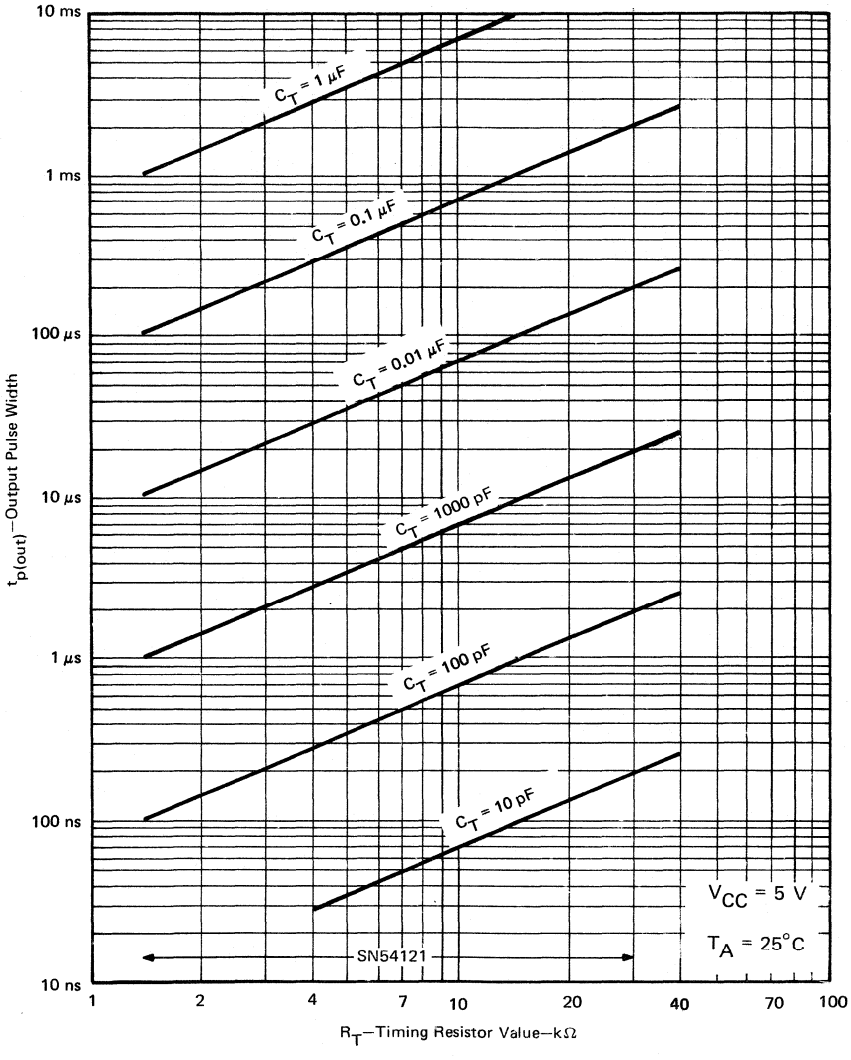


FIGURE O

§Unless otherwise noted data is applicable for SN54121 and SN74121.

TYPICAL CHARACTERISTICS §

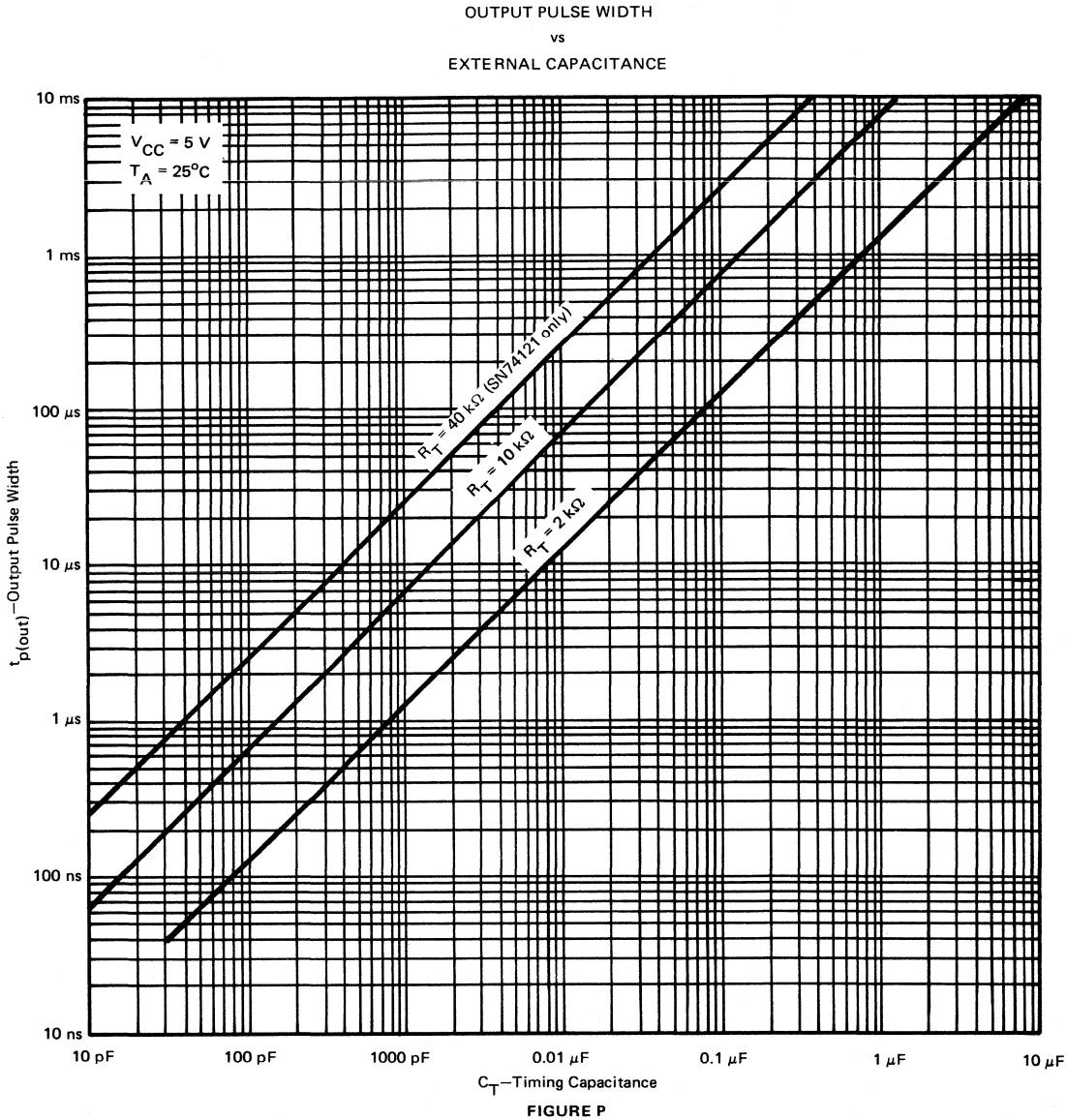
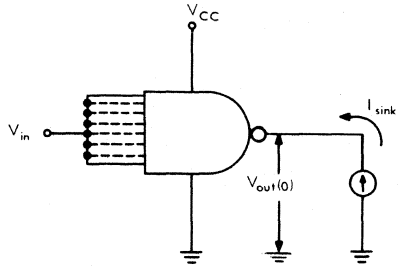


FIGURE P

§Unless otherwise noted data is applicable for SN54121 and SN74121.

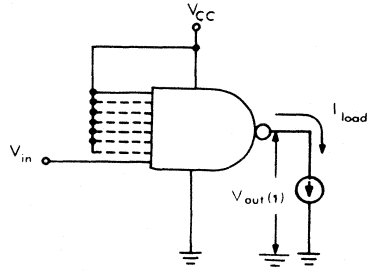
PARAMETER MEASUREMENT INFORMATION

d-c test circuits§



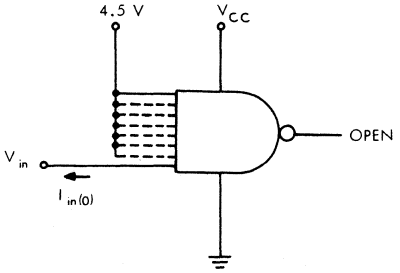
1. All inputs are tested separately.

FIGURE 1



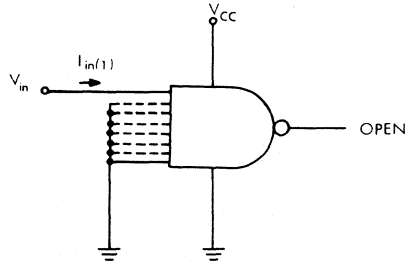
1. Each input is tested separately

FIGURE 2



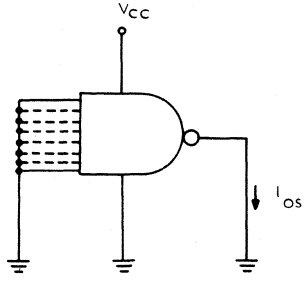
1. Each input is tested separately.

FIGURE 3



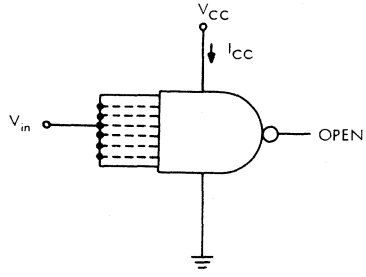
1. Each input is tested separately.

FIGURE 4



1. Each gate is tested separately.

FIGURE 5



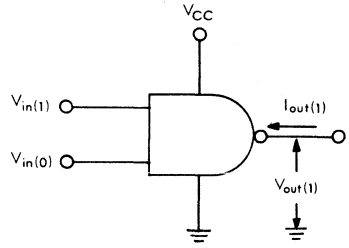
1. Logical 0 and logical 1 conditions are tested.

FIGURE 6

§Arrows indicate actual direction of current flow.

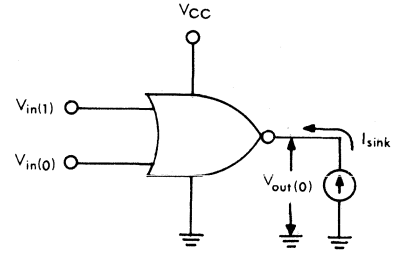
PARAMETER MEASUREMENT INFORMATION

d-c test circuits§ (continued)



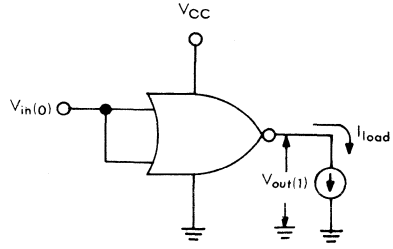
1. Each input is tested separately.

FIGURE 7



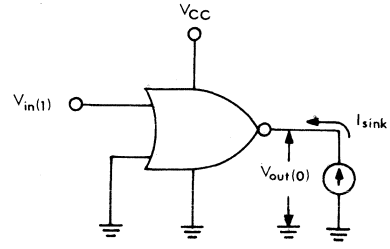
1. Each input is tested separately.

FIGURE 8



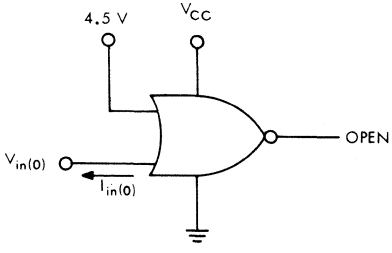
1. Both inputs are tested simultaneously.

FIGURE 9



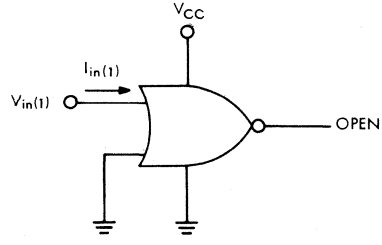
1. Each input is tested separately.

FIGURE 10



1. Each input is tested separately.

FIGURE 11



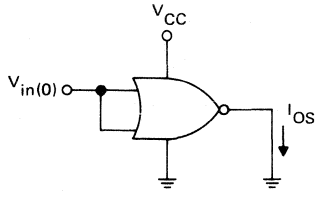
1. Each input is tested separately.

FIGURE 12

§Arrows indicate actual direction of current flow.

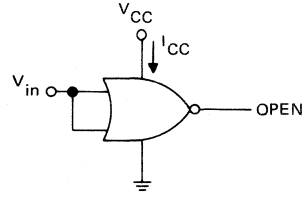
PARAMETER MEASUREMENT INFORMATION

d-c test circuits§ (continued)



1. Each gate is tested separately.

FIGURE 13



1. Each gate is tested separately.
2. Logical 0 and logical 1 conditions are tested.

FIGURE 14

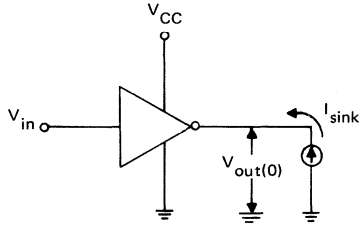
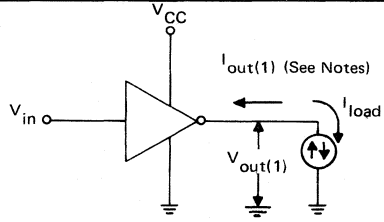


FIGURE 15



1. I_{load} is measured for totem-pole outputs.
2. $I_{out(1)}$ is measured for open-collector outputs.

FIGURE 16

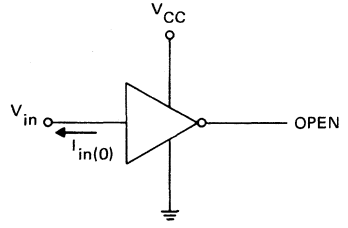


FIGURE 17

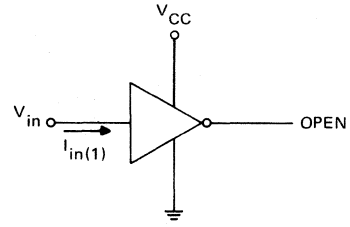
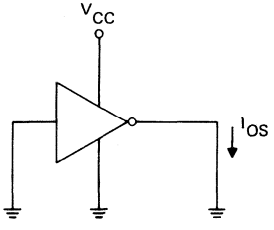
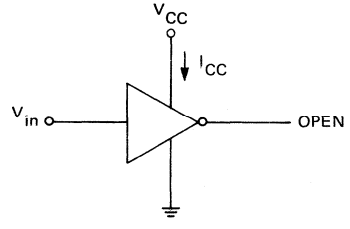


FIGURE 18



1. Each inverter is tested separately

FIGURE 19



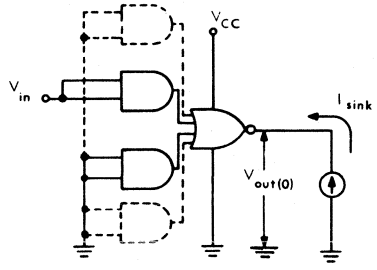
1. All inverters are tested simultaneously

FIGURE 20

§ Arrows indicate actual direction of current flow

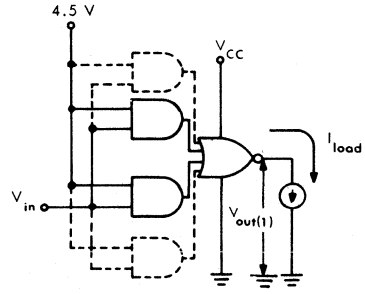
PARAMETER MEASUREMENT INFORMATION

d-c test circuits § (continued)



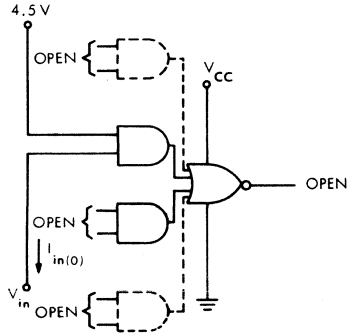
1. Each AND section is tested separately.

FIGURE 21



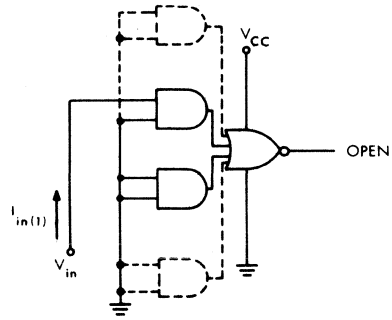
1. Each pair of inputs is tested separately.

FIGURE 22



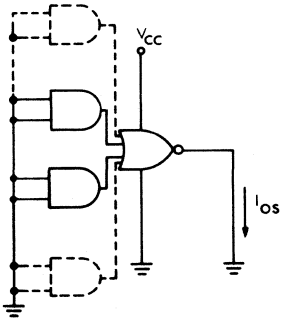
1. Each input is tested separately.

FIGURE 23



1. Each input is tested separately.

FIGURE 24



1. Each gate is tested separately.

FIGURE 25

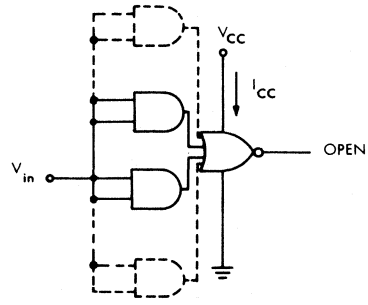


FIGURE 26

§ Arrows indicate actual direction of current flow.

PARAMETER MEASUREMENT INFORMATION

d-c test circuits § (continued)

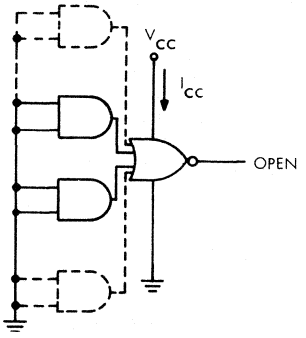


FIGURE 27

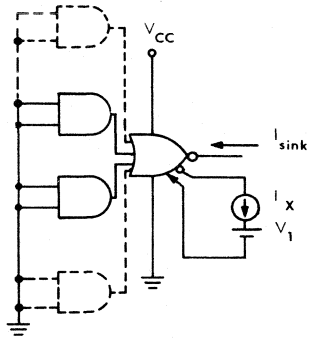


FIGURE 28

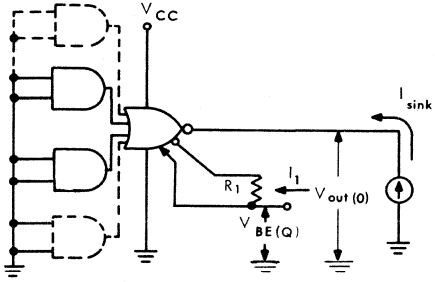


FIGURE 29

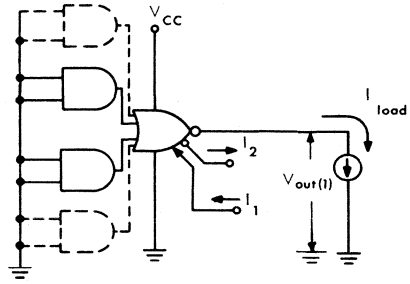
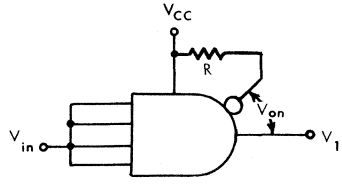
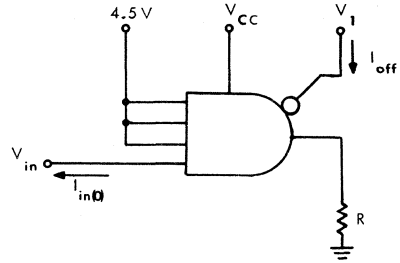


FIGURE 30



1. All inputs are tested simultaneously.

FIGURE 31



1. Each input is tested separately.

FIGURE 32

§ Arrows indicate actual direction of current flow.

PARAMETER MEASUREMENT INFORMATION

d-c test circuits§ (continued)

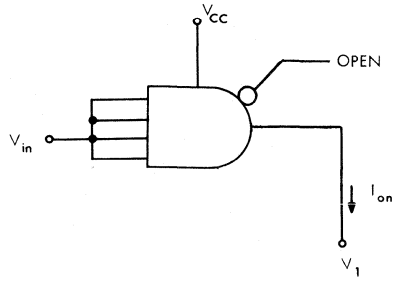
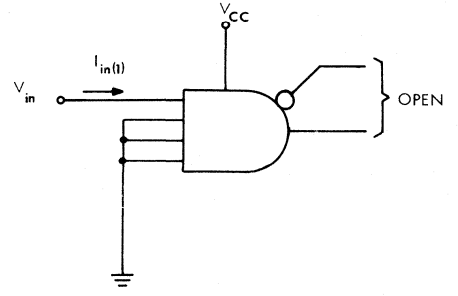
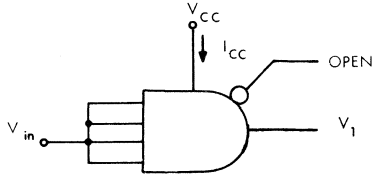


FIGURE 33



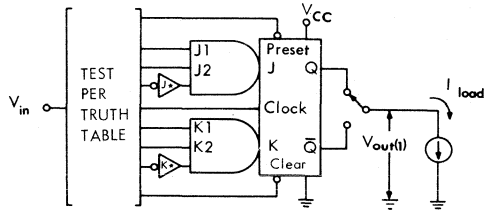
1. Each input is tested separately.

FIGURE 34



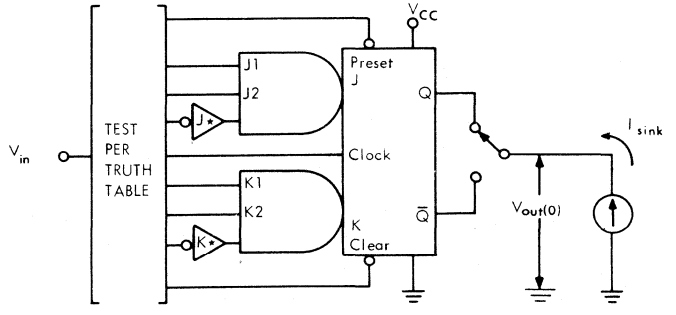
1. "On" and "off" conditions are tested separately.
2. Each gate is tested separately.

FIGURE 35



1. Each output is tested separately.
2. Preset and clear are tested with $V_{in(clock)} = 0$.

FIGURE 36



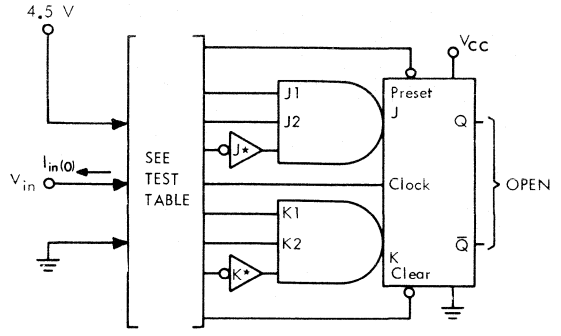
1. Each output is tested separately.

FIGURE 37

§Arrows indicate actual direction of current flow.

PARAMETER MEASUREMENT INFORMATION

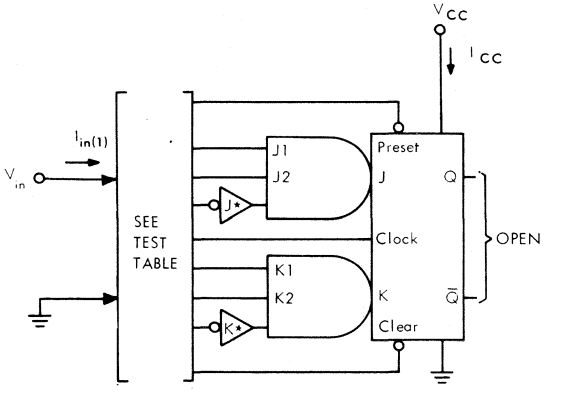
d-c test circuits § (continued)



TEST TABLE			
Apply V_{in} (Test $I_{in(0)}$)	Apply 4.5 V	Ground	Apply Momentary GND, then 4.5 V
J2	J1	J★	Clear
J1	J2	J★	Clear
J★	None	None	None
K2	K1	K★	Preset
K1	K2	K★	Preset
K★	None	None	None
Clock	None	None	None
Preset	K1 and K2	K★	None
Clear	J1 and J2	J★	None

1. Each output is tested separately.

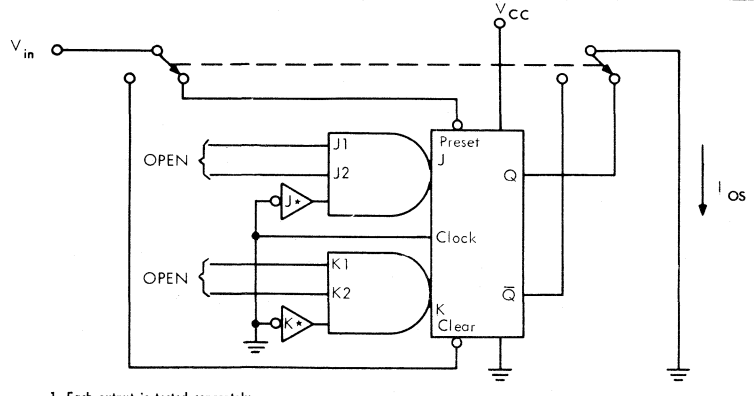
FIGURE 38



TEST TABLE		
Apply V_{in} (Test $I_{in(1)}$)	Ground	Apply 4.5 V
J2	J1 and Clear	J★
J1	J2 and Clear	J★
J★	None	None
K2	K1 and Preset	K★
K1	K2 and Preset	K★
K★	None	None
Clock	None	None
Preset	K1 and K2	K★
Clear	J1 and J2	J★

1. Each input is tested separately.
2. I_{CC} is measured with clear at GND, then with preset at GND.

FIGURE 39



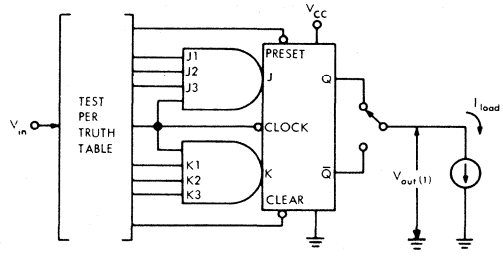
1. Each output is tested separately.

FIGURE 40

§ Arrows indicate actual direction of current flow.

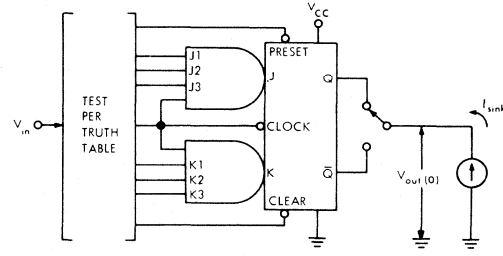
PARAMETER MEASUREMENT INFORMATION

d-c test circuits § (continued)



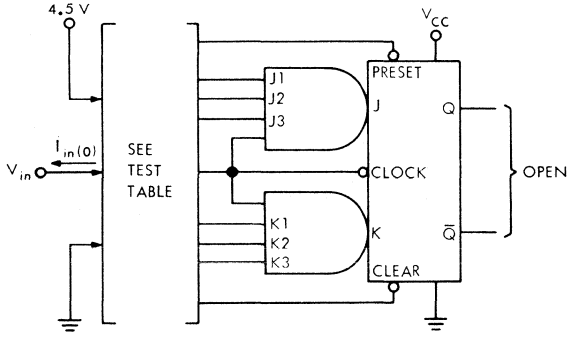
1. Each output is tested separately.

FIGURE 41



1. Each output is tested separately.

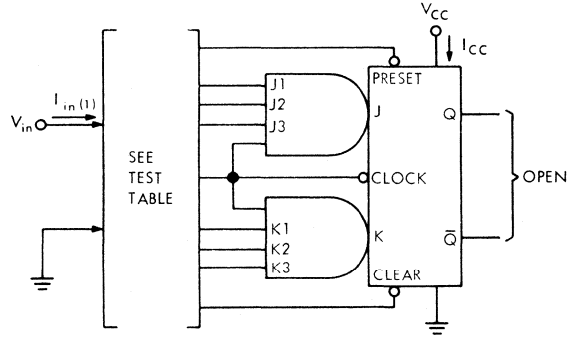
FIGURE 42



1. Each input is tested separately.

TEST TABLE		
Apply V_{in} (Test $I_{in(0)}$)	Apply Momentary GND, then 4.5 V	Apply 4.5 V
Clock	Preset	J1, J2, J3, K1, K2, and K3
Clock	Clear	J1, J2, J3, K1, K2, and K3
Preset	None	J1, J2, J3, K1, K2, and K3
Clear	None	J1, J2, J3, K1, K2, and K3
J1	Clear	Clock, J2, and J3
J2	Clear	Clock, J1, and J3
J3	Clear	Clock, J1, and J2
K1	Preset	Clock, K2, and K3
K2	Preset	Clock, K1, and K3
K3	Preset	Clock, K1, and K2

FIGURE 43



1. Each input is tested separately.
2. I_{CC} is measured with clear at GND, then with preset at GND.

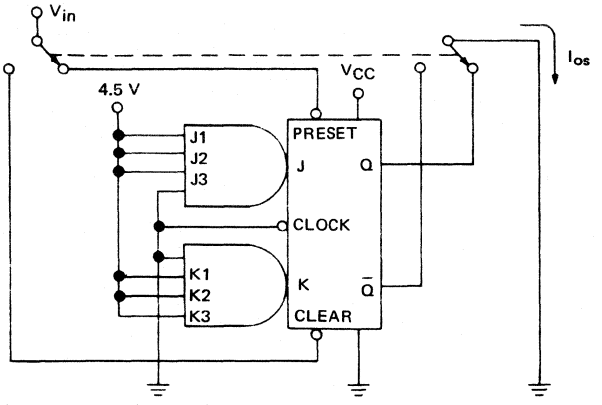
TEST TABLE	
Apply V_{in} (Test $I_{in(1)}$)	Ground
Clock	Preset, Clear, J1, J2, J3, K1, K2, and K3
Preset	Clock, K1, K2, and K3
Clear	Clock, J1, J2, and J3
J1	Clock, Clear, J2, and J3
J2	Clock, Clear, J1, and J3
J3	Clock, Clear, J1, and J2
K1	Clock, Preset, K2, and K3
K2	Clock, Preset, K1, and K3
K3	Clock, Preset, K1, and K2

FIGURE 44

§Arrows indicate actual direction of current flow.

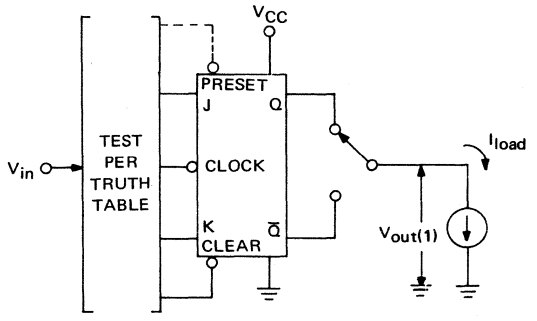
PARAMETER MEASUREMENT INFORMATION

d-c test circuits§ (continued)



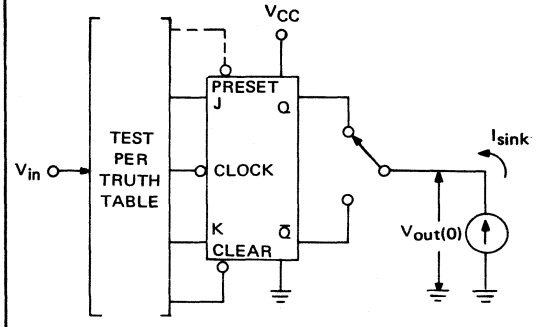
1. Each output is tested separately.

FIGURE 45



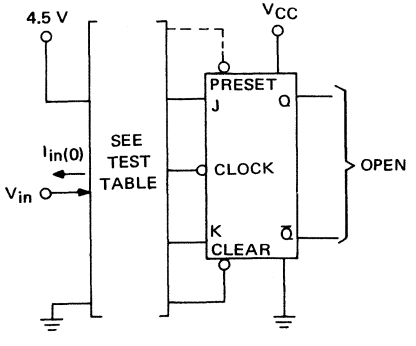
1. Each flip-flop is tested separately.
2. Each output is tested separately.

FIGURE 46



1. Each flip-flop is tested separately.
2. Each output is tested separately.

FIGURE 47



TEST TABLE		
Apply V_{in} (Test $I_{in(0)}$)	Apply Momentary GND	Apply 4.5 V
Clock	Clear (See Note 2)	J and K
Clear	None	Clock and J
Preset	None (See Note 5)	Clock and K
J	Q (See Note 3)	Clock and Clear
K	$\overline{Q}$ (See Note 3)	Clock and Clear

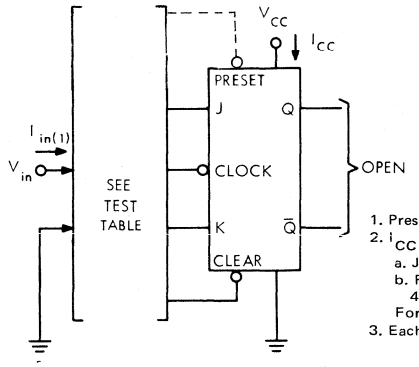
1. Each flip-flop is tested separately.
2. Apply momentary ground, then 4.5 V.
3 After application of momentary ground, Q and $\overline{Q}$ are left floating.
4. Ground all inputs of the unused flip-flop.
5. Preset is applicable for SN5476/SN7476 circuits only.

FIGURE 48

§ Arrows indicate actual direction of current flow.

PARAMETER MEASUREMENT INFORMATION

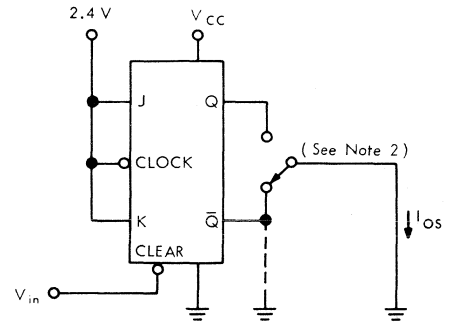
d-c test circuits§ (continued)



TEST TABLE		
Apply V_{in} (Test $I_{in(1)}$)	Ground	Apply Momentary GND, then 4.5 V
Clock	Clear, J, and K	None
Clear	Clock and J	None
Preset (See Note 1)	Clock and K	None
J (See Note 1)	Clock and Clear	Preset
K (See Note 1)	Clock and Preset	Clear

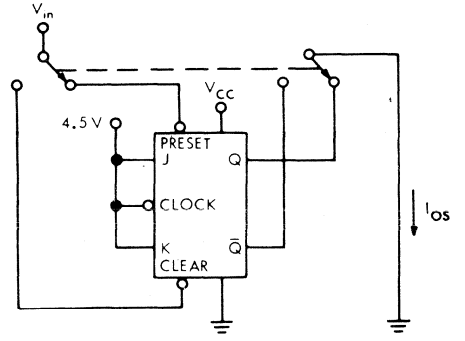
1. Preset is applicable for SN5476/SN7476 circuits only.
2. I_{CC} is measured (simultaneously for both flip-flops) for the following conditions:
   a. J = K = Clock = Clear = GND. For SN5476/SN7476: Preset = 4.5 V.
   b. For SN5473/SN7473: J = Clear = 4.5 V, K = GND, and apply momentary 4.5 V, then GND to Clock.
   For SN5476/SN7476: J = K = Clock = Preset = GND, and Clear = 4.5 V.
3. Each flip-flop is tested separately for $I_{in(1)}$.

FIGURE 49



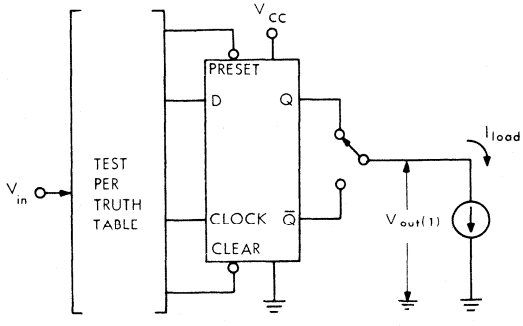
1. Each flip-flop is tested separately.
2. Test circuit shows setup for testing $\bar{Q}$. When testing Q, apply 2.4 V to Clear, ground Q, and limit duration of test to 100 ms.

FIGURE 50



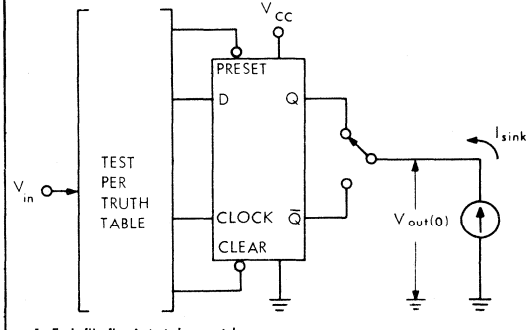
1. Each flip-flop is tested separately.

FIGURE 51



1. Each flip-flop is tested separately.
2. Each output is tested separately.

FIGURE 52



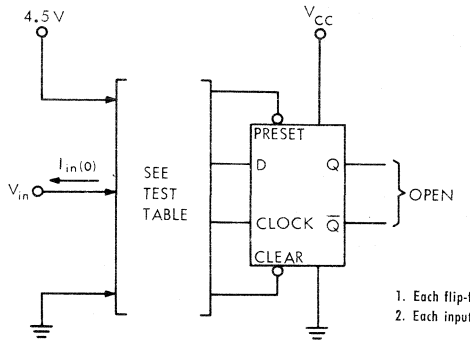
1. Each flip-flop is tested separately.
2. Each output is tested separately.

FIGURE 53

§Arrows indicate actual direction of current flow.

PARAMETER MEASUREMENT INFORMATION

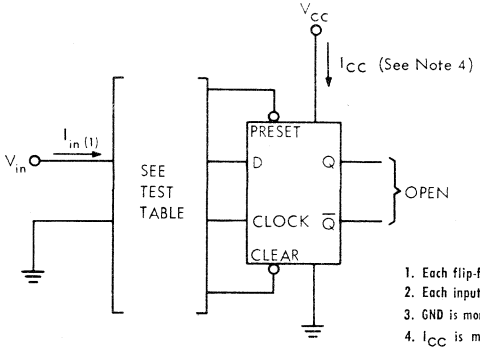
d-c test circuits§ (continued)



TEST TABLE		
Apply V_{in} (Test $I_{in(0)}$)	Apply 4.5 V	Apply GND
Clock	Clear and Preset	D
Preset	Clear and Clock	D
Clear	Clock and D	None
D	Clear and Clock	Preset

1. Each flip-flop is tested separately.
2. Each input is tested separately.

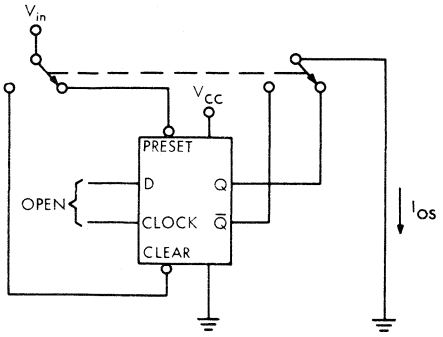
FIGURE 54



TEST TABLE		
Apply V_{in} (Test $I_{in(1)}$)	Apply 4.5 V	Apply GND
Clock	None	Clear
Preset	Clear and D	Clock (See Note 3)
Clear	D and Clock	None
D	Clock	Clear

1. Each flip-flop is tested separately.
2. Each input is tested separately.
3. GND is momentarily applied to clock, then 4.5 V.
4. I_{CC} is measured with D, clock, and preset at GND, then with D, clock, and clear at GND.

FIGURE 55



1. Each output is tested separately.

FIGURE 56

§Arrows indicate actual direction of current flow.

PARAMETER MEASUREMENT INFORMATION

d-c test circuits§ (continued)

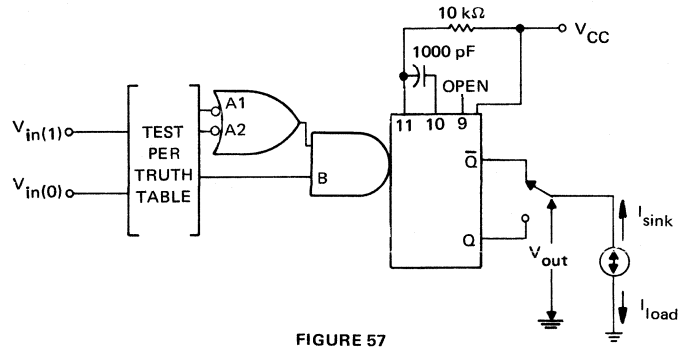
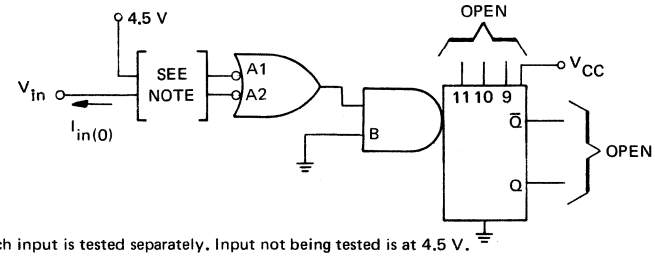


FIGURE 57



1. Each input is tested separately. Input not being tested is at 4.5 V.

FIGURE 58

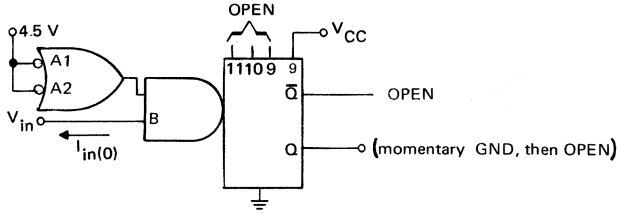
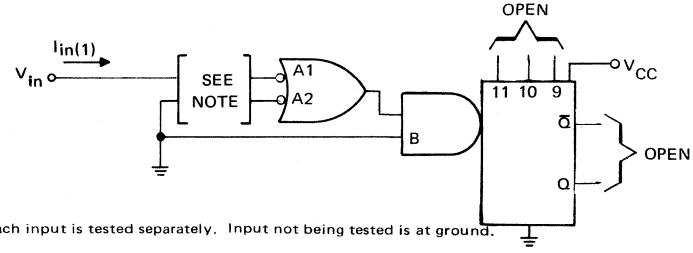


FIGURE 59



1. Each input is tested separately. Input not being tested is at ground.

FIGURE 60

§ Arrows indicate actual direction of current flow.

d-c test circuits § (continued) PARAMETER MEASUREMENT INFORMATION

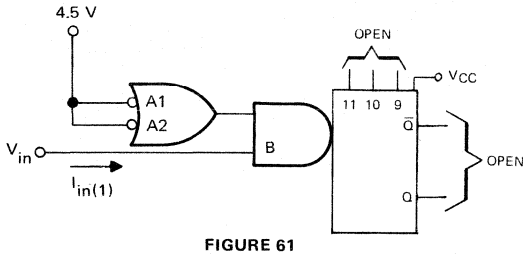
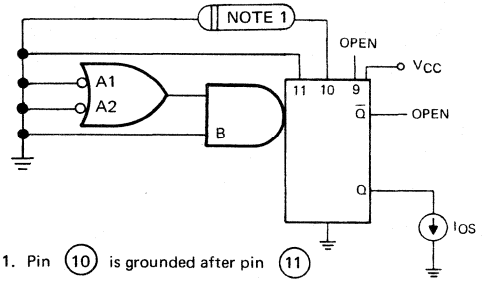


FIGURE 61



1. Pin (10) is grounded after pin (11)

FIGURE 62

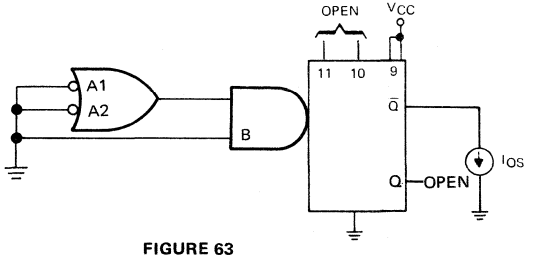
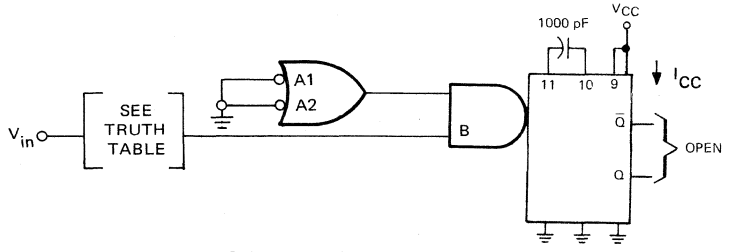


FIGURE 63



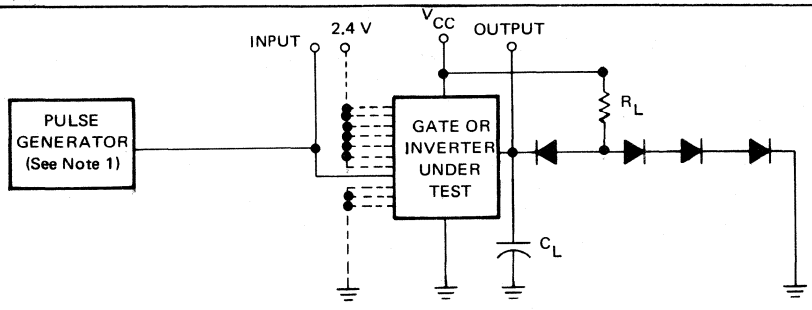
1. Quiescent and fired conditions are tested.

FIGURE 64

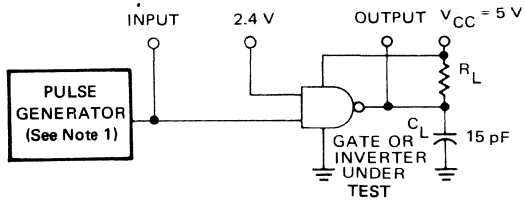
§ Arrows indicate actual direction of current flow.

PARAMETER MEASUREMENT INFORMATION

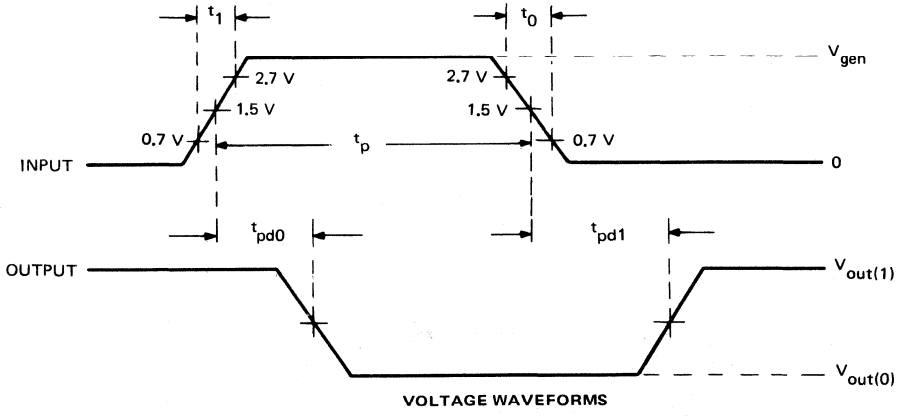
switching characteristics



TEST CIRCUIT FOR SN5400, SN5402, SN5404, SN5410, SN5420, SN5430, SN5440, SN5450, SN5451, SN5453, SN5454, SN7400, SN7402, SN7404, SN7410, SN7420, SN7430, SN7440, SN7450, SN7451, SN7453, AND SN7454



TEST CIRCUIT FOR SN5401, SN5405, SN7401, SN7405



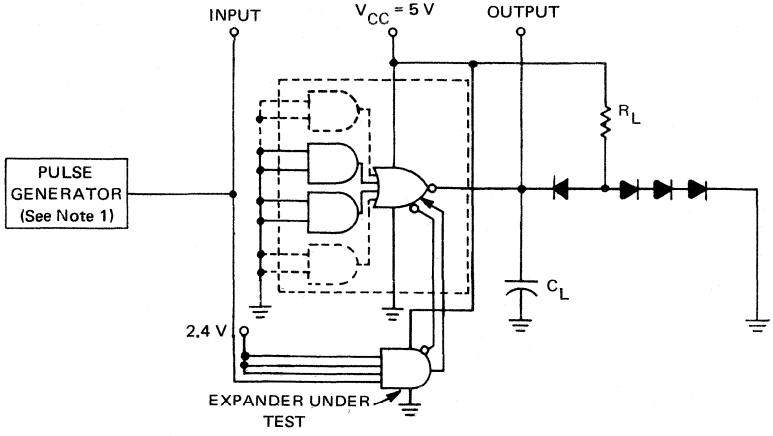
VOLTAGE WAVEFORMS

NOTES: 1. The generator has the following charactertistic: V_{gen} = 3.5 V, t_0 = 5 ns, t_1 = 10 ns, t_p = 0.5 μs, PRR = 1 MHz, $Z_{out} \approx 50\ \Omega$.
2. All diodes are 1N3064.
3. $t_{pd} = \dfrac{t_{pd0} + t_{pd1}}{2}$
4. C_l includes probe and jig capacitance.
5. When testing the SN5400/SN7400 through SN5440/SN7440 (except SN5402/SN7402) connect all unused inputs to 2.4 V. When testing the SN5402/SN7402 or SN5450/SN7450 through SN5454/SN7454, apply the input pulse to one input of one AND section and 2.4 V to all unused inputs of that AND section. All inputs of unused AND sections are grounded.

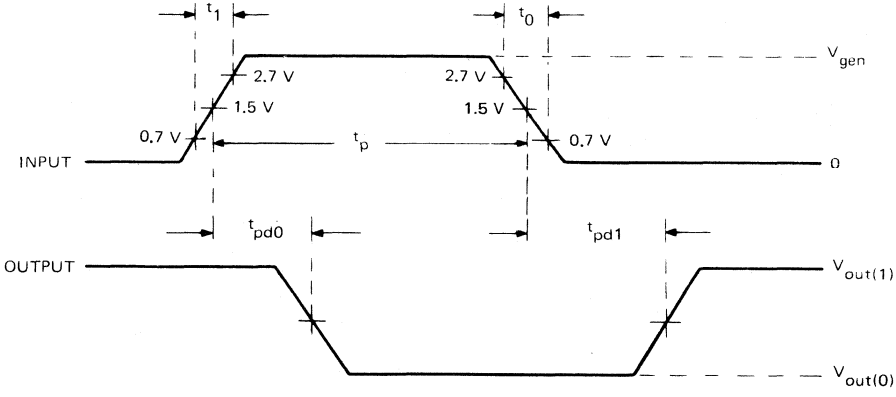
FIGURE 65-GATE PROPAGATION DELAY TIMES

PARAMETER MEASUREMENT INFORMATION

switching characteristics (continued)



TEST CIRCUIT



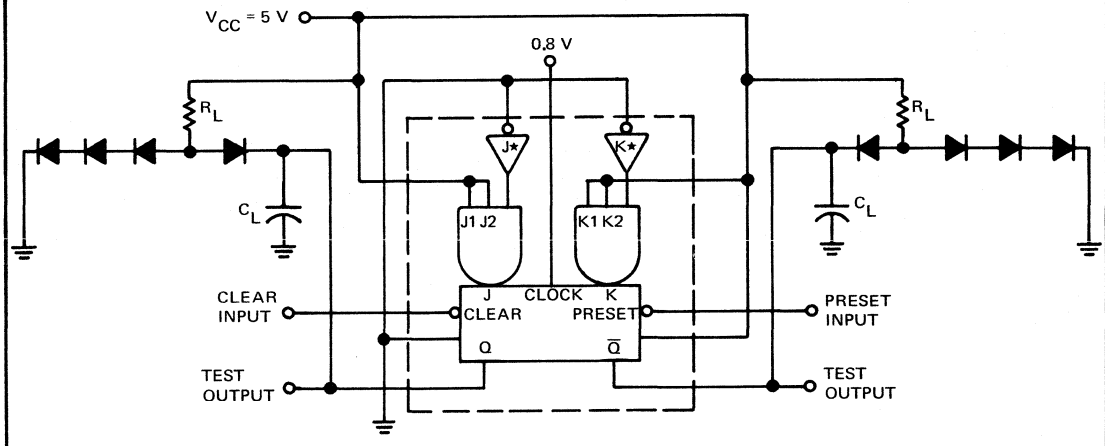
VOLTAGE WAVEFORMS

NOTES:
1. The generator has the following characteristics: V_{gen} = 3.5 V, t_0 = 5 ns, t_1 = 10 ns, t_p = 0.5 μs, PRR = 1 MHz, $Z_{out} \approx 50\ \Omega$.
2. All diodes are 1N3064.
3. $t_{pd} = \dfrac{t_{pd0} + t_{pd1}}{2}$
4. C_L includes probe and jig capacitance.

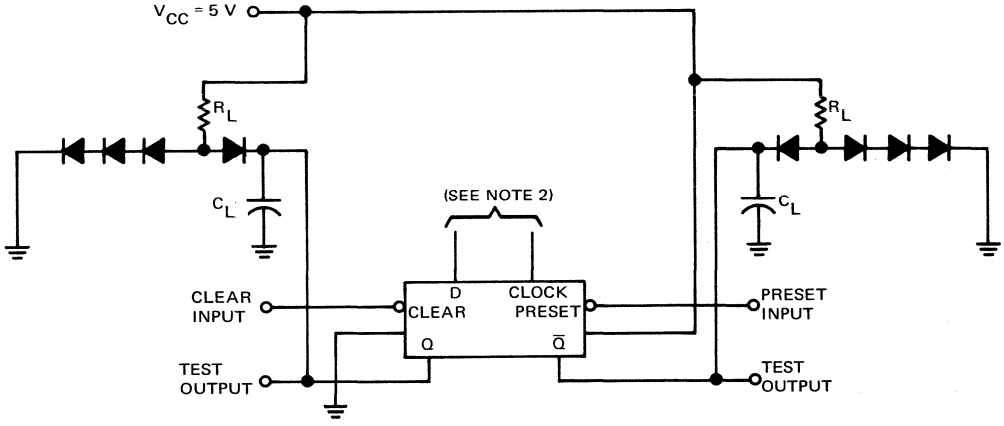
FIGURE 66–EXPANDER PROPAGATION DELAY TIMES

PARAMETER MEASUREMENT INFORMATION

switching characteristics (continued)



SN5470/SN7470 TEST CIRCUIT



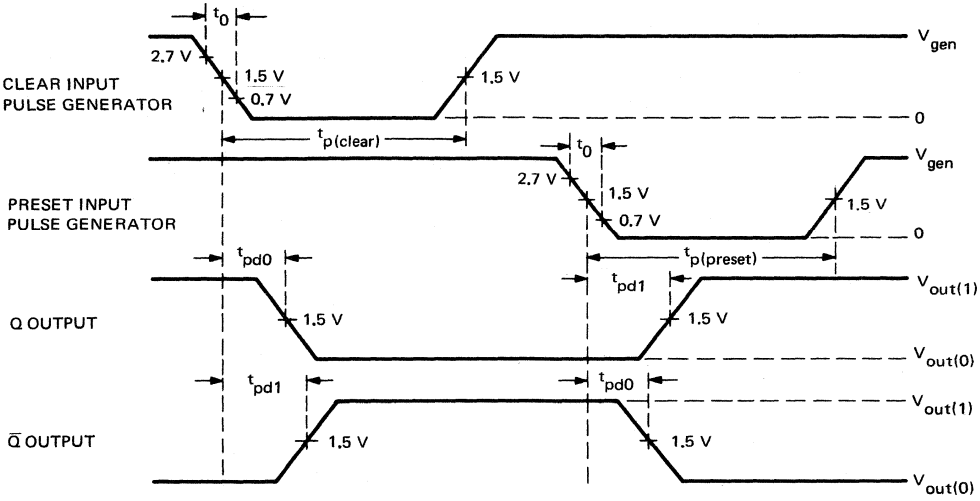
SN5474/SN7474 TEST CIRCUIT

NOTES:
1. Preset or clear function of the SN5470/SN7470 can occur only when clock input is low. Gated inputs are inhibited.
2. Clear and preset inputs of the SN5474/SN7474 dominate regardless of the state of clock or D inputs.
3. All diodes are 1N3064.
4. C_L includes probe and jig capacitance.

FIGURE 67–SN5470/SN7470 AND SN5474/SN7474 PRESET/CLEAR PROPAGATION DELAY TIMES (SHEET 1 OF 2)

PARAMETER MEASUREMENT INFORMATION

switching characteristics (continued)



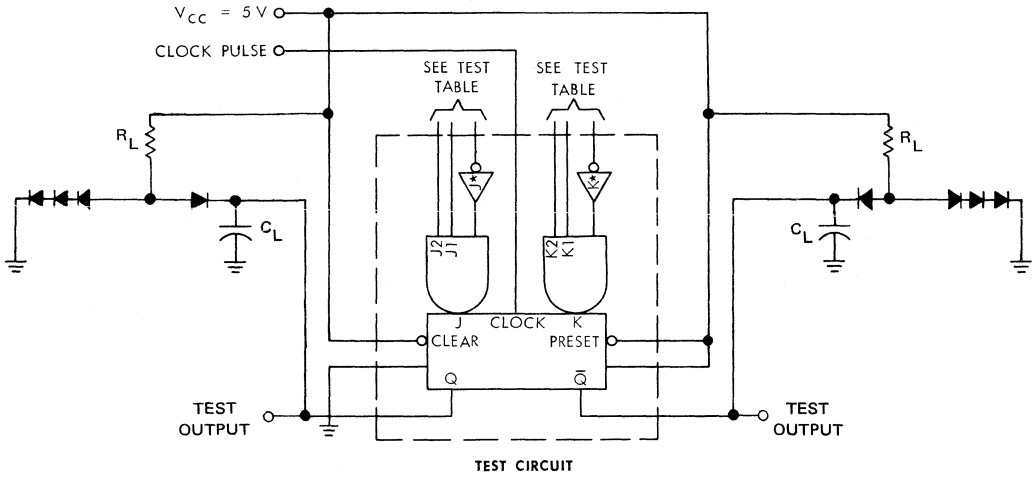
VOLTAGE WAVEFORMS

NOTE 6: Clear or preset input pulse characteristics: V_{gen} = 3.5 V, t_0 = 5 ns, t_p = 25 ns for the SN5470/SN7470, and t_p = 30 ns for SN5474/SN7474.

FIGURE 67–SN5470/SN7470 AND SN5474/SN7474 PRESET/CLEAR PROPAGATION DELAY TIMES (SHEET 2 OF 2)

PARAMETER MEASUREMENT INFORMATION

switching characteristics (continued)



TEST CIRCUIT

TEST TABLE					
TEST NO.	TEST	INPUT A	INPUT B	APPLY 2.4 V	GND
1	t_{setup} at J★	J★	None	J1, J2, K1, K2	K★
2	t_{hold} at J1, J2	None	J1, J2	K1, K2	J★ and K★
3	t_{setup} at K★	K★	None	J1, J2, K1, K2	J★
4	t_{hold} at K1, K2	None	K1, K2	J1, J2	J★ and K★

NOTES: 1. Clock pulse (see note 3), input A, and input B are used to measure t_{setup} and t_{hold}.

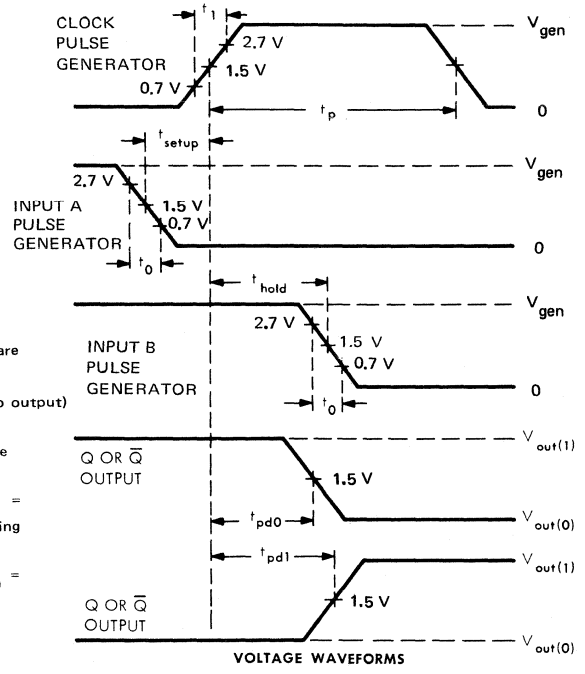
2. Clock frequency, t_{pd1}, and t_{pd0} (from clock to output) are measured in the toggle mode. Hold J = K = Logical 1 per truth table and apply clock pulse (see note 3).

3. Clock pulse characteristics: V_{gen} = 3.5 V, t_1 = 10 ns, t_p = 20 ns, and PRR = 1 MHz. When testing f_{clock}, vary PRR.

4. Input pulse characteristics: V_{gen} = 3.5 V, t_0 = 5 ns.

5. All diodes are 1N3064.

6. C_L includes probe and jig capacitance.

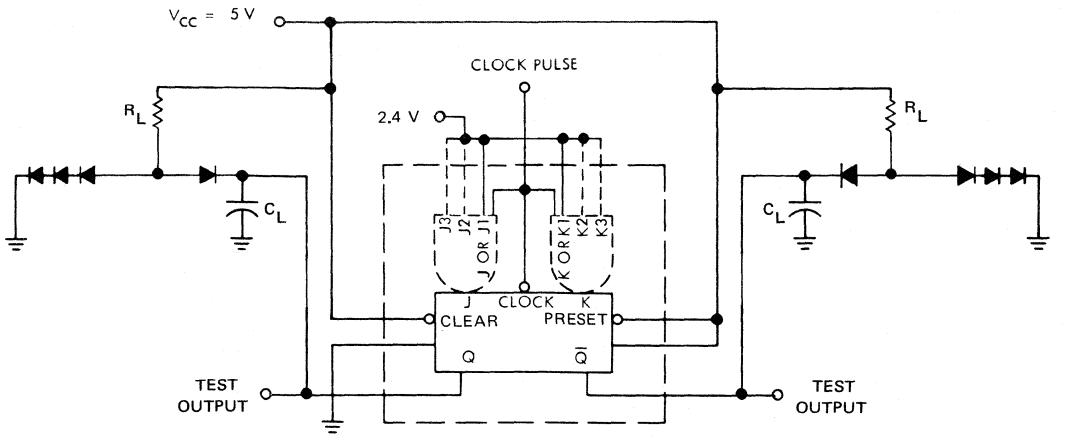


VOLTAGE WAVEFORMS

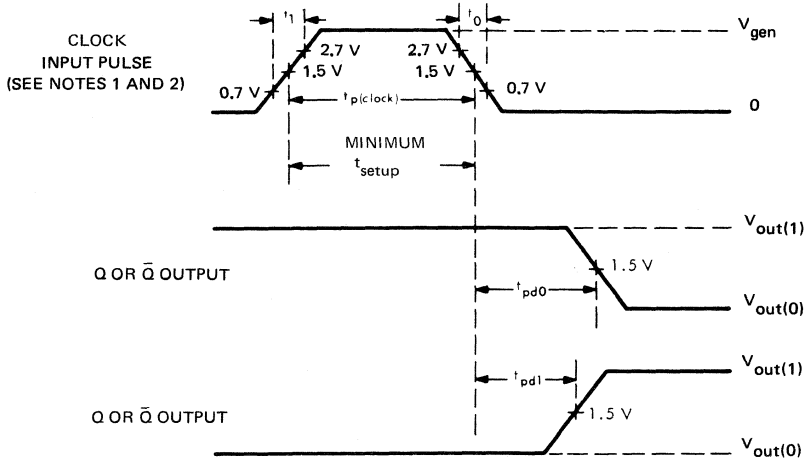
FIGURE 68—SN5470/SN7470 FLIP-FLOP SWITCHING TIMES

PARAMETER MEASUREMENT INFORMATION

switching characteristics (continued)



TEST CIRCUIT



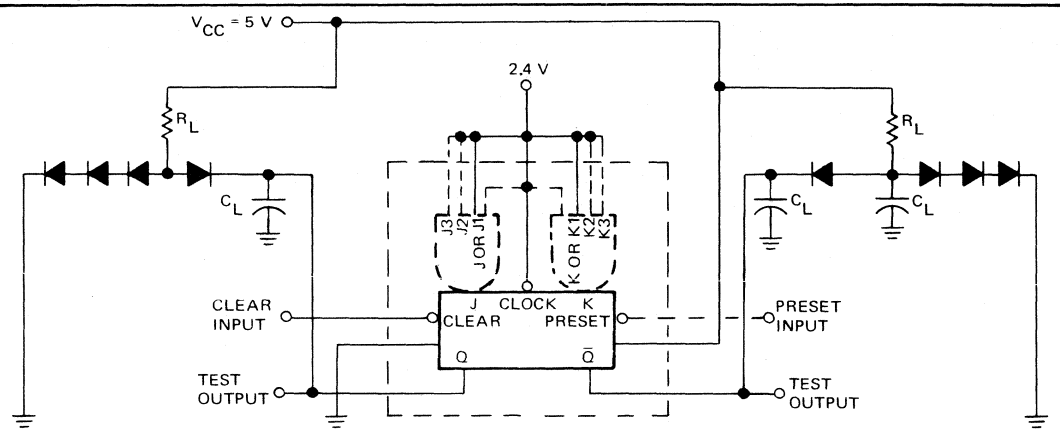
VOLTAGE WAVEFORMS

NOTES:
1. Clock, J, and K input pulse characteristics: V_{gen} = 3.5 V, t_0 = 5 ns, t_1 = 10 ns, t_p = 20 ns, and PRR = 1 MHz. When testing f_{clock}, vary PRR.
2. For the SN5472/SN7472, J = J1 • J2 • J3; and K = K1 • K2 • K3.
3. Gated inputs (shown with dotted lines) are for the SN5472/SN7472 only. The SN5473/SN7473, SN54107/SN74107 and SN5476/SN7476. Dual Flip-Flops have direct J and K inputs, and preset is not available on the SN5473/SN7473 and SN54107/SN74107.
4. All diodes are 1N3064.
5. C_L includes probe and jig capacitance.

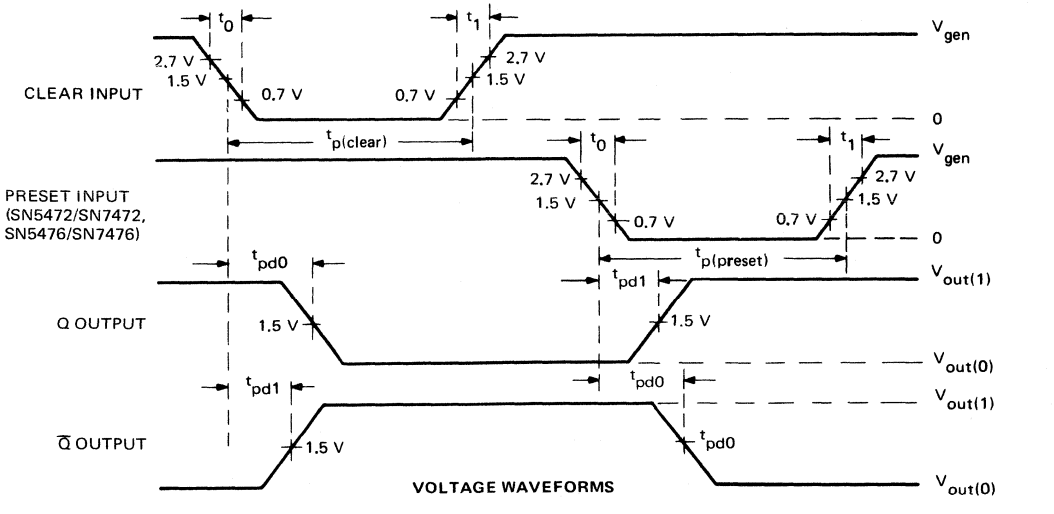
FIGURE 69–SN5472/SN7472, SN5473/SN7473, SN5476/SN7476, SN54107/SN74107 FLIP-FLOP SWITCHING TIMES

PARAMETER MEASUREMENT INFORMATION

switching characteristics (continued)



TEST CIRCUIT



VOLTAGE WAVEFORMS

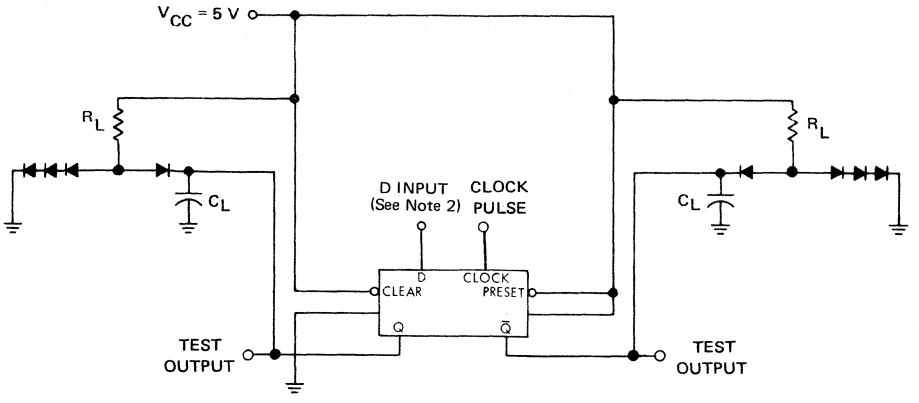
NOTES:

1. Clear or preset inputs dominate regardless of the state of clock or J-K inputs.
2. Clear or preset input pulse characteristics: V_{CC} = 3.5 V, t_0 = 5 ns, t_1 = 10 ns, $t_{p(clear)} = t_{p(preset)}$ = 25 ns, PRR = 1 MHz, and $Z_{out} \approx 50\ \Omega$.
3. Gates inputs (shown with dotted lines) are for the SN5472/SN7472 only. The SN5473/SN7473, SN5476/SN7476, and SN54107/SN74107 Dual Flip-Flops have direct J and K inputs, and preset is not available on the SN5473/SN7473 or SN54107/SN74107.
4. All diodes are 1N3064.
5. C_L includes probe and jig capacitance.

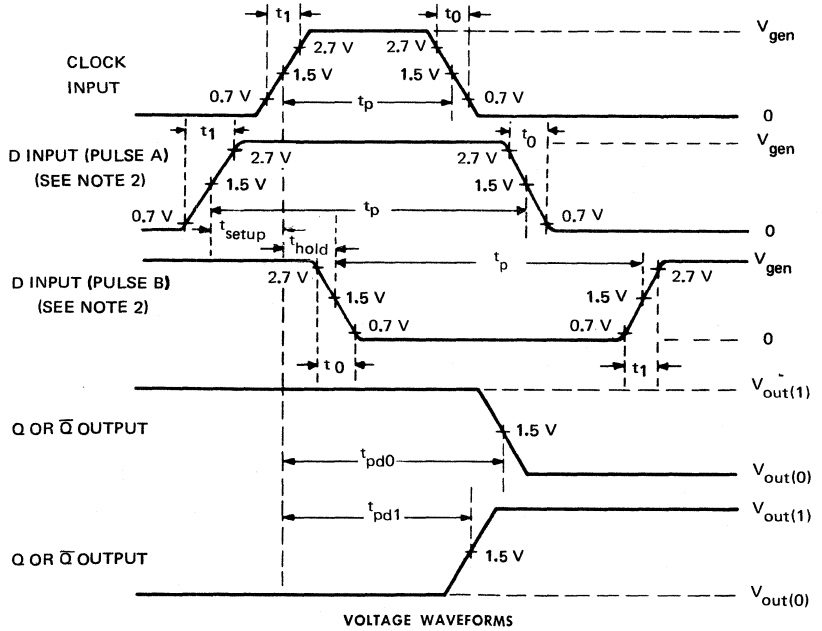
FIGURE 70–SN5472/SN7472, SN5473/SN7473, SN5476/SN7476, SN54107/SN74107 PRESET/CLEAR PROPAGATION DELAY TIMES

PARAMETER MEASUREMENT INFORMATION

switching characteristics (continued)



TEST CIRCUIT



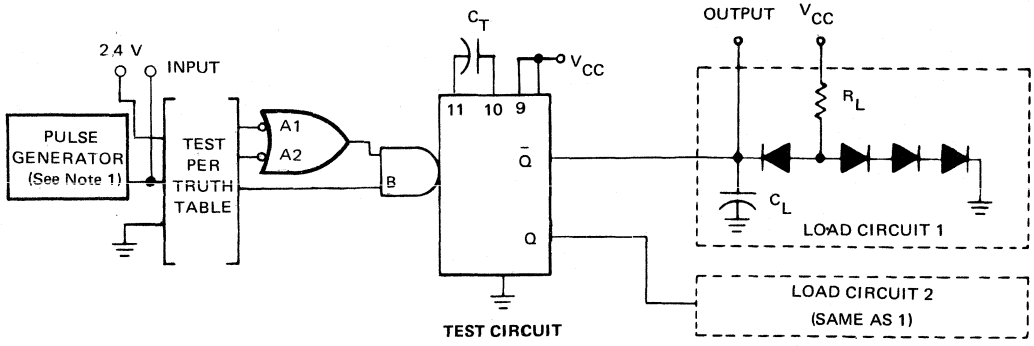
VOLTAGE WAVEFORMS

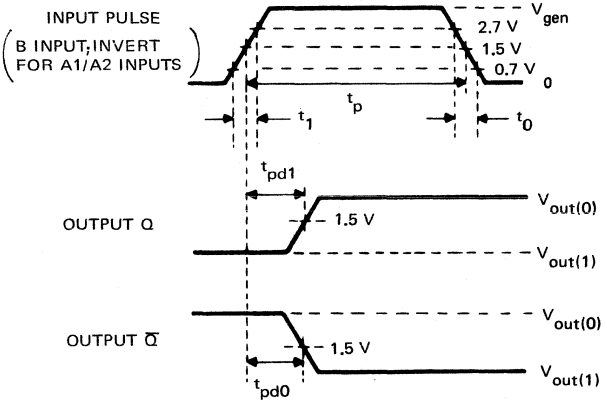
NOTES:
1. Clock input pulse has the following characteristics: V_{gen} = 3.5 V, t_0 = 5 ns, t_1 = 10 ns, t_p = 30 ns, and PRR = 1 MHz. When testing f_{clock}, vary PRR.
2. D input (pulse A) has the following characteristics: V_{gen} = 3.5 V, t_0 = 5 ns, t_1 = 10 ns, t_{setup} = 20 ns, t_p = 60 ns, and PRR is 50% of the clock PRR. D input (pulse B) has the following characteristics: V_{gen} = 3.5 V, t_0 = 5 ns, t_1 = 10 ns, t_{hold} = 5 ns, t_p = 60 ns, and PRR is 50% of the clock PRR.
3. All diodes are 1N3064.
4. C_L includes probe and jig capacitance.

FIGURE 71–SN5474/SN7474 FLIP-FLOP SWITCHING TIMES

PARAMETER MEASUREMENT INFORMATION

switching characteristics (continued)





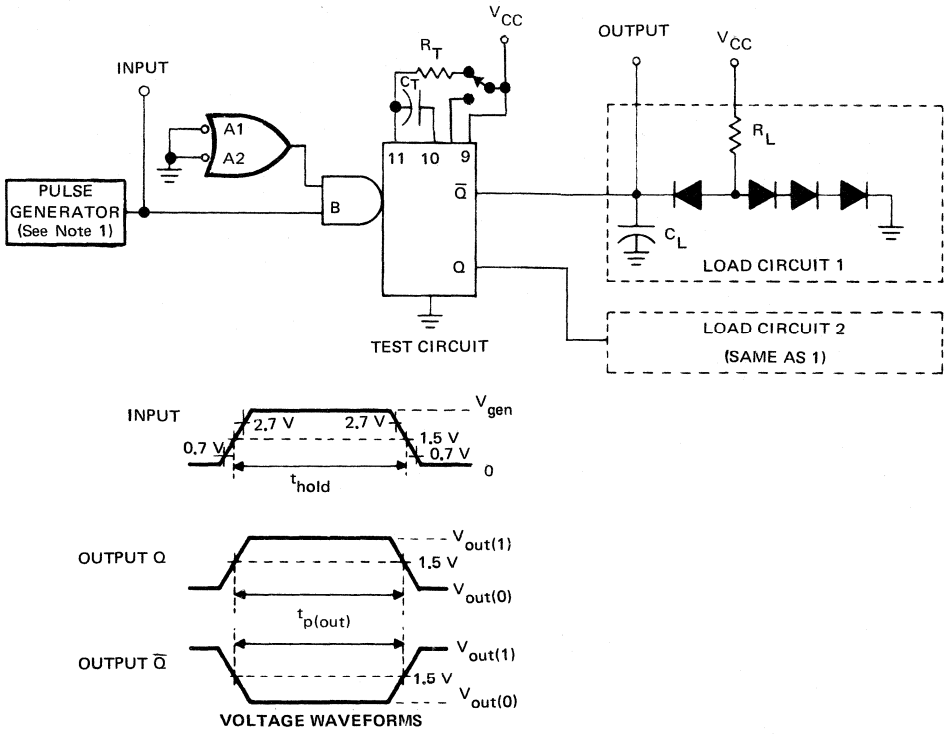
VOLTAGE WAVEFORMS

1. The pulse generator has the following characteristics: V_{gen} = 3.5 V, t_0 = 5 ns, t_1 = 10 ns, $t_p \geqslant 50$ ns, PRR = 1 MHz, and $Z_{out} \approx 50\ \Omega$.
2. All diodes are 1N3064.
3. C_L includes probe and jig capacitance.

FIGURE 72–SN54121/SN74121 SWITCHING TIMES

PARAMETER MEASUREMENT INFORMATION

switching characteristics (continued)

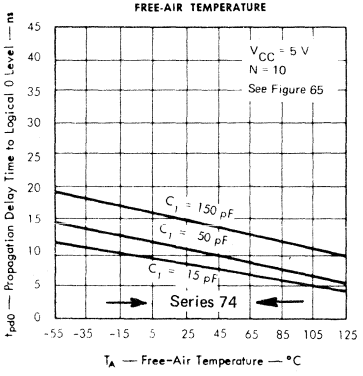


1. The pulse generator has the following characteristics: V_{gen} = 3.5 V, t_0 = 5 ns, t_1 = 10 ns, t_p = 50 ns, PRR = 1 MHz, and $Z_{out} \approx 50\ \Omega$.
2. All diodes are 1N3064.
3. C_L includes probe and jig capacitance.

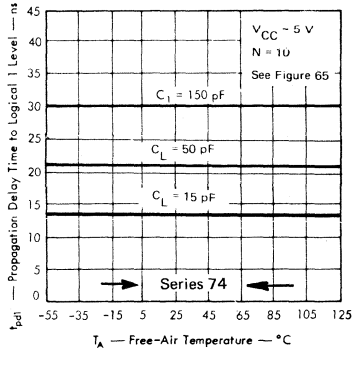
FIGURE 73—$t_{p(out)}$ (internal/minimum), t_{hold}

TYPICAL CHARACTERISTICS §

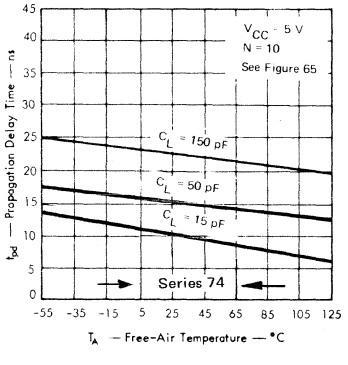
PROPAGATION DELAY TIME TO LOGICAL 0 LEVEL
vs
FREE-AIR TEMPERATURE



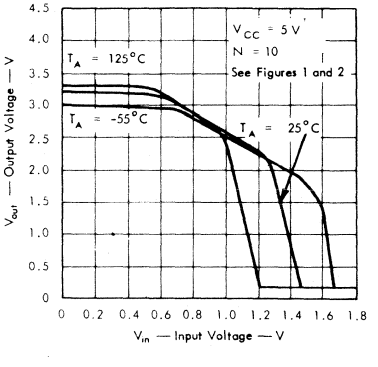
PROPAGATION DELAY TIME TO LOGICAL 1 LEVEL
vs
FREE-AIR TEMPERATURE



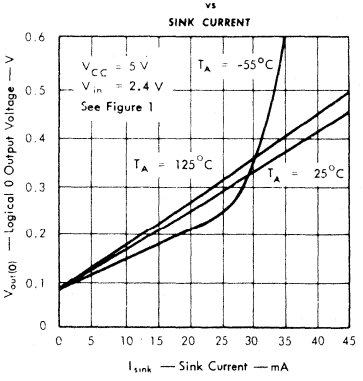
PROPAGATION DELAY TIME
vs
FREE-AIR TEMPERATURE



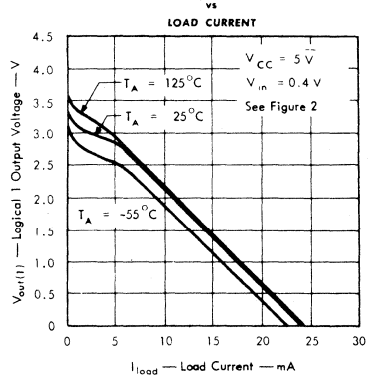
OUTPUT VOLTAGE
vs
INPUT VOLTAGE



LOGICAL 0 OUTPUT VOLTAGE
vs
SINK CURRENT



LOGICAL 1 OUTPUT VOLTAGE
vs
LOAD CURRENT



§Unless otherwise noted, data as shown is applicable for:SN5400, SN5402, SN5404, SN5410, SN5420, SN5430, SN5450, SN5451, SN5453, SN5454, SN7400, SN7402, SN7404, SN7410, SN7420, SN7430, SN7450, SN7451, SN7453, SN7454.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

SERIES 54H, 74H
HIGH-SPEED TRANSISTOR-TRANSISTOR LOGIC

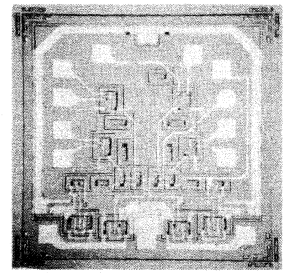
FOR GENERAL-PURPOSE DIGITAL SYSTEM APPLICATIONS

description

Series 54H and 74H TTL integrated circuits are designed to be used in systems where very-high-speed saturated logic and high d-c noise margins are required. Definitive specifications are provided for operating characteristics over the full military temperature range (−55°C to 125°C) and the industrial temperature range (0°C to 70°C). This logic series includes the gates and flip-flop elements needed to perform all functions within general-purpose digital systems.

Series 54H and 74H are completely compatible with Series 54 and 74 TTL logic families and circuits are designed to operate at the same supply voltages, logic levels, and high d-c noise margins which are characteristic of Series 54/74 TTL circuits. Series 54H/74H circuits feature a darlington-connected, double-ended, high-speed output for improved switching speeds. Typical flip-flop clock frequencies are 30 and 50 megahertz.

Since the Series 54H/ 74H circuits are compatible with other products in the TTL family, these higher-speed devices may be selectively used in system locations requiring minimal propagation delay times. In other locations where speed is not critical, Series 54/74 circuits may be used, thus minimizing total system power dissipation.



SN54H50 CIRCUIT BAR

Further flexibility is provided by the addition of noninverting AND and AND-OR functions to the Series 54H/74H line. This eliminates, in so far as possible, the need for extra packages and resultant wiring to perform mere signal-inverting functions. In addition to improving speed, the low impedance of the double-ended output rejects capacitively coupled a-c pulses, ensures waveshape integrity, and provides the necessary additional drive capability.

features

LOW SYSTEM COST

- **multifunction gates and dual flip-flops offer low cost per function**
- **special circuit types (AND and AND-OR functions) reduce system package count**

OPTIMUM CIRCUIT PERFORMANCE

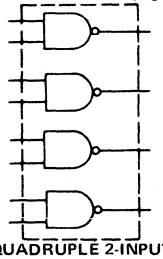
- **high speed — typical gate propagation delay times: 6 ns at $C_L = 25$ pF**
- **high d-c noise margin — typically one volt**
- **low output impedance provides low a-c noise susceptibility**
- **waveform integrity over full range of loading and temperature conditions**
- **power dissipation — typically 23 mW per NAND gate at 50% duty cycle**
- **fan-out — 10 Series 54H/74H loads or 12 Series 54/74 loads**
- **compatible with standard Series 54/74 logic circuits**

CONTENTS

standard line summary

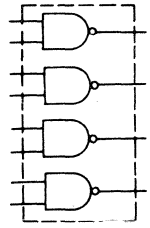
GATES

SN54H00
SN74H00 See page 3-5



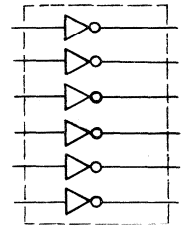
QUADRUPLE 2-INPUT POSITIVE NAND GATES

SN54H01
SN74H01 See page 3-6



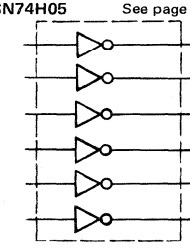
QUADRUPLE 2-INPUT POSITIVE NAND GATES (OPEN-COLLECTOR OUTPUT)

SN54H04
SN74H04 See page 3-9



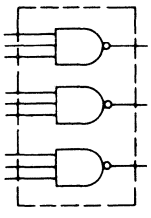
HEX INVERTERS

SN54H05
SN74H05 See page 3-10



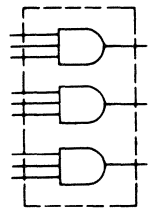
HEX INVERTERS (OPEN-COLLECTOR OUTPUT)

SN54H10
SN74H10 See page 3-11



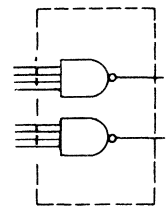
TRIPLE 3-INPUT POSITIVE NAND GATES

SN54H11
SN74H11 See page 3-12



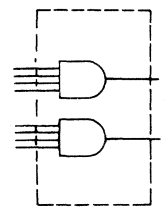
TRIPLE 3-INPUT POSITIVE AND GATES

SN54H20
SN74H20 See page 3-13



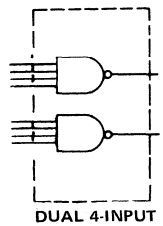
DUAL 4-INPUT POSITIVE NAND GATES

SN54H21
SN74H21 See page 3-14



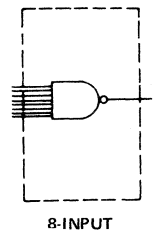
DUAL 4-INPUT POSITIVE AND GATES

SN54H22
SN74H22 See page 3-15



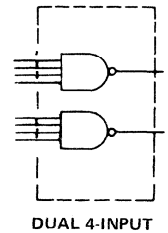
DUAL 4-INPUT POSITIVE NAND GATES (OPEN-COLLECTOR OUTPUT)

SN54H30
SN74H30 See page 3-16



8-INPUT POSITIVE NAND GATES

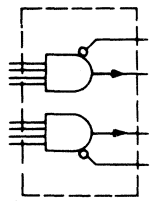
SN54H40
SN74H40 See page 3-17



DUAL 4-INPUT POSITIVE NAND BUFFERS

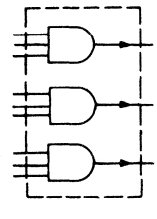
EXPANDERS

SN54H60
SN74H60 See page 3-26



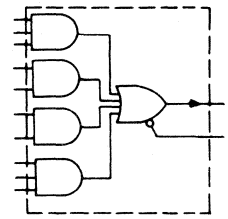
DUAL 4-INPUT EXPANDERS

SN54H61
SN74H61 See page 3-28



TRIPLE 3-INPUT EXPANDERS

SN54H62
SN74H62 See page 3-29



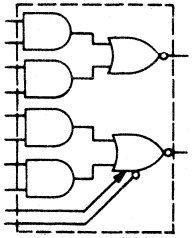
3-2-2-3-INPUT AND-OR EXPANDERS

SEE PAGES A-6 AND A-7

standard line summary (continued)

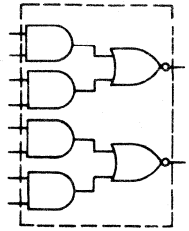
GATES

SN54H50
SN74H50 See page 3-18



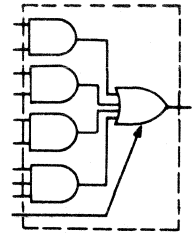
EXPANDABLE
DUAL 2-WIDE 2-INPUT
AND-OR-INVERT GATES

SN54H51
SN74H51 See page 3-18



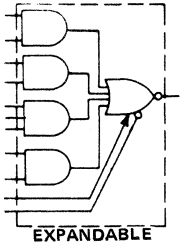
DUAL 2-WIDE 2-INPUT
AND-OR-INVERT GATES

SN54H52
SN74H52 See page 3-20



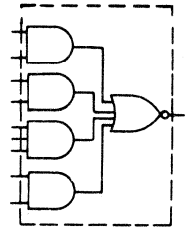
EXPANDABLE
2-2-2-3-INPUT AND-OR GATES

SN54H53
SN74H53 See page 3-22



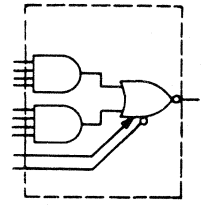
EXPANDABLE
2-2-2-3-INPUT
AND-OR-INVERT GATES

SN54H54
SN74H54 See Page 3-22



2-2-2-3-INPUT
AND-OR-INVERT GATES

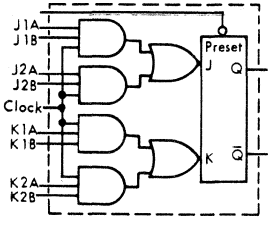
SN54H55
SN74H55 See page 3-24



EXPANDABLE 2-WIDE
4-INPUT
AND-OR-INVERT GATES

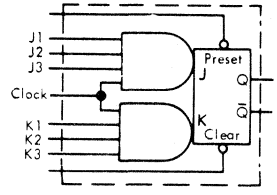
FLIP-FLOPS

SN54H71 (MASTER-SLAVE)
SN74H71 See page 3-31
SN54H101 (EDGE-TRIGGERED)
SN74H101 See page 3-46



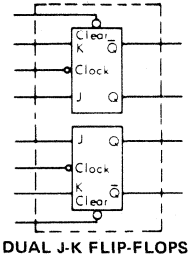
J-K FLIP-FLOPS

SN54H72 (MASTER-SLAVE)
SN74H72 See page 3-34
SN54H102 (EDGE-TRIGGERED)
SN74H102 See page 3-49



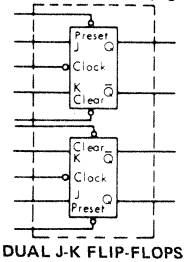
J-K FLIP-FLOPS

SN54H73 (MASTER-SLAVE)
SN74H73 See page 3-37
SN54H103 (EDGE-TRIGGERED)
SN74H103 See page 3-52



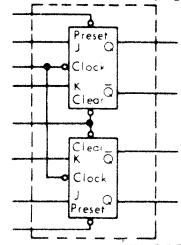
DUAL J-K FLIP-FLOPS

SN54H76 (MASTER-SLAVE)
SN74H76 See page 3-40
SN54H106 (EDGE-TRIGGERED)
SN74H106 See page 3-55



DUAL J-K FLIP-FLOPS

SN54H78 (MASTER-SLAVE)
SN74H78 See page 3-43
SN54H108 EDGE-TRIGGERED)
SN74H108 See page 3-58



DUAL J-K FLIP-FLOPS

FOR SUMMARY OF TTL MSI FUNCTIONS —

absolute amximum ratings over operating free-air temperature range (unless otherwise noted)

Supply Voltage V_{CC} (See Note 1)	7 V
Input Voltage, V_{in} (See Notes 1 and 2)	5.5 V
Operating Free-Air Temperature Range: Series 54H	−55°C to 125°C
Series 74H	0°C to 70°C
Storage Temperature Range	−65°C to 150°C

NOTES: 1. Voltage values are with respect to network ground terminal.
2. Input signals must be zero or positive with respect to network ground terminal.

logic definition

Series 54H and 74H logic is defined in terms of standard POSITIVE LOGIC using the following definitions:

LOW VOLTAGE = LOGICAL 0

HIGH VOLTAGE = LOGICAL 1

unused inputs

For optimum switching times and minimum noise susceptibility unused inputs should be maintained at a positive voltage greater than 2.4 V but not to exceed the absolute maximum rating of 5.5 V. This eliminates the distributed capacitance associated with the floating input-transistor emitter, bond wire, and package lead, and ensures that no degradation will occur in the propagation delay times. Some possible ways of handling input emitters are:

a. Connect unused inputs to an independent supply voltage. Preferably, this voltage should be between 2.4 V and 3.5 V.

b. Connect unused inputs to a used input if maximum fan-out of the driving output will not be exceeded. Each input presents a full load in the logical 1 state to the driving output.

c. Connect unused inputs to V_{CC} through a 1-kΩ resistor so that if a transient which exceeds the 5.5-V maximum rating should occur, the impedance will be high enough to protect the input. One to 25 unused inputs may be connected to each 1-kΩ resistor.

input-current requirements

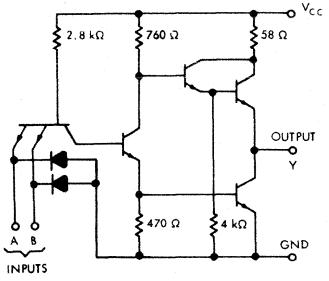
Input-current requirements reflect worst-case V_{CC} and temperature conditions. Each input of the multiple-emitter input transistors which has a 2.8-kΩ base resistor, requires no more than a 2-mA flow out of the input at a logical 0 voltage level; therefore, one load (N = 1) is −2 mA maximum. Each input requires current into the input at a logical 1 voltage level. This current is 50 μA maximum for each emitter of input transistors with the 2.8-kΩ base resistor. Currents into the input terminals are specified as positive values.

Inputs requiring current drive in excess of one normalized load are indicated by shading in the electrical characteristics tables.

fan-out capability

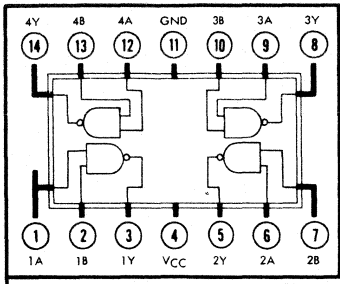
Fan-out (N) reflects the ability of an output to sink current from a number of Series 54H or 74H loads at a logical 0 voltage level and to supply current at a logical 1 voltage level. Each standard output is capable of sinking current or supplying current to 10 Series 54H or 74H loads (N=10) or 12 Series 54 or 74 loads. Load currents (out of the output terminal) are specified as negative values. See Section 12 for more detailed explanation of drive capabilities.

schematic (each gate)

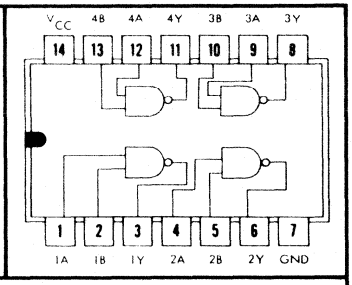


NOTE: Component values shown are nominal

S
FLAT PACKAGE (TOP VIEW)



J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



positive logic: $Y = \overline{AB}$

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply Voltage V_{CC}: SN54H00 Circuits	4.5	5	5.5	V
SN74H00 Circuits	4.75	5	5.25	V
Normalized Fan-Out From Each Output, N			10	
Operating Free-Air Temperature Range, T_A: SN54H00 Circuits	−55	25	125	°C
SN74H00 Circuits	0	25	70	°C

electrical characteristics (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS†	MIN	TYP §	MAX	UNIT
$V_{in(1)}$	Logical 1 input voltage required at all input terminals to ensure logical 0 level at output	1	V_{CC} = MIN	2			V
$V_{in(0)}$	Logical 0 input voltage required at any input terminal to ensure logical 1 level at output	2	V_{CC} = MIN			0.8	V
$V_{out(1)}$	Logical 1 output voltage	2	V_{CC} = MIN, V_{in} = 0.8 V, I_{load} = −500 μA	2.4			V
$V_{out(0)}$	Logical 0 output voltage	1	V_{CC} = MIN, V_{in} = 2 V, I_{sink} = 20 mA			0.4	V
$I_{in(0)}$	Logical 0 level input current (each input)	3	V_{CC} = MAX, V_{in} = 0.4 V			−2	mA
$I_{in(1)}$	Logical 1 level input current (each input)	4	V_{CC} = MAX, V_{in} = 2.4 V			50	μA
			V_{CC} = MAX, V_{in} = 5.5 V			1	mA
I_{OS}	Short-circuit output current‡	5	V_{CC} = MAX	−40		−100	mA
$I_{CC(0)}$	Logical 0 level supply current	6	V_{CC} = MAX, V_{in} = 4.5 V		26	40	mA
$I_{CC(1)}$	Logical 1 level supply current	6	V_{CC} = MAX, V_{in} = 0		10	16.8	mA

switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10

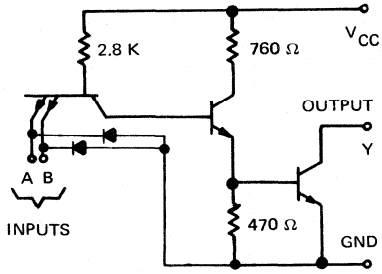
PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{pd0}	Propagation delay time to logical 0 level	74	C_L = 25 pF, R_L = 280 Ω		6.2	10	ns
t_{pd1}	Propagation delay time to logical 1 level	74	C_L = 25 pF, R_L = 280 Ω		5.9	10	ns

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
‡Not more than one output should be shorted at a time, and duration of short-circuit test should not exceed 1 second.
§ All typical values are at V_{CC} = 5 V, T_A = 25°C.

—SEE ORDERING INSTRUCTIONS PAGE 1-1—

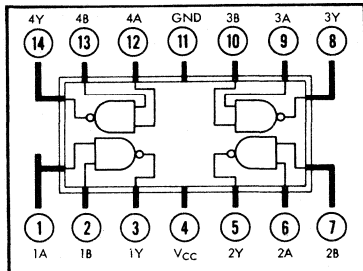
CIRCUIT TYPES SN54H01, SN74H01
QUADRUPLE 2-INPUT POSITIVE NAND GATES
(WITH OPEN-COLLECTOR OUTPUT)

schematic (each gate)

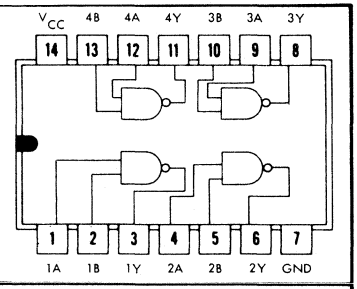


NOTE: Component values shown are nominal.

S
FLAT PACKAGE (TOP VIEW)



J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



positive logic: $Y = \overline{AB}$

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply Voltage V_{CC}: SN54H01 Circuits	4.5	5	5.5	V
SN74H01 Circuits	4.75	5	5.25	V
Normalized Fan-Out from Each Output, N (and see pages 3-7 and 3-8)			10	
Operating Free-Air Temperature Range: SN54H01 Circuits	−55	25	125	°C
SN74H01 Circuits	0	25	70	°C

electrical characteristics (over operating free-air temperature range unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS†	MIN	TYP§	MAX	UNIT
$V_{in(1)}$	Logical 1 input voltage required at both input terminals to ensure logical 0 (on) level at output	1	V_{CC} = MIN	2			V
$V_{in(0)}$	Logical 0 input voltage required at either input terminal to ensure logical 1 (off) level at output	7	V_{CC} = MIN			0.8	V
$I_{out(1)}$	Output reverse current	7	V_{CC} = MIN, V_{in} = 0.8 V, $V_{out(1)}$ = 5.5 V			250	μA
$V_{out(0)}$	Logical 0 output voltage (on level)	1	V_{CC} = MIN, V_{in} = 2 V, I_{sink} = 20 mA			0.4	V
$I_{in(0)}$	Logical 0 level input current (each input)	3	V_{CC} = MAX, V_{in} = 0.4 V			−2	mA
$I_{in(1)}$	Logical 1 level input current (each input)	4	V_{CC} = MAX, V_{in} = 2.4 V			50	μA
			V_{CC} = MAX, V_{in} = 5.5 V			1	mA
$I_{CC(0)}$	Logical 0 level supply current	6	V_{CC} = MAX, V_{in} = 4.5 V		26	40	mA
$I_{CC(1)}$	Logical 1 level supply current	6	V_{CC} = MAX, V_{in} = 0		6.8	10	mA

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{pd0}	Propagation delay time to logical 0 level	74	C_L = 25 pF, R_L = 280 Ω		7.5	12	ns
t_{pd1}	Propagation delay time to logical 1 level	74	C_L = 25 pF, R_L = 280 Ω		10	15	ns

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

§ All typical values are at V_{CC} = 5 V, T_A = 25°C.

—SEE ORDERING INSTRUCTIONS PAGE 1-1—

combined fan-out and wire-OR capabilities

The open-collector TTL gate, when supplied with a proper load resistor (R_L), may be paralleled with other similar TTL gates to perform the wire-OR function and simultaneously, will drive from one to nine 54H or 74H loads. When no other open-collector gates are paralleled, this gate may be used to drive ten 54H or 74H loads. For any of these conditions an appropriate load-resistor value must be determined for the desired circuit configuration. A maximum resistor value must be determined which will ensure that sufficient load current (to loads) and I_{off} current (through paralleled outputs) will be available during a logical 1 level at the output. A minimum resistor value must be determined which will ensure that current through this resistor and sink current from the loads will not cause the output voltage to rise above the logical 0 level even if one of the paralleled outputs is sinking all the current.

In both conditions (logical 0 and logical 1) the value of R_L is determined by:

$$R_L = \frac{V_{RL}}{I_{RL}}$$

Where: V_{RL} is voltage drop in volts, and I_{RL} is the current in amperes.

logical 1 (off level) circuit calculations (see figure A)

The allowable voltage drop across the load resistor (V_{RL}) is the difference between V_{CC} applied and the $V_{out(1)}$ level required at the load:

$$V_{RL} = V_{CC} - V_{out(1)\ required}$$

The total current through the load resistor (I_{RL} is the sum of the load currents ($I_{in(1)}$) and off-level reverse currents ($I_{out(1)}$) through each of the wire-OR connected outputs:

$$I_{RL} = \eta \cdot I_{out(1)} + N \cdot I_{in(1)} \text{ to loads}$$

Therefore, calculations for the maximum value of R_L would be:

$$R_{L(max)} = \frac{V_{CC} - V_{out(1)\ required}}{\eta \cdot I_{out(1)} + N \cdot I_{in(1)}}$$

Where: η = number of gates wire-OR connected, and N = number of 54H/74H loads.

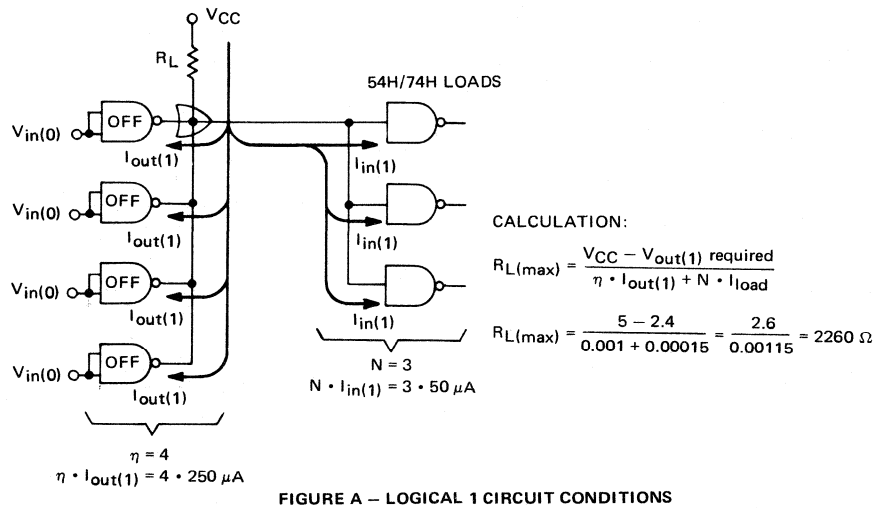


FIGURE A – LOGICAL 1 CIRCUIT CONDITIONS

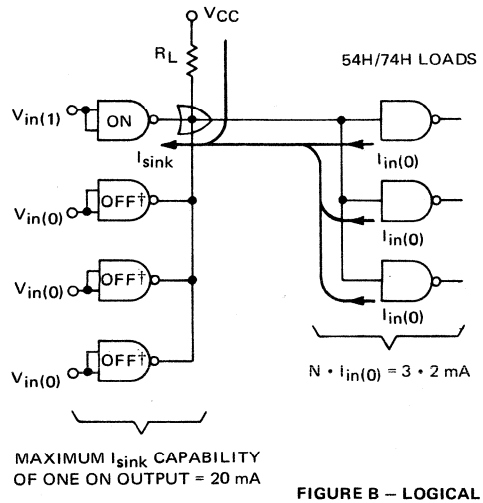
logical 0 (on level) circuit calculations (see figure B)

The current through the resistor must be limited to the maximum sink-current capability of one output transistor. Note that if several output transistors are wire-OR connected, the current through R_L may be shared by those paralleled transistors. However, unless it can be absolutely guaranteed that more than one transistor will be on during logical 0 periods, the current must be limited to 20 mA, the maximum current which will ensure a logical 0 maximum of 0.4 volts.

Also, fan-out must be considered. Part of the 20 mA will be supplied from the inputs which are being driven. This reduces the amount of current which can be allowed through R_L.

Therefore, the equation used to determine the minimum value of R_L would be:

$$R_{L(min)} = \frac{V_{CC} - V_{out(0)\ required}}{I_{sink\ capability} - I_{sink\ from\ loads}}$$



CALCULATION:

$$R_{L(min)} = \frac{V_{CC} - V_{out(0)\ required}}{I_{sink\ capability} - I_{sink\ from\ TTL\ loads}}$$

$$R_{L(min)} = \frac{5 - 0.4}{0.02 - 0.006} = \frac{4.6}{0.014} = 323\ \Omega$$

†Current through OFF outputs is negligible at logical 0.

FIGURE B – LOGICAL 0 CIRCUIT CONDITIONS

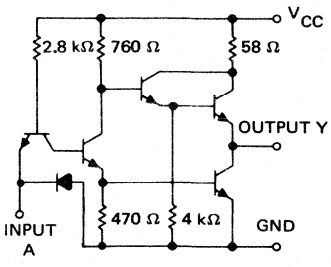
Table I provides minimum and maximum resistor values, calculated from equations shown above, for driving one to ten 54H/74H loads and wire-OR connecting two to seven parallel outputs. Each value shown for one wire-OR output is determined by the fan-out plus the cutoff current of a single output transistor. Extension beyond seven wire-OR connections is permitted with fan-outs of seven or less if a valid minimum and maximum R_L is possible. Fastest rise times are obtained when $R_{L(min)}$ is used. When fanning-out to ten 54H/74H loads, the calculation for the minimum value of R_L indicates that an infinite resistance should be used ($V_{RL} \div 0 = \infty$); however, the use of a 3466 Ω resistor in this case will satisfy the logical 1 condition and limit the logical 0 voltage level to less than 0.42 V.

FAN-OUT TO 54H/74H LOADS	WIRE-OR OUTPUTS							
	1	2	3	4	5	6	7	1 to 7
1	8666	4727	3250	2476	2000	1677	1444	255
2	7428	4333	3058	2363	1925	1625	1405	288
3	6500	4000	2888	2260	1857	1575	1368	323
4	5777	3714	2736	2166	1793	1529	1333	384
5	5200	3466	2600	2080	1733	1485	1300	460
6	4727	3250	2476	2000	1677	1444	1268	578
7	4333	3058	2363	1925	1625	1405	1238	767
8	4000	2888	2260	1857	1575	1368	1209	1150
9	3714	2736	X	X	X	X	X	2300
10	3466	X	X	X	X	X	X	3466‡
	MAXIMUM							MIN
	LOAD RESISTOR VALUE IN OHMS							

X – Not recommended or not possible.
‡ – The theoretical value is ∞. See explanation in text.
All values shown in the table are based on:
Logical 1 conditions: V_{CC} = 5 V, $V_{out(1)}$ required = 2.4 V
Logical 0 conditions: V_{CC} = 5 V, $V_{out(0)}$ required = 0.4 V

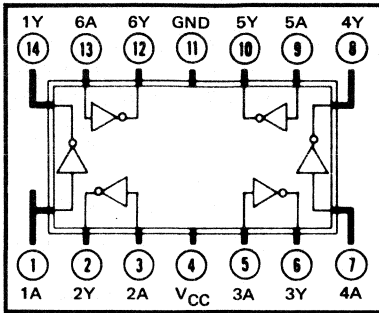
TABLE I – LOAD RESISTOR VALUES

schematic (each inverter)

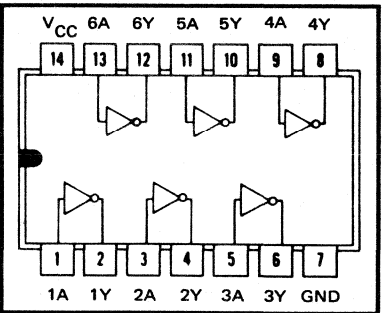


Component values shown are normal

S
FLAT PACKAGE (TOP VIEW)



J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



positive logic: $Y = \overline{A}$

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply Voltage V_{CC}: SN54H04 Circuits	4.5	5	5.5	V
SN74H04 Circuits	4.75	5	5.25	V
Normalized Fan-Out From Each Output, N			10	
Operating Free-Air Temperature Range, T_A: SN54H04 Circuits	−55	25	125	°C
SN74H04 Circuits	0	25	70	°C

electrical characteristics (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS†	MIN	TYP§	MAX	UNIT
$V_{in(1)}$	Logical 1 input voltage required at input terminal to ensure logical 0 level at output	8	V_{CC} = MIN	2			V
$V_{in(0)}$	Logical 0 input voltage required at input terminal to ensure logical 1 level at output	9	V_{CC} = MIN			0.8	V
$V_{out(1)}$	Logical 1 output voltage	9	V_{CC} = MIN, V_{in} = 0.8 V, I_{load} = −500 μA	2.4			V
$V_{out(0)}$	Logical 0 output voltage	8	V_{CC} = MIN, V_{in} = 2 V, I_{sink} = 20 mA			0.4	V
$I_{in(0)}$	Logical 0 level input current	10	V_{CC} = MAX, V_{in} = 0.4 V			−2	mA
$I_{in(1)}$	Logical 1 level input current	11	V_{CC} = MAX, V_{in} = 2.4 V			50	μA
			V_{CC} = MAX, V_{in} = 5.5 V			1	mA
I_{OS}	Short-circuit output current‡	12	V_{CC} = MAX	−40		−100	mA
$I_{CC(0)}$	Logical 0 level supply current	13	V_{CC} = MAX, V_{in} = 4.5 V		40	58	mA
$I_{CC(1)}$	Logical 1 level supply current	13	V_{CC} = MAX, V_{in} = 0		16	26	mA

switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{pd0}	Propagation delay time to logical 0 level	74	C_L = 25 pF, R_L = 280 Ω		6.5	10	ns
t_{pd1}	Propagation delay time to logical 1 level	74	C_L = 25 pF, R_L = 280 Ω		9	13	ns

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

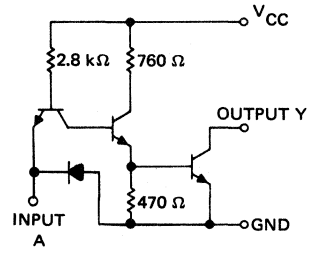
‡ Not more than one output should be shorted at a time, and duration of short-circuit test should not exceed 1 second.

§ All typical values are at V_{CC} = 5 V, T_A = 25°C.

—SEE ORDERING INSTRUCTIONS PAGE 1-1—

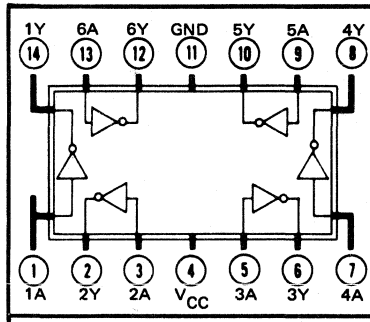
CIRCUIT TYPES SN54H05, SN74H05
HEX INVERTERS (WITH OPEN-COLLECTOR OUTPUT)

schematic (each inverter)

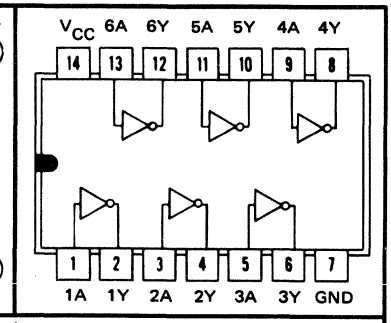


Component values shown are normal

S
FLAT PACKAGE (TOP VIEW)



J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



positive logic: $Y = \overline{A}$

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply Voltage V_{CC}: SN54H05 Circuits	4.5	5	5.5	V
SN74H05 Circuits	4.75	5	5.25	V
Normalized Fan-Out From Each Output, N (and see pages 3-7 and 3-8)			10	
Operating Free-Air Temperature Range, T_A: SN54H05 Circuits	−55	25	125	°C
SN74H05 Circuits	0	25	70	°C

electrical characteristics (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS†	MIN	TYP§	MAX	UNIT
$V_{in(1)}$	Logical 1 input voltage required at input terminal to ensure logical 0 (on) level at output	8	V_{CC} = MIN	2			V
$V_{in(0)}$	Logical 0 input voltage required at input terminal to ensure logical 1 (off) level at output	9	V_{CC} = MIN			0.8	V
$I_{out(1)}$	Output reverse current	9	V_{CC} = MIN, V_{in} = 0.8 V, $V_{out(1)}$ = 5.5 V			250	μA
$V_{out(0)}$	Logical 0 output voltage (on level)	8	V_{CC} = MIN, V_{in} = 2 V, I_{sink} = 20 mA			0.4	V
$I_{in(0)}$	Logical 0 level input current	10	V_{CC} = MAX, V_{in} = 0.4 V			−2	mA
$I_{in(1)}$	Logical 1 level input current	11	V_{CC} = MAX, V_{in} = 2.4 V			50	μA
			V_{CC} = MAX, V_{in} = 5.5 V			1	mA
$I_{CC(0)}$	Logical 0 level supply current	13	V_{CC} = MAX, V_{in} = 4.5 V		40	58	mA
$I_{CC(1)}$	Logical 1 level supply current	13	V_{CC} = MAX, V_{in} = 0		16	26	mA

switching characteristics, V_{CC} = 5 V, T_A = 25°C

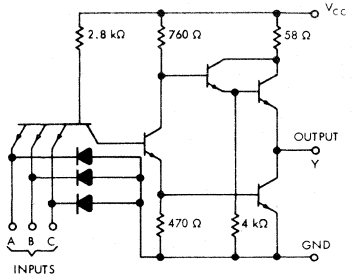
PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{pd0}	Propagation delay time to logical 0 level	74	C_L = 25 pF, R_L = 280 Ω		10	15	ns
t_{pd1}	Propagation delay time to logical 1 level	74	C_L = 25 pF, R_L = 280 Ω		13	18	ns

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

§ All typical values are at V_{CC} = 5 V, T_A = 25°C.

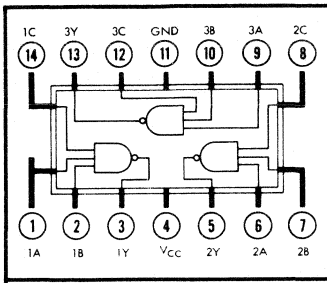
—SEE ORDERING INSTRUCTIONS PAGE 1-1—

schematic (each gate)

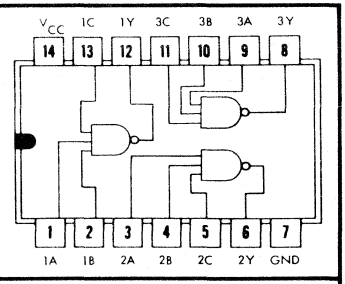


NOTE: Component values shown are nominal

S
FLAT PACKAGE (TOP VIEW)



J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



positive logic: $Y = \overline{ABC}$

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply Voltage V_{CC}: SN54H10 Circuits	4.5	5	5.5	V
SN74H10 Circuits	4.75	5	5.25	V
Normalized Fan-Out From Each Output, N			10	
Operating Free-Air Temperature Range, T_A: SN54H10 Circuits	−55	25	125	°C
SN74H10 Circuits	0	25	70	°C

electrical characteristics (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS†	MIN	TYP §	MAX	UNIT
$V_{in(1)}$	Logical 1 input voltage required at all input terminals to ensure logical 0 level at output	1	V_{CC} = MIN	2			V
$V_{in(0)}$	Logical 0 input voltage required at any input terminal to ensure logical 1 level at output	2	V_{CC} = MIN			0.8	V
$V_{out(1)}$	Logical 1 output voltage	2	V_{CC} = MIN, V_{in} = 0.8 V, I_{load} = −500 μA	2.4			V
$V_{out(0)}$	Logical 0 output voltage	1	V_{CC} = MIN, V_{in} = 2 V, I_{sink} = 20 mA			0.4	V
$I_{in(0)}$	Logical 0 level input current (each input)	3	V_{CC} = MAX, V_{in} = 0.4 V			−2	mA
$I_{in(1)}$	Logical 1 level input current (each input)	4	V_{CC} = MAX, V_{in} = 2.4 V			50	μA
			V_{CC} = MAX, V_{in} = 5.5 V			1	mA
I_{OS}	Short-circuit output current‡	5	V_{CC} = MAX	−40		−100	mA
$I_{CC(0)}$	Logical 0 level supply current	6	V_{CC} = MAX, V_{in} = 4.5 V		19.5	30	mA
$I_{CC(1)}$	Logical 1 level supply current	6	V_{CC} = MAX, V_{in} = 0		7.5	12.6	mA

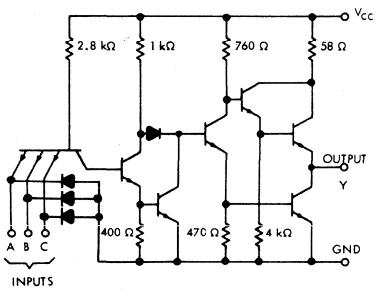
switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{pd0}	Propagation delay time to logical 0 level	74	C_L = 25 pF, R_L = 280 Ω		6.3	10	ns
t_{pd1}	Propagation delay time to logical 1 level	74	C_L = 25 pF, R_L = 280 Ω		5.9	10	ns

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
‡Not more than one output should be shorted at a time, and duration of short-circuit test should not exceed 1 second.
§ All typical values are at V_{CC} = 5 V, T_A = 25°C.

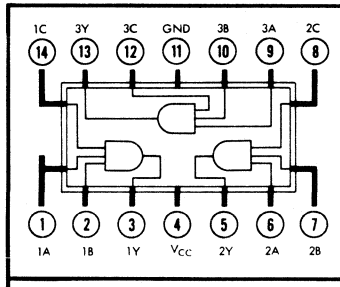
CIRCUIT TYPES SN54H11, SN74H11
TRIPLE 3-INPUT POSITIVE AND GATES

schematic (each gate)

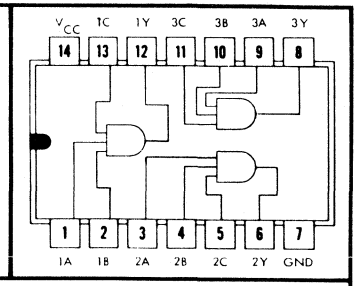


NOTE: Component values shown are nominal

S
FLAT PACKAGE (TOP VIEW)



J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



positive logic: Y = ABC

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply Voltage V_{CC}: SN54H11 Circuits	4.5	5	5.5	V
SN74H11 Circuits	4.75	5	5.25	V
Normalized Fan-Out From Each Output, N			10	
Operating Free-Air Temperature Range, T_A: SN54H11 Circuits	−55	25	125	°C
SN74H11 Circuits	0	25	70	°C

electrical characteristics (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS†	MIN	TYP §	MAX	UNIT
$V_{in(1)}$	Logical 1 input voltage required at all input terminals to ensure logical 1 level at output	14	V_{CC} = MIN	2			V
$V_{in(0)}$	Logical 0 input voltage required at any input terminal to ensure logical 0 level at output	15	V_{CC} = MIN			0.8	V
$V_{out(1)}$	Logical 1 output voltage	14	V_{CC} = MIN, $V_{in(1)}$ = 2 V, I_{load} = −500 μA	2.4			V
$V_{out(0)}$	Logical 0 output voltage	15	V_{CC} = MIN, $V_{in(0)}$ = 0.8 V, I_{sink} = 20 mA			0.4	V
$I_{in(0)}$	Logical 0 level input current (each input)	16	V_{CC} = MAX, V_{in} = 0.4 V			−2	mA
$I_{in(1)}$	Logical 1 level input current (each input)	17	V_{CC} = MAX, V_{in} = 2.4 V			50	μA
			V_{CC} = MAX, V_{in} = 5.5 V			1	mA
I_{OS}	Short-circuit output current‡	18	V_{CC} = MAX, V_{in} = 4.5 V	−40		−100	mA
$I_{CC(0)}$	Logical 0 level supply current	19	V_{CC} = MAX, V_{in} = 0		30	48	mA
$I_{CC(1)}$	Logical 1 level supply current	19	V_{CC} = MAX, V_{in} = 4.5 V		18	30	mA

switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{pd0}	Propagation delay time to logical 0 level	74	C_L = 25 pF, R_L = 280 Ω		8.8	12	ns
t_{pd1}	Propagation delay time to logical 1 level	74	C_L = 25 pF, R_L = 280 Ω		7.6	12	ns

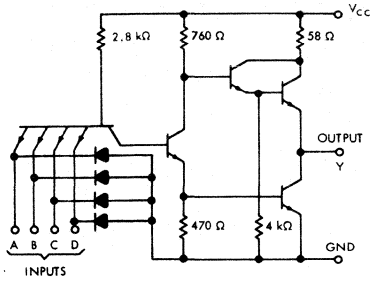
†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

‡Not more than one output should be shorted at a time, and duration of short-circuit test should not exceed 1 second.

§ All typical values are at V_{CC} = 5 V, T_A = 25°C.

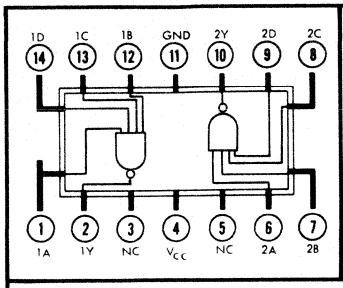
–SEE ORDERING INSTRUCTIONS PAGE 1-1–

schematic (each gate)

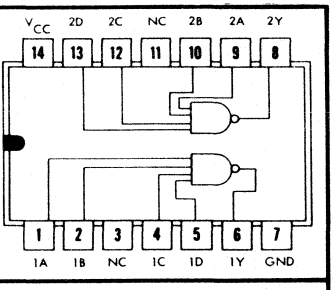


NOTES: 1. Component values shown are nominal
2. NC — No internal connection

S
FLAT PACKAGE (TOP VIEW)



J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



positive logic: $Y = \overline{ABCD}$

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply Voltage V_{CC}: SN54H20 Circuits	4.5	5	5.5	V
SN74H20 Circuits	4.75	5	5.25	V
Normalized Fan-Out From Each Output, N			10	
Operating Free-Air Temperature Range, T_A: SN54H20 Circuits	−55	25	125	°C
SN74H20 Circuits	0	25	70	°C

electrical characteristics (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS†	MIN	TYP§	MAX	UNIT
$V_{in(1)}$	Logical 1 input voltage required at all input terminals to ensure logical 0 output voltage	1	V_{CC} = MIN	2			V
$V_{in(0)}$	Logical 0 input voltage required at any input terminal to ensure logical 1 level at output	2	V_{CC} = MIN			0.8	V
$V_{out(1)}$	Logical 1 output voltage	2	V_{CC} = MIN, V_{in} = 0.8 V, I_{load} = −500 μA	2.4			V
$V_{out(0)}$	Logical 0 output voltage	1	V_{CC} = MIN, V_{in} = 2 V, I_{sink} = 20 mA			0.4	V
$I_{in(0)}$	Logical 0 level input current (each input)	3	V_{CC} = MAX, V_{in} = 0.4 V			−2	mA
$I_{in(1)}$	Logical 1 level input current (each input)	4	V_{CC} = MAX, V_{in} = 2.4 V			50	μA
			V_{CC} = MAX, V_{in} = 5.5 V			1	mA
I_{OS}	Short-circuit output current‡	5	V_{CC} = MAX	−40		−100	mA
$I_{CC(0)}$	Logical 0 level supply current	6	V_{CC} = MAX, V_{in} = 4.5 V		13	20	mA
$I_{CC(1)}$	Logical 1 level supply current	6	V_{CC} = MAX, V_{in} = 0		5	8.4	mA

switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10

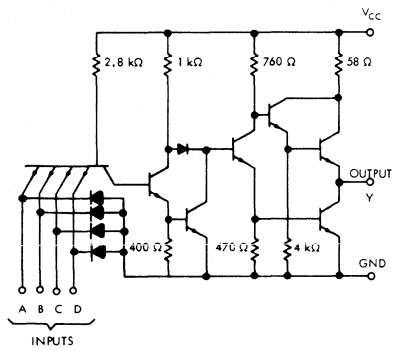
PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{pd0}	Propagation delay time to logical 0 level	74	C_L = 25 pF, R_L = 280 Ω		7	10	ns
t_{pd1}	Propagation delay time to logical 1 level	74	C_L = 25 pF, R_L = 280 Ω		6	10	ns

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
‡Not more than one output should be shorted at a time, and duration of short-circuit test should not exceed 1 second.
§All typical values are at V_{CC} = 5 V, T_A = 25°C.

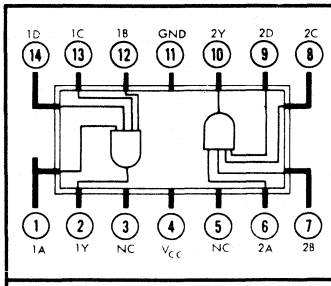
—SEE ORDERING INSTRUCTIONS PAGE 1-1—

CIRCUIT TYPES SN54H21, SN74H21
DUAL 4-INPUT POSITIVE AND GATES

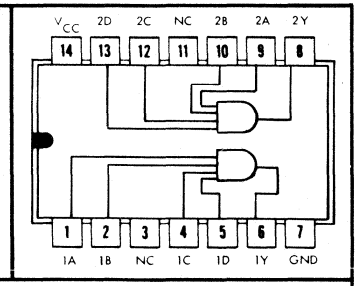
schematic (each gate)



S
FLAT PACKAGE (TOP VIEW)



J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



positive logic: Y = ABCD

NOTES: 1. Component values shown are nominal
2. NC — No internal connection

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply Voltage V_{CC}: SN54H21 Circuits	4.5	5	5.5	V
SN74H21 Circuits	4.75	5	5.25	V
Normalized Fan-Out From Each Output, N			10	
Operating Free-Air Temperature Range, T_A: SN54H21 Circuits	−55	25	125	°C
SN74H21 Circuits	0	25	70	°C

electrical characteristics (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS†	MIN	TYP §	MAX	UNIT
$V_{in(1)}$	Logical 1 input voltage required at all input terminals to ensure logical 1 level at output	14	V_{CC} = MIN	2			V
$V_{in(0)}$	Logical 0 input voltage required at any input terminal to ensure logical 0 level at output	15	V_{CC} = MIN			0.8	V
$V_{out(1)}$	Logical 1 output voltage	14	V_{CC} = MIN, $V_{in(1)}$ = 2 V, I_{load} = −500 μA	2.4			V
$V_{out(0)}$	Logical 0 output voltage	15	V_{CC} = MIN, $V_{in(0)}$ = 0.8 V, I_{sink} = 20 mA			0.4	V
$I_{in(0)}$	Logical 0 level input current (each input)	16	V_{CC} = MAX, V_{in} = 0.4 V			−2	mA
$I_{in(1)}$	Logical 1 level input current (each input)	17	V_{CC} = MAX, V_{in} = 2.4 V			50	μA
			V_{CC} = MAX, V_{in} = 5.5 V			1	mA
I_{OS}	Short-circuit output current‡	18	V_{CC} = MAX, V_{in} = 4.5 V	−40		−100	mA
$I_{CC(0)}$	Logical 0 level supply current	19	V_{CC} = MAX, V_{in} = 0		20	32	mA
$I_{CC(1)}$	Logical 1 level supply current	19	V_{CC} = MAX, V_{in} = 4.5 V		12	20	mA

switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10

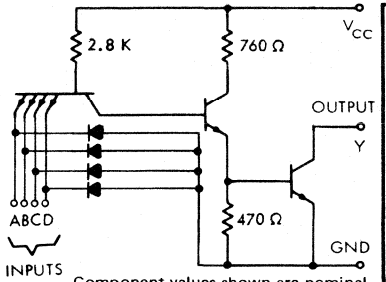
PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{pd0}	Propagation delay time to logical 0 level	74	C_L = 25 pF, R_L = 280 Ω		8.8	12	ns
t_{pd1}	Propagation delay time to logical 1 level	74	C_L = 25 pF, R_L = 280 Ω		7.6	12	ns

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
‡Not more than one output should be shorted at a time, and duration of short-circuit test should not exceed 1 second.
§ All typical values are at V_{CC} = 5 V, T_A = 25°C.

–SEE ORDERING INSTRUCTIONS PAGE 1-1–

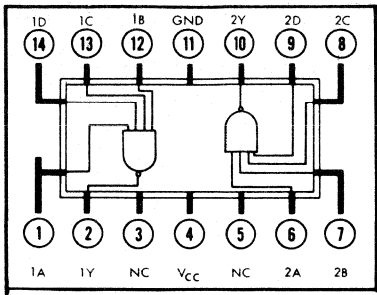
DUAL 4-INPUT POSITIVE NAND GATES (WITH OPEN-COLLECTOR OUTPUT)

schematic (each gate)

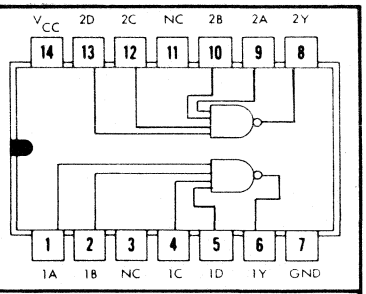


Component values shown are nominal.
NC—No Internal Connection

S
FLAT PACKAGE (TOP VIEW)



J OR N
DUAL-IN-PACKAGE (TOP VIEW)



positive logic: $Y = \overline{ABCD}$

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply Voltage V_{CC}: SN54H22 Circuits	4.5	5	5.5	V
SN74H22 Circuits	4.75	5	5.25	V
Normalized Fan-Out from Each Output,N (and see pages 3-7 and 3-8)			10	
Operating Free-Air Temperature Range: SN54H22 Circuits	−55	25	125	°C
SN74H22 Circuits	0	25	70	°C

electrical characteristics (over operating free-air temperature range unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS†	MIN	TYP§	MAX	UNIT
$V_{in(1)}$	Logical 1 input voltage required at all input terminals to ensure logical 0 (on) level at output	1	V_{CC} = MIN	2			V
$V_{in(0)}$	Logical 0 input voltage required at any input terminal to ensure logical 1 (off) level at output	7	V_{CC} = MIN			0.8	V
$I_{out(1)}$	Output reverse current	7	V_{CC} = MIN, V_{in} = 0.8 V, $V_{out(1)}$ = 5.5 V			250	μA
$V_{out(0)}$	Logical 0 output voltage (on level)	1	V_{CC} = MIN, V_{in} = 2 V, I_{sink} = 20 mA			0.4	V
$I_{in(0)}$	Logical 0 level input current (each input)	3	V_{CC} = MAX, V_{in} = 0.4 V			−2	mA
$I_{in(1)}$	Logical 1 level input current (each input)	4	V_{CC} = MAX, V_{in} = 2.4 V			50	μA
			V_{CC} = MAX, V_{in} = 5.5 V			1	mA
$I_{CC(0)}$	Logical 0 level supply current	6	V_{CC} = MAX, V_{in} = 4.5 V		26	40	mA
$I_{CC(1)}$	Logical 1 level supply current	6	V_{CC} = MAX, V_{in} = 0		3.4	5	mA

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{pd0}	Propagation delay time to logical 0 level	74	C_L = 25 pF, R_L = 280 Ω		7.5	12	ns
t_{pd1}	Propagation delay time to logical 1 level	74	C_L = 25 pF, R_L = 280 Ω		10	15	ns

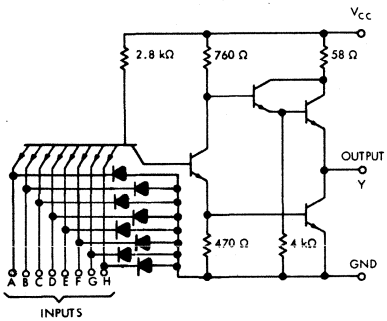
† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
§ All typical values are at V_{CC} = 5 V, T_A = 25°C.

For Applications Data, see pages 3-7 and 3-8.

—SEE ORDERING INSTRUCTIONS PAGE 1-1—

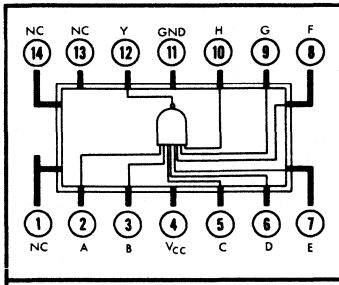
CIRCUIT TYPES SN54H30, SN74H30
8-INPUT POSITIVE NAND GATES

schematic

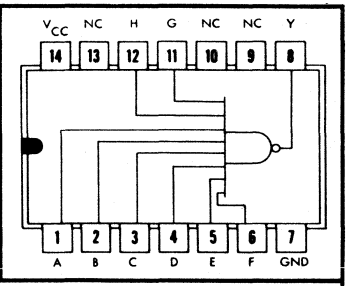


NOTES: 1. Component values shown are nominal
2. NC — No internal connection

S
FLAT PACKAGE (TOP VIEW)



J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



positive logic: $Y = \overline{ABCDEFGH}$

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply Voltage V_{CC}: SN54H30 Circuits	4.5	5	5.5	V
SN74H30 Circuits	4.75	5	5.25	V
Normalized Fan-Out From Each Output, N			10	
Operating Free-Air Temperature Range, T_A: SN54H30 Circuits	−55	25	125	°C
SN74H30 Circuits	0	25	70	°C

electrical characteristics (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS†	MIN	TYP §	MAX	UNIT
$V_{in(1)}$	Logical 1 input voltage required at all input terminals to ensure logical 0 level at output	1	V_{CC} = MIN	2			V
$V_{in(0)}$	Logical 0 input voltage required at any input terminal to ensure logical 1 level at output	2	V_{CC} = MIN			0.8	V
$V_{out(1)}$	Logical 1 output voltage	2	V_{CC} = MIN, V_{in} = 0.8 V, I_{load} = −500 μA	2.4			V
$V_{out(0)}$	Logical 0 output voltage	1	V_{CC} = MIN, V_{in} = 2 V, I_{sink} = 20 mA			0.4	V
$I_{in(0)}$	Logical 0 level input current (each input)	3	V_{CC} = MAX, V_{in} = 0.4 V			−2	mA
$I_{in(1)}$	Logical 1 level input current (each input)	4	V_{CC} = MAX, V_{in} = 2.4 V			50	μA
			V_{CC} = MAX, V_{in} = 5.5 V			1	mA
I_{OS}	Short-circuit output current‡	5	V_{CC} = MAX	−40		−100	mA
$I_{CC(0)}$	Logical 0 level supply current	6	V_{CC} = MAX, V_{in} = 4.5 V		6.5	10	mA
$I_{CC(1)}$	Logical 1 level supply current	6	V_{CC} = MAX, V_{in} = 0		2.5	4.2	mA

switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{pd0}	Propagation delay time to logical 0 level	74	C_L = 25 pF, R_L = 280 Ω		8.9	12	ns
t_{pd1}	Propagation delay time to logical 1 level	74	C_L = 25 pF, R_L = 280 Ω		6.8	10	ns

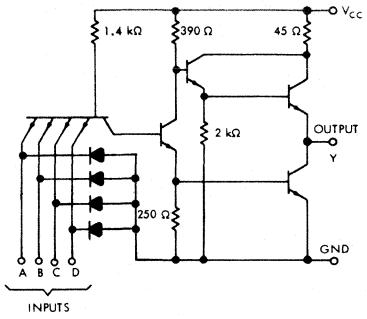
†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

‡Duration of short-circuit test should not exceed 1 second.

§ All typical values are at V_{CC} = 5 V, T_A = 25°C.

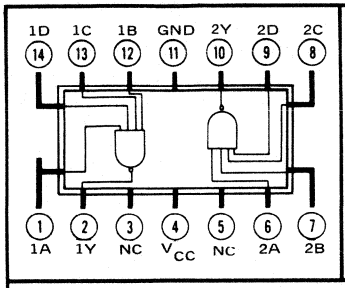
—SEE ORDERING INSTRUCTIONS PAGE 1-1—

schematic (each gate)

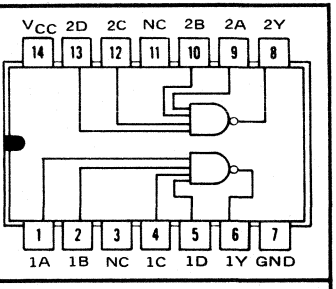


NOTES: 1. Component values shown are nominal
2. NC — No internal connection

S
FLAT PACKAGE (TOP VIEW)



J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



positive logic: $Y = \overline{ABCD}$

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply Voltage V_{CC}: SN54H40 Circuits	4.5	5	5.5	V
SN74H40 Circuits	4.75	5	5.25	V
Normalized Fan-Out From Each Output, N			30	
Operating Free-Air Temperature Range, T_A: SN54H40 Circuits	−55	25	125	°C
SN74H40 Circuits	0	25	70	°C

electrical characteristics (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS†	MIN	TYP §	MAX	UNIT
$V_{in(1)}$	Logical 1 input voltage required at all input terminals to ensure logical 0 level at output	1	V_{CC} = MIN	2			V
$V_{in(0)}$	Logical 0 input voltage required at any input terminal to ensure logical 1 level at output	2	V_{CC} = MIN			0.8	V
$V_{out(1)}$	Logical 1 output voltage	2	V_{CC} = MIN, V_{in} = 0.8 V, I_{load} = −1.5 mA	2.4			V
$V_{out(0)}$	Logical 0 output voltage	1	V_{CC} = MIN, V_{in} = 2 V, I_{sink} = 60 mA			0.4	V
$I_{in(0)}$	Logical 0 level input current (each input)	3	V_{CC} = MAX, V_{in} = 0.4 V			−4	mA
$I_{in(1)}$	Logical 1 level input current (each input)	4	V_{CC} = MAX, V_{in} = 2.4 V			100	μA
			V_{CC} = MAX, V_{in} = 5.5 V			1	mA
I_{OS}	Short-circuit output current‡	5	V_{CC} = MAX	−40		−125	mA
$I_{CC(0)}$	Logical 0 level supply current	6	V_{CC} = MAX, V_{in} = 4.5 V		25	40	mA
$I_{CC(1)}$	Logical 1 level supply current	6	V_{CC} = MAX, V_{in} = 0		10.4	16	mA

switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 30

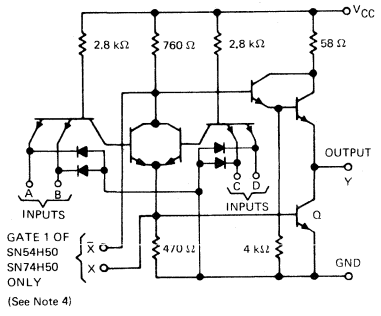
PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{pd0}	Propagation delay time to logical 0 level	$\overline{74}$	C_L = 25 pF, R_L = 93 Ω		6.5	12	ns
t_{pd1}	Propagation delay time to logical 1 level	$\overline{74}$	C_L = 25 pF, R_L = 93 Ω		8.5	12	ns

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
‡Not more than one output should be shorted at a time, and duration of short-circuit test should not exceed 1 second.
§All typical values are at V_{CC} = 5 V, T_A = 25°C.

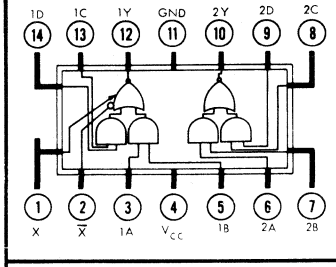
—SEE ORDERING INSTRUCTIONS PAGE 1-1—

CIRCUIT TYPES SN54H50, SN54H51, SN74H50, SN74H51
DUAL 2-WIDE 2-INPUT AND-OR-INVERT GATES

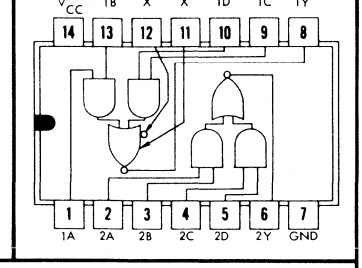
schematic (each gate)



S
FLAT PACKAGE (TOP VIEW)



J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



positive logic: $Y = \overline{(AB) + (CD) + (X)}$
(X = Output of SN54H60/SN74H60 or SN54H62/SN74H62)

NOTES:
1. Component values are nominal.
2. Both expander inputs are used simultaneously for expanding.
3. If expander is not used leave X and $\bar{X}$ pins open.
4. Expander inputs X and $\bar{X}$ are functional on the SN54H50 and SN75H50 circuits only. Make no external connection to X and $\bar{X}$ pins of the SN54H51 and SN74H51.
5. A total of four SN54H60/SN74H60 expander gates or one SN54H62/SN74H62 expander gate may be connected to the expander inputs.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply Voltage V_{CC}: SN54H50, SN54H51 Circuits	4.5	5	5.5	V
SN74H50, SN74H51 Circuits	4.75	5	5.25	V
Normalized Fan-Out From Each Output, N			10	
Operating Free-Air Temperature Range, T_A: SN54H50, SN54H51 Circuits	−55	25	125	°C
SN74H50, SN74H51 Circuits	0	25	70	°C

electrical characteristics (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS†	MIN	TYP§	MAX	UNIT
$V_{in(1)}$	Logical 1 input voltage required at both input terminals of either AND section to ensure logical 0 at output	20	V_{CC} = MIN	2			V
$V_{in(0)}$	Logical 0 input voltage required at one input terminal of each AND section to ensure logical 1 at output	21	V_{CC} = MIN			0.8	V
$V_{out(1)}$	Logical 1 output voltage	21	V_{CC} = MIN, V_{in} = 0.8 V, I_{load} = −500 μA	2.4			V
$V_{out(0)}$	Logical 0 output voltage	20	V_{CC} = MIN, V_{in} = 2 V, I_{sink} = 20 mA			0.4	V
$I_{in(0)}$	Logical 0 level input current (each input)	22	V_{CC} = MAX, V_{in} = 0.4 V			−2	mA
$I_{in(1)}$	Logical 1 level input current (each input)	23	V_{CC} = MAX, V_{in} = 2.4 V			50	μA
			V_{CC} = MAX, V_{in} = 5.5 V			1	mA
I_{OS}	Short-circuit output current‡	24	V_{CC} = MAX	−40		−100	mA
$I_{CC(0)}$	Logical 0 level supply current	25	V_{CC} = MAX, V_{in} = 4.5 V		15.2	24	mA
$I_{CC(1)}$	Logical 1 level supply current	26	V_{CC} = MAX, V_{in} = 0		8.2	12.8	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type. Expander pins are open.

‡Not more than one output should be shorted at a time, and duration of short-circuit test should not exceed 1 second.

§ All typical values are at V_{CC} = 5 V, T_A = 25°C.

—SEE ORDERING INSTRUCTIONS PAGE 1-1—

electrical characteristics (SN54H50 circuits only) using expander inputs, V_{CC} = 4.5 V, T_A = −55°C

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{in\bar{x}}$	Expander-node input current	27	$V_{\bar{x}}$ = 1.4 V			−5.85	mA
$V_{BE(Q)}$	Base-emitter voltage of output transistor Q	28	I_{sink} = 20 mA, I_1 = 700 μA, R_1 = 0			1	V
$V_{out(1)}$	Logical 1 output voltage	29	I_{load} = −500 μA, I_1 = 320 μA, I_2 = −320 μA	2.4			V
$V_{out(0)}$	Logical 0 output voltage	28	I_{sink} = 20 mA, I_1 = 470 μA, R_1 = 68 Ω			0.4	V

electrical characteristics (SN74H50 circuits only) using expander inputs, V_{CC} = 4.75 V, T_A = 0°C

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{in\bar{x}}$	Expander-node input current	27	$V_{\bar{x}}$ = 1.4 V			−6.3	mA
$V_{BE(Q)}$	Base-emitter voltage of output transistor Q	28	I_{sink} = 20 mA, I_1 = 1.1 mA, R_1 = 0			1	V
$V_{out(1)}$	Logical 1 output voltage	29	I_{load} = −500 μA, I_1 = 570 μA, I_2 = −570 μA	2.4			V
$V_{out(0)}$	Logical 0 output voltage	28	I_{sink} = 20 mA, I_1 = 600 μA, R_1 = 63 Ω			0.4	V

switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10, expander pins are open

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{pd0}	Propagation delay time to logical 0 level	74	C_L = 25 pF, R_L = 280 Ω		6.2	11	ns
t_{pd1}	Propagation delay time to logical 1 level	74	C_L = 25 pF, R_L = 280 Ω		6.8	11	ns

switching characteristics, (SN54H50/SN74H50 circuits only), V_{CC} = 5 V, T_A = 25°C, N = 10, C_x = 15 pF¶

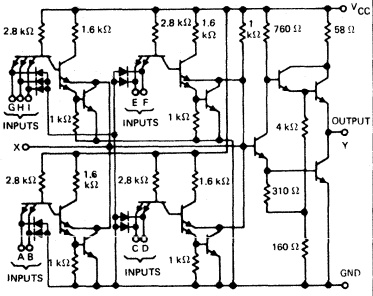
PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{pd0}	Propagation delay time to logical 0 level	75	C_L = 25 pF, R_L = 280 Ω		7.4		ns
t_{pd1}	Propagation delay time to logical 1 level	75	C_L = 25 pF, R_L = 280 Ω		11		ns

¶ See curves on page 3-80 for effect of other values of C_x.

—SEE ORDERING INSTRUCTIONS PAGE 1-1—

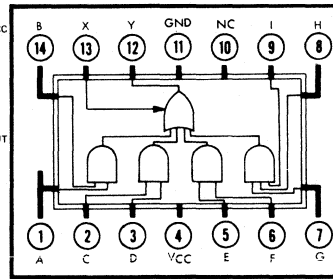
CIRCUIT TYPES SN54H52, SN74H52
EXPANDABLE 2-2-2-3-INPUT AND-OR GATES

schematic



NOTES: 1. Component values shown are nominal.
2. A total of six expander gates may be connected to the expander input X.
3. NC — No internal connection.

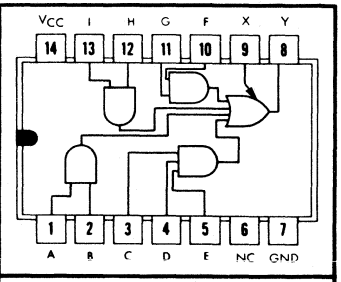
S
FLAT PACKAGE (TOP VIEW)



positive logic:

$Y = (AB) + (CD) + (EF) + (GHI) + (X)$
(X = Output of SN54H61/SN74H61)

J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



positive logic:

$Y = (AB) + (CDE) + (FG) + (HI) + (X)$
(X = Output of SN54H61/SN74H61)

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply Voltage V_{CC}: SN54H52 Circuits	4.5	5	5.5	V
SN74H52 Circuits	4.75	5	5.25	V
Normalized Fan-Out From Each Output, N			10	
Operating Free-Air Temperature Range, T_A: SN54H52 Circuits	−55	25	125	°C
SN74H52 Circuits	0	25	70	°C

electrical characteristics (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS†	MIN	TYP§	MAX	UNIT
$V_{in(1)}$	Logical 1 input voltage required at all input terminals of one AND section to ensure logical 1 at output	30	V_{CC} = MIN	2			V
$V_{in(0)}$	Logical 0 input voltage required at one input terminal of each AND section to ensure logical 0 at output	31	V_{CC} = MIN			0.8	V
$V_{out(1)}$	Logical 1 output voltage	30	V_{CC} = MIN, V_{in} = 2 V, I_{load} = −500 μA	2.4			V
$V_{out(0)}$	Logical 0 output voltage	31	V_{CC} = MIN, V_{in} = 0.8 V, I_{sink} = 20 mA			0.4	V
$I_{in(0)}$	Logical 0 level input current (each input)	32	V_{CC} = MAX, V_{in} = 0.4 V			−2	mA
$I_{in(1)}$	Logical 1 level input current (each input)	33	V_{CC} = MAX, V_{in} = 2.4 V			50	μA
			V_{CC} = MAX, V_{in} = 5.5 V			1	mA
I_{os}	Short-circuit output current‡	34	V_{CC} = MAX, V_{in} = 4.5 V	−40		−100	mA
$I_{CC(0)}$	Logical 0 level supply current	35	V_{CC} = MAX, V_{in} = 0		15.2	24	mA
$I_{CC(1)}$	Logical 1 level supply current	35	V_{CC} = MAX, V_{in} = 4.5 V		20	31	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type. Expander pin is open.
‡Duration of short-circuit test should not exceed 1 second.
§ All typical values are at V_{CC} = 5 V, T_A = 25°C.

—SEE ORDERING INSTRUCTIONS PAGE 1-1—

electrical characteristics (SN54H52 circuits only) using expander input, V_{CC} = 4.5 V

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{inX}	Expander-node input current	36	V_X = 1 V, I_{load} = −500 μA, T_A = −55°C	−2.7		−4.5	mA
$V_{out(1)}$	Logical 1 output voltage	36	V_X = 1 V, I_{load} = −500 μA, T_A = −55°C	2.4			V
$V_{out(0)}$	Logical 0 output voltage	37	I_{inX} = −300 μA, I_{sink} = 20 mA, T_A = 125°C			0.4	V

electrical characteristics (SN74H52 circuits only) using expander input, V_{CC} = 4.75 V

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{inX}	Expander-node input current	36	V_X = 1 V, I_{load} = −500 μA, T_A = 0°C	−2.9		−5.35	mA
$V_{out(1)}$	Logical 1 output voltage	36	V_X = 1 V, I_{load} = −500 μA, T_A = 0°C	2.4			V
$V_{out(0)}$	Logical 0 output voltage	37	I_{inX} = −300 μA, I_{sink} = 20 mA, T_A = 70°C			0.4	V

switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10, expander pin is open

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{pd0}	Propagation delay time to logical 0 level	74	C_L = 25 pF, R_L = 280 Ω		9.2	15	ns
t_{pd1}	Propagation delay time to logical 1 level	74	C_L = 25 pF, R_L = 280 Ω		10.6	15	ns

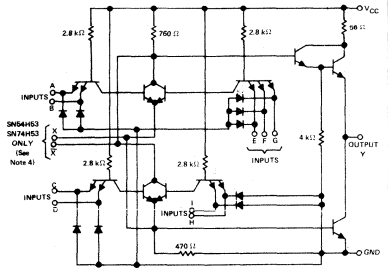
switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10, C_X = 15 pF¶

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{pd0}	Propagation delay time to logical 0 level	76	C_L = 25 pF, R_L = 280 Ω		9.8		ns
t_{pd1}	Propagation delay time to logical 1 level	76	C_L = 25 pF, R_L = 280 Ω		14.8		ns

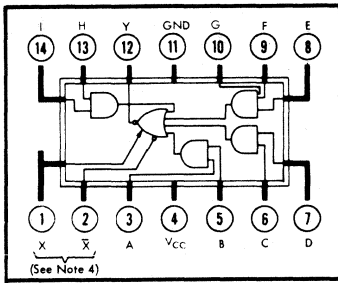
¶See curves on page 3-80 for effect of other values of C_X.

CIRCUIT TYPES SN54H53, SN54H54, SN74H53, SN74H54
EXPANDABLE 2-2-2-3-INPUT AND-OR-INVERT GATES

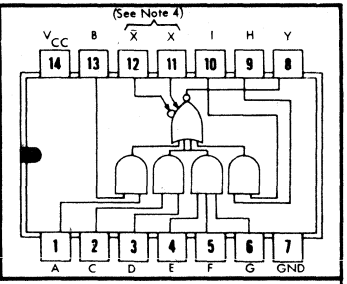
schematic



S
FLAT PACKAGE (TOP VIEW)



J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



positive logic: $Y = \overline{(AB) + (CD) + (EFG) + (HI) + (\bar{X})}$
(X = Output of SN54H60/SN74H60 or SN54H62/SN74H62)

NOTES: 1. *Component values shown are nominal.*
2. Both expander inputs are used simultaneously for expanding.
3. If expander is not used leave X and $\bar{X}$ pins open.
4. Expander inputs X and $\bar{X}$ are functional on the SN54H53 and SN74H53 circuits only. Make no external connection to X and $\bar{X}$ pins of the SN54H54 and SN74H54.
5. A total of four SN54H60/SN74H60 expander gates or one SN54H62/SN74H62 expander gate may be connected to the expander inputs.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply Voltage V_{CC}: SN54H53, SN54H54 Circuits	4.5	5	5.5	V
SN74H53, SN74H54 Circuits	4.75	5	5.25	V
Normalized Fan-Out From Each Output, N			10	
Operating Free-Air Temperature Range, T_A: SN54H53, SN54H54 Circuits	−55	25	125	°C
SN74H53, SN74H54 Circuits	0	25	70	°C

electrical characteristics (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS†	MIN	TYP §	MAX	UNIT
$V_{in(1)}$	Logical 1 input voltage required at all input terminals of one AND section to ensure logical 0 at output	20	V_{CC} = MIN	2			V
$V_{in(0)}$	Logical 0 input voltage required at one input terminal of each AND section to ensure logical 1 at output	21	V_{CC} = MIN			0.8	V
$V_{out(1)}$	Logical 1 output voltage	21	V_{CC} = MIN, V_{in} = 0.8 V, I_{load} = −500 μA	2.4			V
$V_{out(0)}$	Logical 0 output voltage	20	V_{CC} = MIN, V_{in} = 2 V, I_{sink} = 20 mA			0.4	V
$I_{in(0)}$	Logical 0 level input current (each input)	22	V_{CC} = MAX, V_{in} = 0.4 V			−2	mA
$I_{in(1)}$	Logical 1 level input current (each input)	23	V_{CC} = MAX, V_{in} = 2.4 V			50	μA
			V_{CC} = MAX, V_{in} = 5.5 V			1	mA
I_{os}	Short-circuit output current‡	24	V_{CC} = MAX	−40		−100	mA
$I_{CC(0)}$	Logical 0 level supply current	25	V_{CC} = MAX V_{in} = 4.5 V		9.4	14	mA
$I_{CC(1)}$	Logical 1 level supply current	26	V_{CC} = MAX, V_{in} = 0		7.1	11	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type. Expander pins are open.
‡Duration of short-circuit test should not exceed 1 second.
§All typical values are at V_{CC} = 5 V, T_A = 25°C.

–SEE ORDERING INSTRUCTIONS PAGE 1-1–

electrical characteristics (SN54H53 circuits only) using expander inputs, V_{CC} = 4.5 V, T_A = −55° C

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{in\,\bar{x}}$	Expander-node input current	27	$V_{\bar{x}}$ = 1.4 V			−5.85	mA
$V_{BE(Q)}$	Base-emitter voltage of output transistor Q	28	I_{sink} = 20 mA, I_1 = 700 μA, R_1 = 0			1	V
$V_{out(1)}$	Logical 1 output voltage	29	I_{load} = −500 μA, I_1 = 320 μA, I_2 = −320 μA	2.4			V
$V_{out(0)}$	Logical 0 output voltage	28	I_{sink} = 20 mA, I_1 = 470 μA, R_1 = 68 Ω			0.4	V

electrical characteristics (SN74H53 circuits only) using expander inputs, V_{CC} = 4.75 V, T_A = 0° C

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{in\,\bar{x}}$	Expander-node input current	27	$V_{\bar{x}}$ = 1.4 V			−6.3	mA
$V_{BE(Q)}$	Base-emitter voltage of output transistor Q	28	I_{sink} = 20 mA, I_1 = 1.1 mA, R_1 = 0			1	V
$V_{out(1)}$	Logical 1 output voltage	29	I_{load} = −500 μA, I_1 = 570 μA, I_2 = −570 μA	2.4			V
$V_{out(0)}$	Logical 0 output voltage	28	I_{sink} = 20 mA, I_1 = 600 μA, R_1 = 63 Ω			0.4	V

switching characteristics, V_{CC} = 5 V, T_A = 25° C, N = 10 , expander pins are open

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{pd0}	Propagation delay time to logical 0 level	74	C_L = 25 pF, R_L = 280 Ω		6.2	11	ns
t_{pd1}	Propagation delay time to logical 1 level	74	C_L = 25 pF, R_L = 280 Ω		7	11	ns

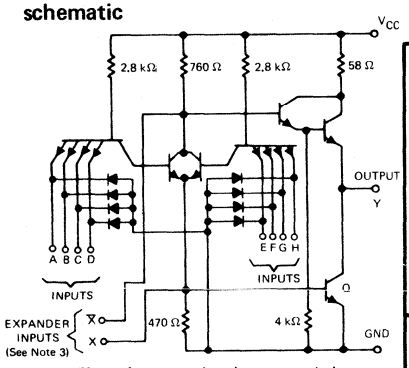
switching characteristics, (SN54H53/SN74H53 circuits only) V_{CC} = 5 V, T_A = 25°C, N = 10, C_x = 15 pF¶

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{pd0}	Propagation delay time to logical 0 level	75	C_L = 25 pF, R_L = 280 Ω		7.4		ns
t_{pd1}	Propagation delay time to logical 1 level	75	C_L = 25 pF, R_L = 280 Ω		11.4		ns

¶See curves on page 3-80 for effect of other values of C_x.

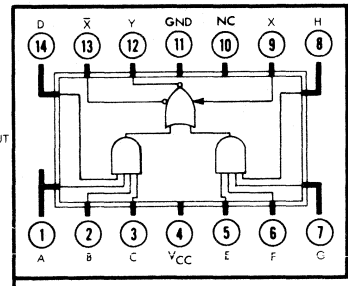
CIRCUIT TYPES SN54H55, SN74H55
EXPANDABLE 4-INPUT AND-OR-INVERT GATES

schematic

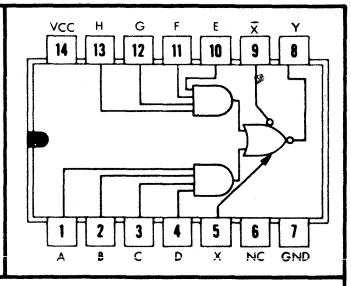


NOTES:
1. Component values shown are nominal.
2. Both expander inputs are used simultaneously for expanding.
3. If expander is not used, leave X and X̄ pins open.
4. A total of four SN54H60/SN74H60 expander gates or one SN54H62/SN74H62 expander gate may be connected to the expander inputs.
5. NC — No internal connection.

S
FLAT PACKAGE (TOP VIEW)



J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



positive logic: $Y = \overline{(ABCD) + (EFGH) + (X)}$
X = Output of SN54H60/SN74H60 or SN54H62/SN74H62 circuit.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply Voltage V_{CC}: SN54H55 Circuits	4.5	5	5.5	V
SN74H55 Circuits	4.75	5	5.25	V
Normalized Fan-Out From Each Output, N			10	
Operating Free-Air Temperature Range, T_A: SN54H55 Circuits	−55	25	125	°C
SN74H55 Circuits	0	25	70	°C

electrical characteristics (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS†	MIN	TYP§	MAX	UNIT
$V_{in(1)}$	Logical 1 input voltage required at all input terminals of either AND section to ensure logical 0 at output	20	V_{CC} = MIN	2			V
$V_{in(0)}$	Logical 0 input voltage required at one input terminal of each AND section to ensure logical 1 at output	21	V_{CC} = MIN			0.8	V
$V_{out(1)}$	Logical 1 output voltage	21	V_{CC} = MIN, V_{in} = 0.8 V, I_{load} = −500 μA	2.4			V
$V_{out(0)}$	Logical 0 output voltage	20	V_{CC} = MIN, V_{in} = 2 V, I_{sink} = 20 mA			0.4	V
$I_{in(0)}$	Logical 0 level input current (each input)	22	V_{CC} = MAX, V_{in} = 0.4 V			−2	mA
$I_{in(1)}$	Logical 1 level input current (each input)	23	V_{CC} = MAX, V_{in} = 2.4 V			50	μA
			V_{CC} = MAX, V_{in} = 5.5 V			1	mA
I_{os}	Short-circuit output current‡	24	V_{CC} = MAX	−40		−100	mA
$I_{CC(0)}$	Logical 0 level supply current	25	V_{CC} = MAX, V_{in} = 4.5 V		7.5	12	mA
$I_{CC(1)}$	Logical 1 level supply current	26	V_{CC} = MAX, V_{in} = 0		4.5	6.4	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type. Expander pins are open.

‡Duration of short-circuit test should not exceed 1 second.

§ All typical values are at V_{CC} = 5 V, T_A = 25°C.

–SEE ORDERING INSTRUCTIONS PAGE 1-1–

electrical characteristics (SN54H55 circuits only) using expander inputs, V_{CC} = 4.5 V, T_A = −55°C

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{in\bar{x}}$	Expander-node input current	27	$V_{\bar{x}}$ = 1.4 V			−5.85	mA
$V_{BE(Q)}$	Base-emitter voltage of output transistor Q	28	I_{sink} = 20 mA, I_1 = 700 μA, R_1 = 0			1	V
$V_{out(1)}$	Logical 1 output voltage	29	I_{load} = −500 μA, I_1 = 320 μA, I_2 = −320 μA	2.4			V
$V_{out(0)}$	Logical 0 output voltage	28	I_{sink} = 20 mA, I_1 = 470 μA, R_1 = 68 Ω			0.4	V

electrical characteristics (SN74H55 circuits only) using expander inputs, V_{CC} = 4.75 V, T_A = 0°C

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{in\bar{x}}$	Expander-node input current	27	$V_{\bar{x}}$ = 1.4 V			−6.3	mA
$V_{BE(Q)}$	Base-emitter voltage of output transistor Q	28	I_{sink} = 20 mA, I_1 = 1.1 mA, R_1 = 0			1	V
$V_{out(1)}$	Logical 1 output voltage	29	I_{load} = −500 μA, I_1 = 570 μA, I_2 = −570 μA	2.4			V
$V_{out(0)}$	Logical 0 output voltage	28	I_{sink} = 20 mA, I_1 = 600 μA, R_1 = 63 Ω			0.4	V

switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10, expander pins are open

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{pd0}	Propagation delay time to logical 0 level	74	C_L = 25 pF, R_L = 280 Ω		6.5	11	ns
t_{pd1}	Propagation delay time to logical 1 level	74	C_L = 25 pF, R_L = 280 Ω		7	11	ns

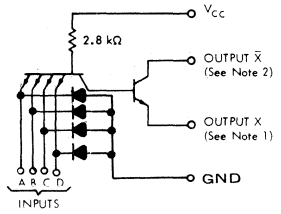
switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10, C_X = 15 pF¶

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{pd0}	Propagation delay time to logical 0 level	75	C_L = 25 pF, R_L = 280 Ω		7.7		ns
t_{pd1}	Propagation delay time to logical 1 level	75	C_L = 25 pF, R_L = 280 Ω		11.4		ns

¶ See curves on page 3-80 for effect of other values of C_X.

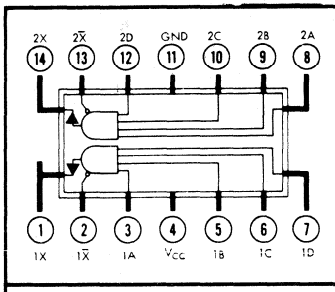
CIRCUIT TYPE SN54H60
DUAL 4-INPUT EXPANDER (FOR USE WITH SN54H50, SN54H53, SN54H55 CIRCUITS)

schematic (each expander)

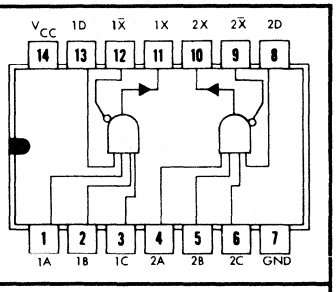


NOTES: 1. Connect to X input of SN54H50, SN54H53, or SN54H55 circuit.
2. Connect to $\overline{X}$ input of SN54H50, SN54H53, or SN54H55 circuit.
3. Component values shown are nominal.

S
FLAT PACKAGE (TOP VIEW)



J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



positive logic: X = ABCD
when connected to X and $\overline{X}$ pins of SN54H50, SN54H53, or SN54H55 circuit.

recommended operating conditions

Supply Voltage V_{CC} . . . . . 4.5 V to 5.5 V
Maximum number of expanders that may be fanned-in to one SN54H50, SN54H53, or SN54H55 circuit 4

electrical characteristics (unless otherwise noted T_A = –55°C to 125°C)

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP§	MAX	UNIT
$V_{in(1)}$	Logical 1 input voltage required at all input terminals to ensure output is in the on state	38	V_{CC} = 4.5 V	2			V
$V_{in(0)}$	Logical 0 input voltage required at any input terminal to ensure output is in the off state	39	V_{CC} = 4.5 V			0.8	V
V_{on}	On-state output voltage	38	V_{CC} = 4.5 V, V_{in} = 2 V, V_1 = 1 V, I_{on} = 5.85 mA, T_A = –55°C			0.4	V
			V_{CC} = 5.5 V, V_{in} = 2 V, V_1 = 0.6 V, I_{on} = 7.85 mA, T_A = 125°C			0.4	V
I_{off}	Off-state output current	39	V_{CC} = 4.5 V, V_{in} = 0.8 V, V_1 = 4.5 V, R = 575 Ω, T_A = –55°C			320	μA
I_{on}	On-state output current	40	V_{CC} = 4.5 V, V_{in} = 2 V, V_1 = 1 V, T_A = –55°C	–470			μA
$I_{in(0)}$	Logical 0 level input current (each input)	39	V_{CC} = 5.5 V, V_{in} = 0.4 V			–2	mA
$I_{in(1)}$	Logical 1 level input current (each input)	41	V_{CC} = 5.5 V, V_{in} = 2.4 V			50	μA
			V_{CC} = 5.5 V, V_{in} = 5.5 V			1	mA
$I_{CC(on)}$	On-state supply current	42	V_{CC} = 5.5 V, V_{in} = 4.5 V, V_1 = 0.85 V		1.9	3.5	mA
$I_{CC(off)}$	Off-state supply current	42	V_{CC} = 5.5 V, V_{in} = 0, V_1 = 0.85 V		3	4.5	mA

§ All typical values are at V_{CC} = 5 V, T_A = 25°C.

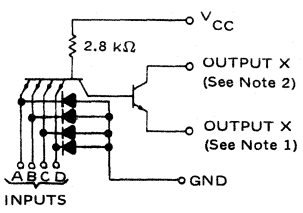
output capacitance, V_{CC} and GND terminals open, T_A = 25°C

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
C_x	Effective capacitance of output transistor Q_1	79	f = 1 MHz		1.3		pF

—SEE ORDERING INSTRUCTIONS PAGE 1-1—

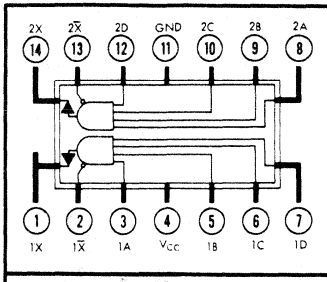
CIRCUIT TYPE SN74H60
DUAL 4-INPUT EXPANDER

schematic (each expander)

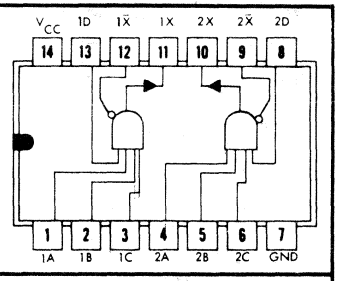


NOTES: 1. Connect to X input of SN74H50, SN74H53, or SN74H55 circuit.
2. Connect to $\overline{X}$ input of SN74H50, SN74H53, or SN74H55 circuit.
3. Component values shown are nominal.

S
FLAT PACKAGE (TOP VIEW)



J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



positive logic: X = ABCD
when connected to X and $\overline{X}$ pins of SN74H50, SN74H53, or SN74H55 circuits.

recommended operating conditions

Supply Voltage V_{CC} . . . . . 4.75 V to 5.25 V
Maximum number of expanders that may be fanned-in to one SN74H50, SN74H53, or SN74H55 circuit 4

electrical characteristics (unless otherwise noted T_A = 0°C to 70°C)

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP §	MAX	UNIT
$V_{in(1)}$	Logical 1 input voltage required at all input terminals to ensure output is in the on state	38	V_{CC} = 4.75 V	2			V
$V_{in(0)}$	Logical 0 input voltage required at any input terminal to ensure output is in the off state	39	V_{CC} = 4.75 V			0.8	V
V_{on}	On-state output voltage	38	V_{CC} = 4.75 V, V_{in} = 2 V, V_I = 1 V, I_{on} = 6.3 mA, T_A = 0°C			0.4	V
			V_{CC} = 5.25 V, V_{in} = 2 V, V_I = 0.6 V, I_{on} = 7.4 mA, T_A = 70°C			0.4	V
I_{off}	Off-state output current	39	V_{CC} = 4.75 V, V_{in} = 0.8 V, V_I = 4.5 V, R = 575 Ω, T_A = 0°C			570	μA
I_{on}	On-state output current	40	V_{CC} = 4.75 V, V_{in} = 2 V, V_I = 1 V, T_A = 0°C	−600			μA
$I_{in(0)}$	Logical 0 level input current (each input)	39	V_{CC} = 5.25 V, V_{in} = 0.4 V			−2	mA
$I_{in(1)}$	Logical 1 level input current (each input)	41	V_{CC} = 5.25 V, V_{in} = 2.4 V			50	μA
			V_{CC} = 5.25 V, V_{in} = 5.5 V			1	mA
$I_{CC(on)}$	On-state supply current	42	V_{CC} = 5.25 V, V_{in} = 4.5 V, V_I = 0.85 V		1.9	3.5	mA
$I_{CC(off)}$	Off-state supply current	42	V_{CC} = 5.25 V, V_{in} = 0, V_I = 0.85 V		3	4.5	mA

§ All typical values are at V_{CC} = 5 V, T_A = 25°C.

output capacitance, V_{CC} and GND terminals open, T_A = 25°C

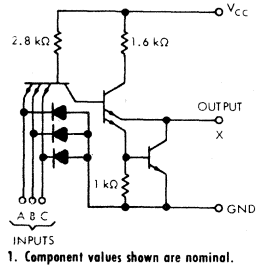
PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
C_X	Effective capacitance of output transistor Q_1	79	f = 1 MHz		1.3		pF

—SEE ORDERING INSTRUCTIONS PAGE 1-1—

CIRCUIT TYPES SN54H61, SN74H61
TRIPLE 3-INPUT EXPANDERS

(FOR USE WITH SN54H52, SN74H52 CIRCUITS)

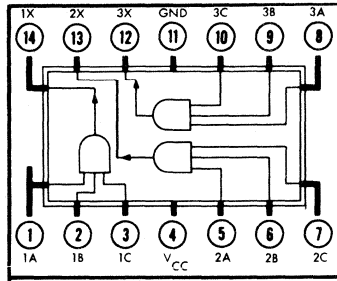
schematic (each expander)



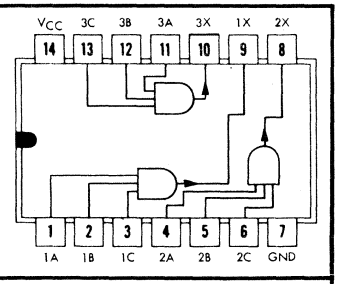
NOTES: 1. Component values shown are nominal.

2. A total of six expander gates may be connected to the SN54H52/SN74H52 expander input.

S
FLAT PACKAGE (TOP VIEW)



J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



positive logic: X = ABC
when connected to the X input of the SN54H52 or SN74H52 circuit.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply Voltage V_{CC}: SN54H61 Circuits	4.5	5	5.5	V
SN74H61 Circuits	4.75	5	5.25	V
Operating Free-Air Temperature Range, T_A: SN54H61 Circuits	−55	25	125	°C
SN74H61 Circuits	0	25	70	°C

electrical characteristics (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS†	MIN	TYP§	MAX	UNIT
$V_{in(0)}$	Logical 0 input voltage required at any input terminal to ensure output is in the off state	43	V_{CC} = MIN			0.8	V
I_{off}	Off-state reverse current	43	V_{CC} = MIN, $V_{in(0)}$ = 0.8 V, V_{off} = 2.2 V, T_A = MAX			50	μA
$I_{in(0)}$	Logical 0 level input current (each input)	44	V_{CC} = MAX, V_{in} = 0.4 V			−2	mA
$I_{in(1)}$	Logical 1 level input current (each input)	45	V_{CC} = MAX, V_{in} = 2.4 V			50	μA
			V_{CC} = MAX, V_{in} = 5.5 V			1	mA
$I_{CC(on)}$	On-state supply current	46	V_{CC} = MAX, V_{in} = 4.5 V		7.2	12	mA
$I_{CC(off)}$	Off-state supply current	46	V_{CC} = MAX, V_{in} = 0		3	5	mA

electrical characteristics SN54H61 circuits only

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{in(1)}$	Logical 1 input voltage required at all input terminals to ensure output is in the on state	47	V_{CC} = 4.5 V	2			V
V_{on}	On-state output voltage	47	V_{CC} = 4.5 V, $V_{in(1)}$ = 2 V, I_{on} = 4.5 mA, T_A = −55°C			1	V

electrical characteristics SN74H61 circuits only

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{in(1)}$	Logical 1 input voltage required at all input terminals to ensure output is in the on state	47	V_{CC} = 4.75 V	2			V
V_{on}	On-state output voltage	47	V_{CC} = 4.75 V, $V_{in(1)}$ = 2 V, I_{on} = 5.35 mA, T_A = 0°C			1	V

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

§ All typical values are at V_{CC} = 5 V, T_A = 25°C.

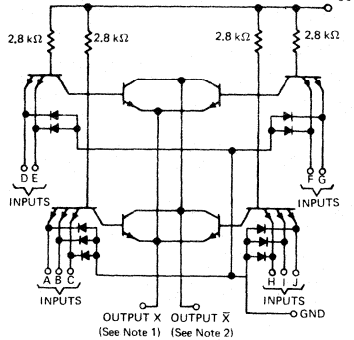
output capacitance, V_{CC} and GND terminals open, T_A = 25°C

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
C_x	Effective capacitance of output transistor Q_1	80	f = 1 MHz		1.3		pF

–SEE ORDERING INSTRUCTIONS PAGE 1-1–

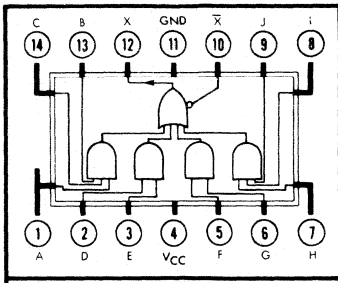
CIRCUIT TYPE SN54H62
3-2-2-3-INPUT AND-OR EXPANDER

schematic



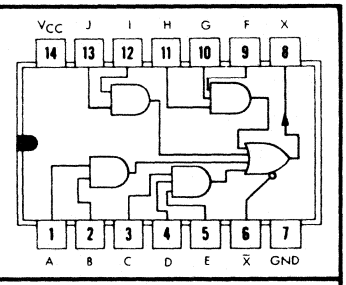
NOTES: 1. Connect to X input of SN54H50, SN54H53, or SN54H55 circuit.
2. Connect to $\overline{X}$ input of SN54H50, SN54H53, or SN54H55 circuit.
3. Component values shown are nominal.

S
FLAT PACKAGE (TOP VIEW)



positive logic:
X = (ABC) + (DE) + (FG) + (HIJ)
when connected to X and $\overline{X}$ pins of SN54H50, SN54H53, or SN54H55 circuit.

J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



positive logic:
X = (AB) + (CDE) + (FGH) + (IJ)
when connected to X and $\overline{X}$ pins of SN54H50, SN54H53, or SN54H55 circuit.

recommended operating conditions

Supply Voltage V_{CC} . . . . . 4.5 V to 5.5 V
Maximum number of expanders that may be fanned-in to one SN54H50, SN54H53, or SN54H55 circuit 1

electrical characteristics (unless otherwise noted T_A = –55°C to 125°C)

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP§	MAX	UNIT
$V_{in(1)}$	Logical 1 input voltage required at all input terminals of one AND section to ensure output is in the on state	48	V_{CC} = 4.5 V	2			V
$V_{in(0)}$	Logical 0 input voltage required at one input terminal of each AND section to ensure output is in the off state	49	V_{CC} = 4.5 V			0.8	V
V_{on}	On-state output voltage	48	V_{CC} = 4.5 V, V_{in} = 2 V, V_I = 1 V, I_{on} = 5.85 mA, T_A = –55°C			0.4	V
			V_{CC} = 5.5 V, V_{in} = 2 V, V_I = 0.6 V, I_{on} = 7.85 mA, T_A = 125°C			0.4	V
I_{off}	Off-state output current	49	V_{CC} = 4.5 V, V_{in} = 0.8 V, V_I = 4.5 V, R = 575 Ω, T_A = –55°C			320	μA
I_{on}	On-state output current	50	V_{CC} = 4.5 V, V_{in} = 2 V, V_I = 1 V, T_A = –55°C	–470			μA
$I_{in(0)}$	Logical 0 level input current (each input)	51	V_{CC} = 5.5 V, V_{in} = 0.4 V			–2	mA
$I_{in(1)}$	Logical 1 level input current (each input)	52	V_{CC} = 5.5 V, V_{in} = 2.4 V			50	μA
			V_{CC} = 5.5 V, V_{in} = 5.5 V			1	mA
$I_{CC(on)}$	On-state supply current	53	V_{CC} = 5.5 V, V_{in} = 4.5 V, V_I = 0.85 V		3.8	7	mA
$I_{CC(off)}$	Off-state supply current	53	V_{CC} = 5.5 V, V_{in} = 0, V_I = 0.85 V		6	9	mA

§ All typical values are at V_{CC} = 5 V, T_A = 25°C.

output capacitance, V_{CC} and GND terminals open, T_A = 25°C

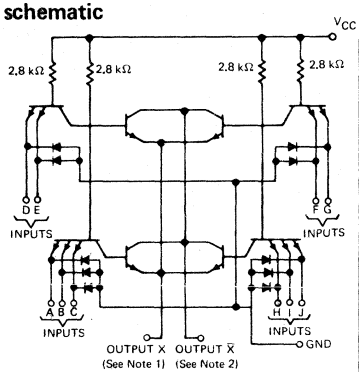
PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
C_x	Effective capacitance of output transistor Q_1	79	f = 1 MHz		1.3		pF

–SEE ORDERING INSTRUCTIONS PAGE 1-1–

CIRCUIT TYPE SN74H62
3-2-2-3-INPUT AND-OR EXPANDER

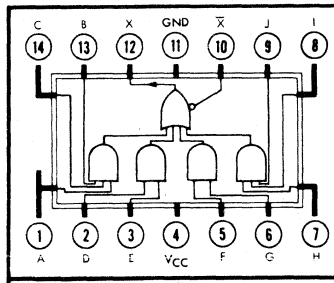
(FOR USE WITH SN74H50, SN74H53, SN74H55 CIRCUITS)

schematic



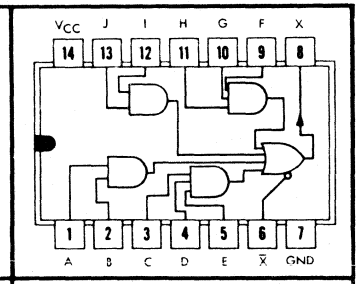
NOTES: 1. Connect to X input of SN74H50, SN74H53, or SN74H55 circuit.
2. Connect to $\overline{X}$ input of SN74H50, SN74H53, or SN74H55 circuit.
3. Component values shown are nominal.

S
FLAT PACKAGE (TOP VIEW)



positive logic:
X = (ABC) + (DE) + (FG) + (HIJ)
when connected to X and $\overline{X}$ pins of SN74H50, SN74H53, or SN74H55 circuit.

J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



positive logic:
X = (AB) + (CDE) + (FGH) + (IJ)
when connected to X and $\overline{X}$ pins of SN74H50, SN74H53, or SN74H55 circuit.

recommended operating conditions

Supply Voltage V_{CC} . . . . . 4.75 V to 5.25 V
Maximum number of expanders that may be fanned-in to one SN74H50, SN74H53, or SN74H55 circuit 1

electrical characteristics (unless otherwise noted T_A = 0°C to 70°C)

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP §	MAX	UNIT
$V_{in(1)}$	Logical 1 input voltage required at all input terminals of one AND section to ensure output is in the on state	48	V_{CC} = 4.75 V	2			V
$V_{in(0)}$	Logical 0 input voltage required at one input terminal of each AND section to ensure output is in the off state	49	V_{CC} = 4.75 V			0.8	V
V_{on}	On-state output voltage	48	V_{CC} = 4.75 V, V_{in} = 2 V, V_I = 1 V, I_{on} = 6.3 mA, T_A = 0°C			0.4	V
			V_{CC} = 5.25 V, V_{in} = 2 V, V_I = 0.6 V, I_{on} = 7.4 mA, T_A = 70°C			0.4	V
I_{off}	Off-state output current	49	V_{CC} = 4.75 V, V_{in} = 0.8 V, V_I = 4.5 V, R = 575 Ω, T_A = 0°C			570	μA
I_{on}	On-state output current	50	V_{CC} = 4.75 V, V_{in} = 2 V, V_I = 1 V, T_A = 0°C	−600			μA
$I_{in(0)}$	Logical 0 level input current (each input)	51	V_{CC} = 5.25 V, V_{in} = 0.4 V			−2	mA
$I_{in(1)}$	Logical 1 level input current (each input)	52	V_{CC} = 5.25 V, V_{in} = 2.4 V			50	μA
			V_{CC} = 5.25 V, V_{in} = 5.5 V			1	mA
$I_{CC(on)}$	On-state supply current	53	V_{CC} = 5.25 V, V_{in} = 4.5 V, V_I = 0.85 V		3.8	7	mA
$I_{CC(off)}$	Off-state supply current	53	V_{CC} = 5.25 V, V_{in} = 0, V_I = 0.85 V		6	9	mA

§ All typical values are at V_{CC} = 5 V, T_A = 25°C.

output capacitance, V_{CC} and GND terminals open, T_A = 25°C

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
C_x	Effective capacitance of output transistor Q_1	79	f = 1 MHz		1.3		pF

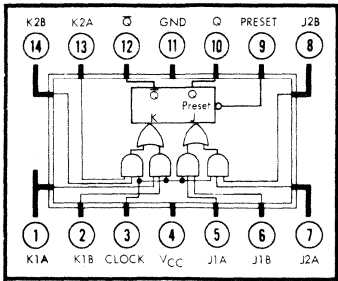
—SEE ORDERING INSTRUCTIONS PAGE 1-1—

logic

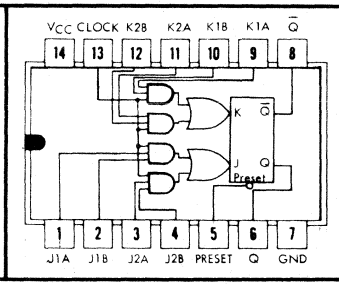
TRUTH TABLE		
t_n		t_{n+1}
J	K	Q
0	0	Q_n
0	1	0
1	0	1
1	1	$\overline{Q}_n$

NOTES: 1. J = (J1A • J1B) + (J2A • J2B)
2. K = (K1A • K1B) + (K2A • K2B)
3. t_n = Bit time before clock pulse.
4. t_{n+1} = Bit time after clock pulse.

S
FLAT PACKAGE (TOP VIEW)



J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



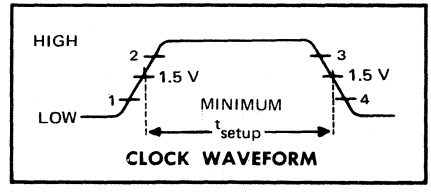
positive logic: Low input to preset sets Q to logical 1
Preset is independent of clock.

description

These J-K flip-flops are based on the master-slave principle. The AND-OR gate inputs for entry into the master section are controlled by the clock pulse. The clock pulse also regulates the circuitry which connects the master and slave sections. The sequence of operation is as follows:

1. Isolate slave from master
2. Enter information from AND-OR gate inputs to master
3. Disable AND-OR gate inputs
4. Transfer information from master to slave.

Logical state of J and K inputs must not be allowed to change when the clock pulse is in a high state.



CLOCK WAVEFORM

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply Voltage V_{CC}: SN54H71 Circuits	4.5	5	5.5	V
SN74H71 Circuits	4.75	5	5.25	V
Operating Free-Air Temperature Range, T_A: SN54H71 Circuits	−55	25	125	°C
SN74H71 Circuits	0	25	70	°C
Normalized Fan-Out From Each Output, N			10	
Width of Clock Pulse, $t_{p(clock)}$ (See Figure 77)	12			ns
Width of Preset Pulse, $t_{p(preset)}$ (See Figure 78)	16			ns
Input Setup Time, t_{setup} (See Above)	≥ $t_{p(clock)}$			
Input Hold Time, t_{hold}	0			

—SEE ORDERING INSTRUCTIONS PAGE 1-1—

electrical characteristics (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS†	MIN	TYP§	MAX	UNIT
$V_{in(1)}$	Input voltage required to ensure logical 1 at any input terminal	54 and 55	V_{CC} = MIN	2			V
$V_{in(0)}$	Input voltage required to ensure logical 0 at any input terminal	54 and 55	V_{CC} = MIN			0.8	V
$V_{out(1)}$	Logical 1 output voltage	54	V_{CC} = MIN, I_{load} = −500 μA	2.4			V
$V_{out(0)}$	Logical 0 output voltage	55	V_{CC} = MIN, I_{sink} = 20 mA			0.4	V
$I_{in(0)}$	Logical 0 level input current at J1A, J1B, J2A, J2B, K1A, K1B, K2A, or K2B	56	V_{CC} = MAX, V_{in} = 0.4 V			−2	mA
$I_{in(0)}$	Logical 0 level input current at preset	56	V_{CC} = MAX, V_{in} = 0.4 V			−6	mA
$I_{in(0)}$	Logical 0 level input current at clock	56	V_{CC} = MAX, V_{in} = 0.4 V			−4	mA
$I_{in(1)}$	Logical 1 level input current at J1A, J1B, J2A, J2B, K1A, K1B, K2A, or K2B	57	V_{CC} = MAX, V_{in} = 2.4 V			50	μA
			V_{CC} = MAX, V_{in} = 5.5 V			1	mA
$I_{in(1)}$	Logical 1 level input current at preset	57	V_{CC} = MAX, V_{in} = 2.4 V			150	μA
			V_{CC} = MAX, V_{in} = 5.5 V			1	mA
$I_{in(1)}$	Logical 1 level input current at clock	57	V_{CC} = MAX, V_{in} = 2.4 V			100	μA
			V_{CC} = MAX, V_{in} = 5.5 V			1	mA
I_{OS}	Short-circuit output current‡	58	V_{CC} = MAX, V_{in} = 0	−40		−100	mA
I_{CC}	Supply current	57	V_{CC} = MAX		19	30	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

‡Not more than one output should be shorted at a time, and duration of short-circuit test should not exceed 1 second.

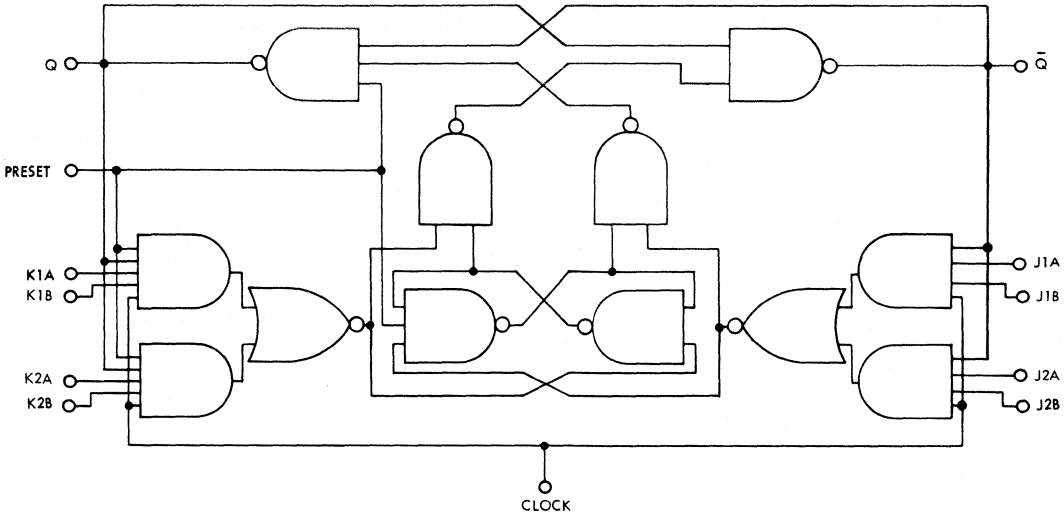
§ All typical values are at V_{CC} = 5 V, T_A = 25°C.

switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10

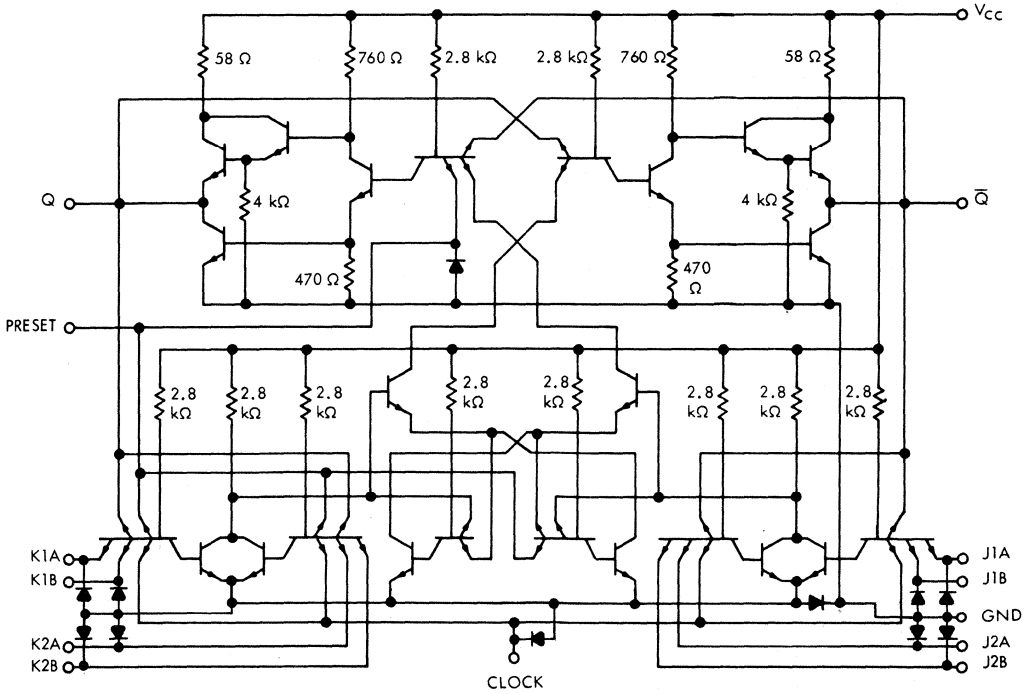
PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{clock}	Maximum clock frequency	77	C_L = 25 pF, R_L = 280 Ω	25	30		MHz
t_{pd1}	Propagation delay time to logical 1 level from preset to output	78	C_L = 25 pF, R_L = 280 Ω		6	13	ns
t_{pd0}	Propagation delay time to logical 0 level from preset to output	78	C_L = 25 pF, R_L = 280 Ω		12	24	ns
t_{pd1}	Propagation delay time to logical 1 level from clock to output	77	C_L = 25 pF, R_L = 280 Ω		16	21	ns
t_{pd0}	Propagation delay time to logical 0 level from clock to output	77	C_L = 25 pF, R_L = 280 Ω		22	27	ns

–SEE ORDERING INSTRUCTIONS PAGE 1-1–

functional block diagram



schematic



Component values shown are nominal.

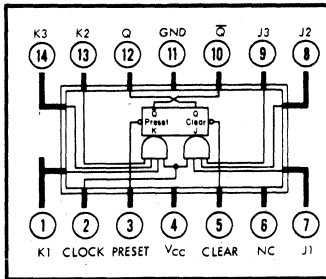
CIRCUIT TYPES SN54H72, SN74H72
J-K MASTER-SLAVE FLIP-FLOPS

logic

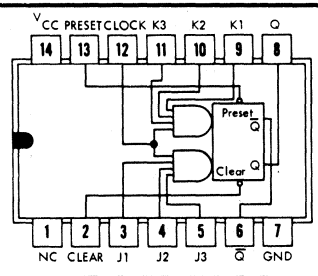
TRUTH TABLE		
t_n		t_{n+1}
J	K	Q
0	0	Q_n
0	1	0
1	0	1
1	1	$\overline{Q}_n$

NOTES: 1. $J = J1 \cdot J2 \cdot J3$
2. $K = K1 \cdot K2 \cdot K3$
3. t_n = Bit time before clock pulse.
4. t_{n+1} = Bit time after clock pulse.

S
FLAT PACKAGE (TOP VIEW)



J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



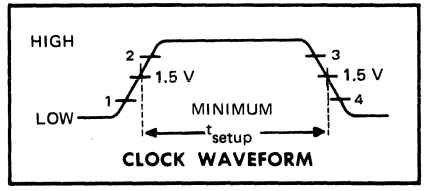
positive logic: Low input to preset sets Q to logical 1
Low input to clear sets Q to logical 0
Preset and clear are independent of clock

description

These J-K flip-flops are based on the master-slave principle. The AND gate inputs for entry into the master section are controlled by the clock pulse. The clock pulse also regulates the circuitry which connects the master and slave sections. The sequence of operation is as follows:

1. Isolate slave from master
2. Enter information from AND gate inputs to master
3. Disable AND gate inputs
4. Transfer information from master to slave.

Logical state of J and K inputs must not be allowed to change when the clock pulse is in a high state.



CLOCK WAVEFORM

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply Voltage V_{CC}: SN54H72 Circuits	4.5	5	5.5	V
SN74H72 Circuits	4.75	5	5.25	V
Operating Free-Air Temperature Range, T_A: SN54H72 Circuits	−55	25	125	°C
SN74H72 Circuits	0	25	70	°C
Normalized Fan-Out From Each Output, N			10	
Width of Clock Pulse, $t_{p(clock)}$ (See Figure 77)	12			ns
Width of Preset Pulse, $t_{p(preset)}$ (See Figure 78)	16			ns
Width of Clear Pulse, $t_{p(clear)}$ (See Figure 78)	16			ns
Input Setup Time, t_{setup} (See Above)	≥ $t_{p(clock)}$			
Input Hold Time, t_{hold}	0			

—SEE ORDERING INSTRUCTIONS PAGE 1-1—

electrical characteristics (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS†		MIN	TYP§	MAX	UNIT
$V_{in(1)}$	Input voltage required to ensure logical 1 at any input terminal	59 and 60	V_{CC} = MIN		2			V
$V_{in(0)}$	Input voltage required to ensure logical 0 at any input terminal	59 and 60	V_{CC} = MIN				0.8	V
$V_{out(1)}$	Logical 1 output voltage	59	V_{CC} = MIN,	I_{load} = −500 μA	2.4			V
$V_{out(0)}$	Logical 0 output voltage	60	V_{CC} = MIN,	I_{sink} = 20 mA			0.4	V
$I_{in(0)}$	Logical 0 level input current at J1, J2, J3, K1, K2, K3, or clock	61	V_{CC} = MAX,	V_{in} = 0.4 V			−2	mA
$I_{in(0)}$	Logical 0 level input current at preset or clear	61	V_{CC} = MAX,	V_{in} = 0.4 V			−4	mA
$I_{in(1)}$	Logical 1 level input current at J1, J2, J3, K1, K2, or K3	62	V_{CC} = MAX,	V_{in} = 2.4 V			50	μA
			V_{CC} = MAX,	V_{in} = 5.5 V			1	mA
$I_{in(1)}$	Logical 1 level input current at clock	62	V_{CC} = MAX,	V_{in} = 2.4 V			50	μA
			V_{CC} = MAX,	V_{in} = 5.5 V			1	mA
$I_{in(1)}$	Logical 1 level input current at preset or clear	62	V_{CC} = MAX,	V_{in} = 2.4 V			100	μA
			V_{CC} = MAX,	V_{in} = 5.5 V			1	mA
I_{OS}	Short-circuit output current‡	63	V_{CC} = MAX,	V_{in} = 0	−40		−100	mA
I_{CC}	Supply current	62	V_{CC} = MAX			16	25	mA

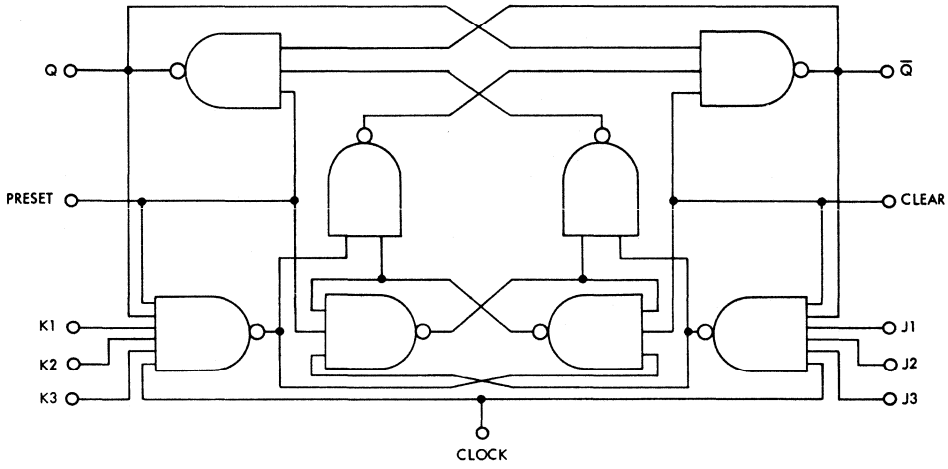
†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
‡Not more than one output should be shorted at a time, and duration of short-circuit test should not exceed 1 second.
§All typical values are at V_{CC} = 5 V, T_A = 25°C.

switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10

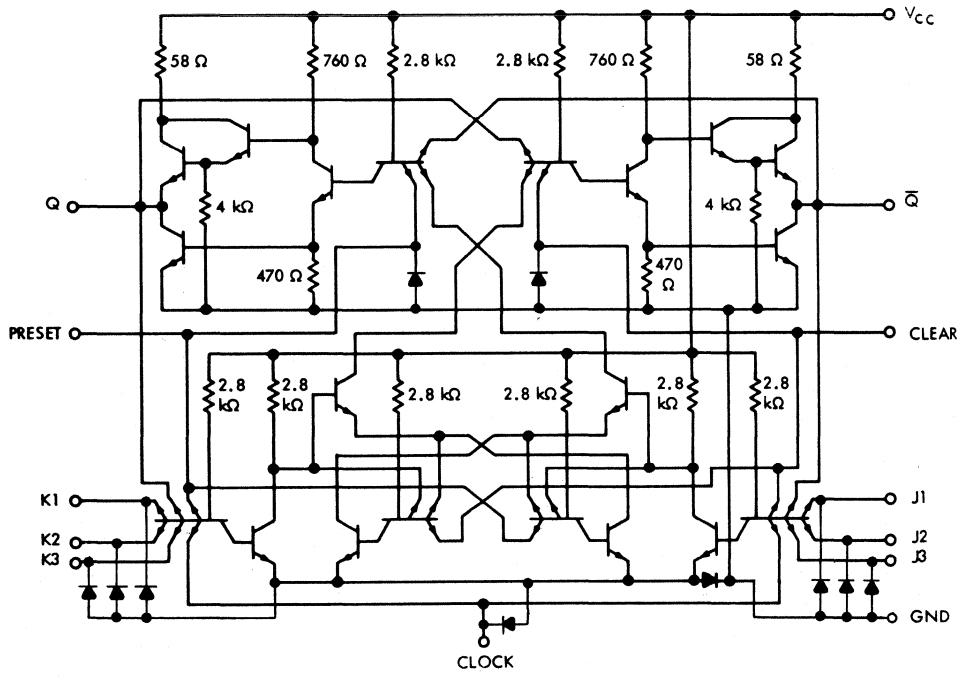
PARAMETER		TEST FIGURE	TEST CONDITIONS		MIN	TYP	MAX	UNIT
f_{clock}	Maximum clock frequency	77	C_L = 25 pF,	R_L = 280 Ω	25	30		MHz
t_{pd1}	Propagation delay time to logical 1 level from clear or preset to output	78	C_L = 25 pF,	R_L = 280 Ω		6	13	ns
t_{pd0}	Propagation delay time to logical 0 level from clear or preset to output	78	C_L = 25 pF,	R_L = 280 Ω		12	24	ns
t_{pd1}	Propagation delay time to logical 1 level from clock to output	77	C_L = 25 pF,	R_L = 280 Ω		16	21	ns
t_{pd0}	Propagation delay time to logical 0 level from clock to output	77	C_L = 25 pF,	R_L = 280 Ω		22	27	ns

—SEE ORDERING INSTRUCTIONS PAGE 1-1—

functional block diagram



schematic



Component values shown are nominal.

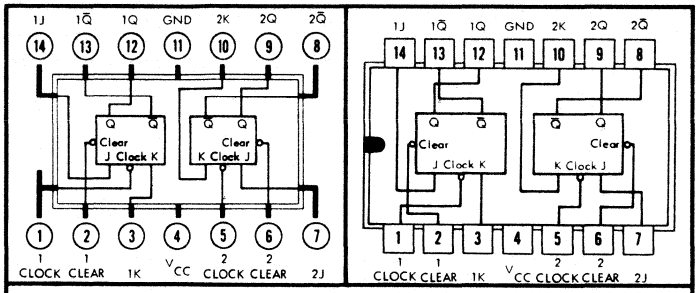
logic

TRUTH TABLE		
t_n		t_{n+1}
J	K	Q
0	0	Q_n
0	1	0
1	0	1
1	1	$\overline{Q}_n$

NOTES: 1. t_n = Bit time before clock pulse.
2. t_{n+1} = Bit time after clock pulse.

S
FLAT PACKAGE (TOP VIEW)

J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



positive logic: Low input to clear sets Q to logical 0
Clear is independent of clock

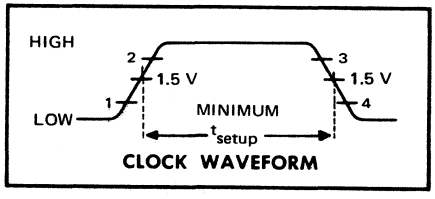
description

These J-K flip-flops are based on the master-slave principle. The AND gate inputs for entry into the master section are controlled by the clock pulse. The clock pulse also regulates the circuitry which connects the master and slave sections.

The sequence of operation is as follows:

1. Isolate slave from master
2. Enter information from AND gate inputs to master
3. Disable AND gate inputs
4. Transfer information from master to slave.

Logical state of J and K inputs must not be allowed to change when the clock pulse is in a high state.



CLOCK WAVEFORM

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply Voltage V_{CC}:	SN54H73 Circuits	4.5	5	5.5	V
	SN74H73 Circuits	4.75	5	5.25	V
Operating Free-Air Temperature Range, T_A:	SN54H73 Circuits	−55	25	125	°C
	SN74H73 Circuits	0	25	70	°C
Normalized Fan-Out From Each Output, N				10	
Width of Clock Pulse, $t_{p(clock)}$ (See Figure 77)		12			ns
Width of Clear Pulse, $t_{p(clear)}$ (See Figure 78)		16			ns
Input Setup Time, t_{setup} (See Above)		≥ $t_{p(clock)}$			
Input Hold Time, t_{hold}		0			

—SEE ORDERING INSTRUCTIONS PAGE 1-1—

electrical characteristics (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS†	MIN	TYP §	MAX	UNIT
$V_{in(1)}$	Input voltage required to ensure logical 1 at any input terminal	64 and 65	V_{CC} = MIN	2			V
$V_{in(0)}$	Input voltage required to ensure logical 0 at any input terminal	64 and 65	V_{CC} = MIN			0.8	V
$V_{out(1)}$	Logical 1 output voltage	64	V_{CC} = MIN, I_{load} = −500 μA	2.4			V
$V_{out(0)}$	Logical 0 output voltage	65	V_{CC} = MIN, I_{sink} = 20 mA			0.4	V
$I_{in(0)}$	Logical 0 level input current at J, K, or clock	66	V_{CC} = MAX, V_{in} = 0.4 V			−2	mA
$I_{in(0)}$	Logical 0 level input current at clear	66	V_{CC} = MAX, V_{in} = 0.4 V			−4	mA
$I_{in(1)}$	Logical 1 level input current at J or K	67	V_{CC} = MAX, V_{in} = 2.4 V			50	μA
			V_{CC} = MAX, V_{in} = 5.5 V			1	mA
$I_{in(1)}$	Logical 1 level input current at clock	67	V_{CC} = MAX, V_{in} = 2.4 V			50	μA
			V_{CC} = MAX, V_{in} = 5.5 V			1	mA
$I_{in(1)}$	Logical 1 level input current at clear	67	V_{CC} = MAX, V_{in} = 2.4 V			100	μA
			V_{CC} = MAX, V_{in} = 5.5 V			1	mA
I_{OS}	Short-circuit output current‡	68	V_{CC} = MAX, V_{in} = 0	−40		−100	mA
I_{CC}	Supply current	67	V_{CC} = MAX		32	50	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

‡Not more than one output should be shorted at a time, and duration of short-circuit test should not exceed 1 second.

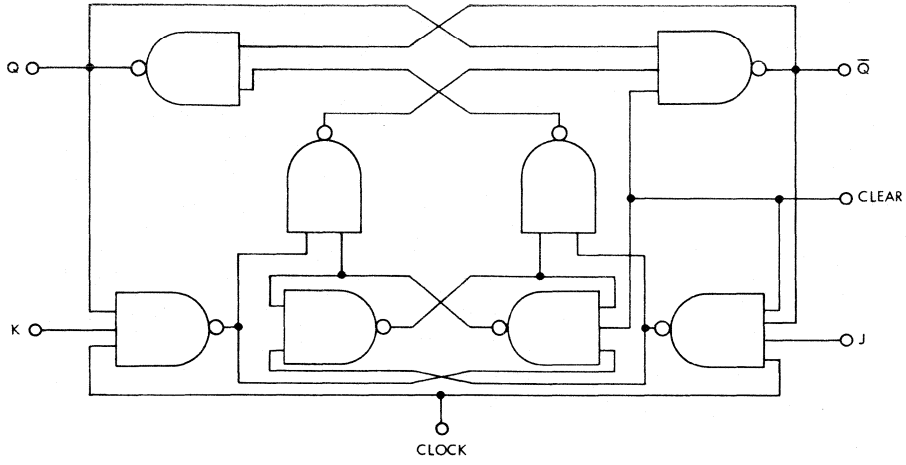
§ All typical values are at V_{CC} = 5 V, T_A = 25°C.

switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10

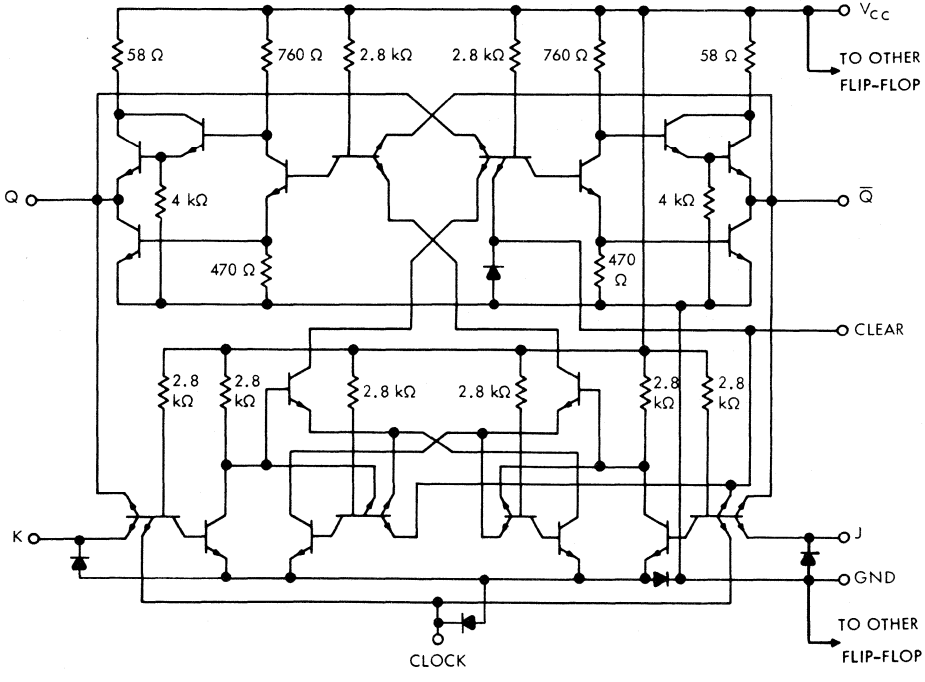
PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{clock}	Maximum clock frequency	77	C_L = 25 pF, R_L = 280 Ω	25	30		MHz
t_{pd1}	Propagation delay time to logical 1 level from clear to output	78	C_L = 25 pF, R_L = 280 Ω		6	13	ns
t_{pd0}	Propagation delay time to logical 0 level from clear to output	78	C_L = 25 pF, R_L = 280 Ω		12	24	ns
t_{pd1}	Propagation delay time to logical 1 level from clock to output	77	C_L = 25 pF, R_L = 280 Ω		16	21	ns
t_{pd0}	Propagation delay time to logical 0 level from clock to output	77	C_L = 25 pF, R_L = 280 Ω		22	27	ns

—SEE ORDERING INSTRUCTIONS PAGE 1-1—

functional block diagram (each flip-flop)



schematic (each flip-flop)



Component values shown are nominal.
Resistor values are in ohms.

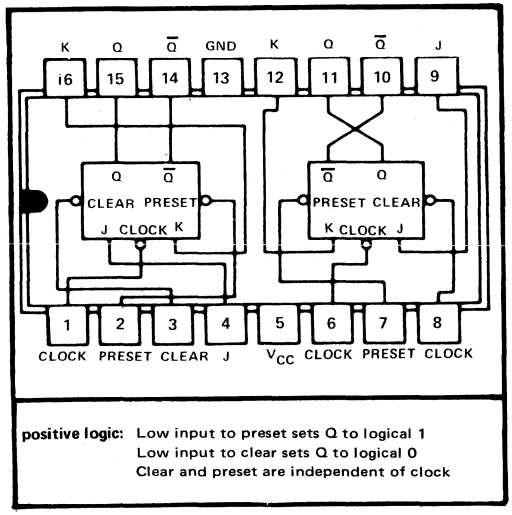
–SEE ORDERING INSTRUCTIONS PAGE 1-1–

logic

TRUTH TABLE		
t_n		t_{n+1}
J	K	Q
0	0	Q_n
0	1	0
1	0	1
1	1	$\overline{Q}_n$

NOTES: 1. t_n = Bit time before clock pulse
2. t_{n+1} = Bit time after clock pulse

J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



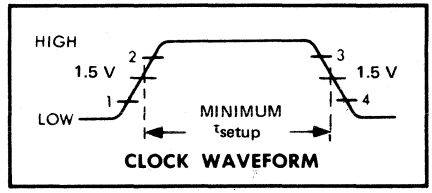
positive logic: Low input to preset sets Q to logical 1
Low input to clear sets Q to logical 0
Clear and preset are independent of clock

description

These dual J-K flip-flops are based on the master-slave principle. Inputs to the master section are controlled by the clock pulse. The clock pulse also regulates the circuitry which connects the master and slave sections. The sequence of operation is as follows:

1. Isolate slave from master
2. Enter information from J and K inputs to master
3. Disable J and K inputs
4. Transfer information from master to slave.

Logical state of J and K inputs must not be allowed to change when the clock pulse is in a high state.



CLOCK WAVEFORM

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply Voltage V_{CC}: SN54H76 Circuits	4.5	5	5.5	V
SN74H76 Circuits	4.75	5	5.25	V
Operating Free-Air Temperature Range, T_A: SN54H76 Circuits	−55	25	125	°C
SN74H76 Circuits	0	25	70	°C
Normalized Fan-Out From Each Output, N			10	
Width of Clock Pulse, $t_{p(clock)}$ (See Figure 77)	12			ns
Width of Preset Pulse, $t_{p(preset)}$ (See Figure 78)	16			ns
Width of Clear Pulse, $t_{p(clear)}$ (See Figure 78)	$\geq t_{p(clock)}$			
Input Setup Time, t_{setup} (See Above)				
Input Hold Time, t_{hold}	0			

—SEE ORDERING INSTRUCTIONS PAGE 1-1—

electrical characteristics (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS†	MIN	TYP§	MAX	UNIT
$V_{in(1)}$	Input voltage required to ensure logical 1 at any input terminal	64 and 65	V_{CC} = MIN	2			V
$V_{in(0)}$	Input voltage required to ensure logical 0 at any input terminal	64 and 65	V_{CC} = MIN			0.8	V
$V_{out(1)}$	Logical 1 output voltage	64	V_{CC} = MIN, I_{load} = −500 μA	2.4			V
$V_{out(0)}$	Logical 0 output voltage	65	V_{CC} = MIN, I_{sink} = 20 mA			0.4	V
$I_{in(0)}$	Logical 0 level input current at J, K, or clock	66	V_{CC} = MAX, V_{in} = 0.4 V			−2	mA
$I_{in(0)}$	Logical 0 level input current at clear or preset	66	V_{CC} = MAX, V_{in} = 0.4 V			−4	mA
$I_{in(1)}$	Logical 1 level input current at J, K, or clock	67	V_{CC} = MAX, V_{in} = 2.4 V			50	μA
			V_{CC} = MAX, V_{in} = 5.5 V			1	mA
$I_{in(1)}$	Logical 1 level input current at clear or preset	67	V_{CC} = MAX, V_{in} = 2.4 V			100	μA
			V_{CC} = MAX, V_{in} = 5.5 V			1	mA
I_{OS}	Short-circuit output current‡	68	V_{CC} = MAX, V_{in} = 0	−40		−100	mA
I_{CC}	Supply current	67	V_{CC} = MAX, V_{in} = 4.5 V		32	50	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

‡ Not more than one output should be shorted at a time.

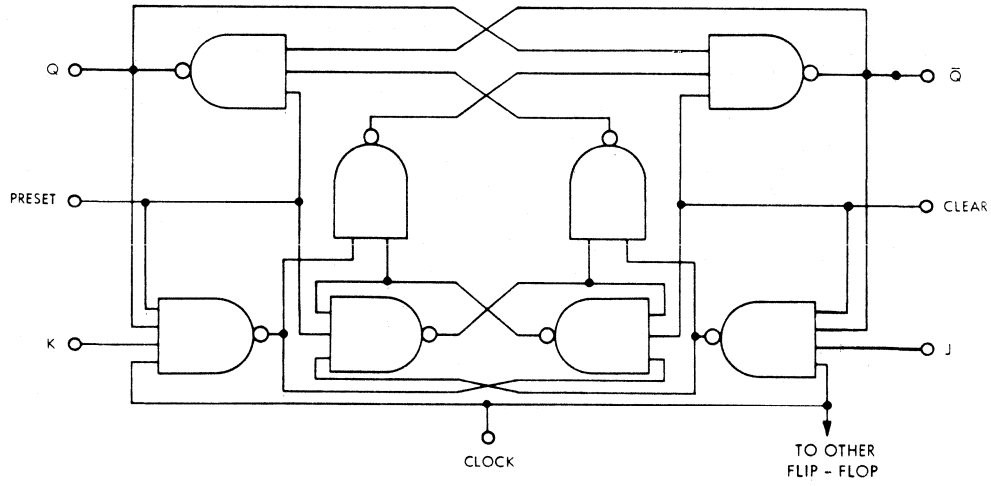
§ All typical values are at V_{CC} = 5 V, T_A = 25°C.

switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10

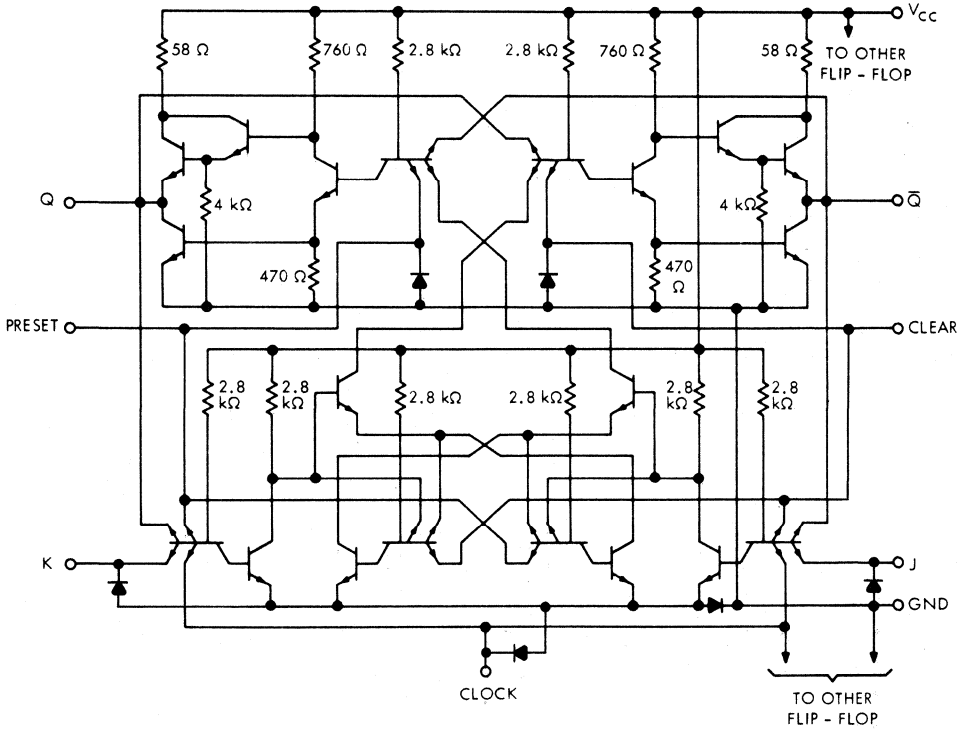
PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{clock}	Maximum clock frequency	77	C_L = 25 pF, R_L = 280 Ω	25	30		MHz
t_{pd1}	Propagation delay time to logical 1 level from clear or preset to output	78	C_L = 25 pF, R_L = 280 Ω		6	13	ns
t_{pd0}	Propagation delay time to logical 0 level from clear or preset to output	78	C_L = 25 pF, R_L = 280 Ω		12	24	ns
t_{pd1}	Propagation delay time to logical 1 level from clock to output	77	C_L = 25 pF, R_L = 280 Ω		16	21	ns
t_{pd0}	Propagation delay time to logical 0 level from clock to output	77	C_L = 25 pF, R_L = 280 Ω		22	27	ns

—SEE ORDERING INSTRUCTIONS PAGE 1-1—

functional block diagram (each flip-flop)



schematic (each flip-flop)



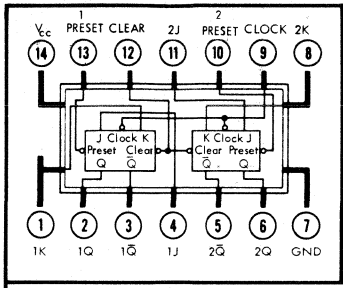
Component values shown are nominal.

logic

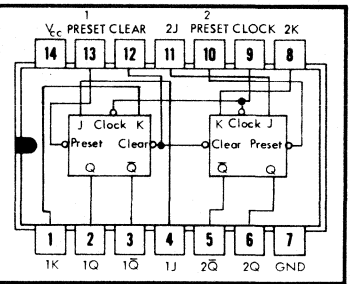
TRUTH TABLE		
t_n		t_{n+1}
J	K	Q
0	0	Q_n
0	1	0
1	0	1
1	1	$\overline{Q}_n$

NOTES: 1. t_n = Bit time before clock pulse.
2. t_{n+1} = Bit time after clock pulse.

S
FLAT PACKAGE (TOP VIEW)



J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



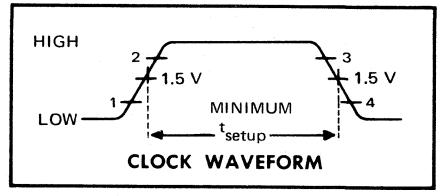
positive logic: Low input to preset sets Q to logical 1
Low input to clear sets Q to logical 0
Preset and clear are independent of clock

description

These J-K flip-flops are based on the master-slave principle. Inputs to the master section are controlled by the clock pulse. The clock pulse also regulates the circuitry which connects the master and slave sections.
The sequence of operation is as follows:

1. Isolate slave from master
2. Enter information from J and K inputs to master
3. Disable J and K inputs
4. Transfer information from master to slave.

Logical state of J and K inputs must not be allowed to change when the clock pulse is in a high state.



CLOCK WAVEFORM

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply Voltage V_{CC}:	SN54H78 Circuits	4.5	5	5.5	V
	SN74H78 Circuits	4.75	5	5.25	V
Operating Free-Air Temperature Range, T_A:	SN54H78 Circuits	−55	25	125	°C
	SN74H78 Circuits	0	25	70	°C
Normalized Fan-Out From Each Output, N				10	
Width of Clock Pulse, $t_{p(clock)}$ (See Figure 77)		12			ns
Width of Preset Pulse, $t_{p(preset)}$ (See Figure 78)		16			ns
Width of Clear Pulse, $t_{p(clear)}$ (See Figure 78)		16			ns
Input Setup Time, t_{setup} (See Above)		$\geq t_{p(clock)}$			
Input Hold Time, t_{hold}		0			

—SEE ORDERING INSTRUCTIONS PAGE 1-1—

electrical characteristics (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS†		MIN	TYP§	MAX	UNIT
$V_{in(1)}$	Input voltage required to ensure logical 1 at any input terminal	64 and 65	V_{CC} = MIN		2			V
$V_{in(0)}$	Input voltage required to ensure logical 0 at any input terminal	64 and 65	V_{CC} = MIN				0.8	V
$V_{out(1)}$	Logical 1 output voltage	64	V_{CC} = MIN,	I_{load} = −500 μA	2.4			V
$V_{out(0)}$	Logical 0 output voltage	65	V_{CC} = MIN,	I_{sink} = 20 mA			0.4	V
$I_{in(0)}$	Logical 0 level input current at J or K	66	V_{CC} = MAX,	V_{in} = 0.4 V			−2	mA
$I_{in(0)}$	Logical 0 level input current at preset or clock	66	V_{CC} = MAX,	V_{in} = 0.4 V			−4	mA
$I_{in(0)}$	Logical 0 level input current at clear	66	V_{CC} = MAX,	V_{in} = 0.4 V			−8	mA
$I_{in(1)}$	Logical 1 level input current at J or K	67	V_{CC} = MAX,	V_{in} = 2.4 V			50	μA
			V_{CC} = MAX,	V_{in} = 5.5 V			1	mA
$I_{in(1)}$	Logical 1 level input current at preset or clock	67	V_{CC} = MAX,	V_{in} = 2.4 V			100	μA
			V_{CC} = MAX,	V_{in} = 5.5 V			1	mA
$I_{in(1)}$	Logical 1 level input current at clear	67	V_{CC} = MAX,	V_{in} = 2.4 V			200	μA
			V_{CC} = MAX,	V_{in} = 5.5 V			1	mA
I_{OS}	Short-circuit output current‡	69	V_{CC} = MAX,	V_{in} = 0	−40		−100	mA
I_{CC}	Supply current	67	V_{CC} = MAX			32	50	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

‡Not more than one output should be shorted at a time, and duration of short-circuit test should not exceed 1 second.

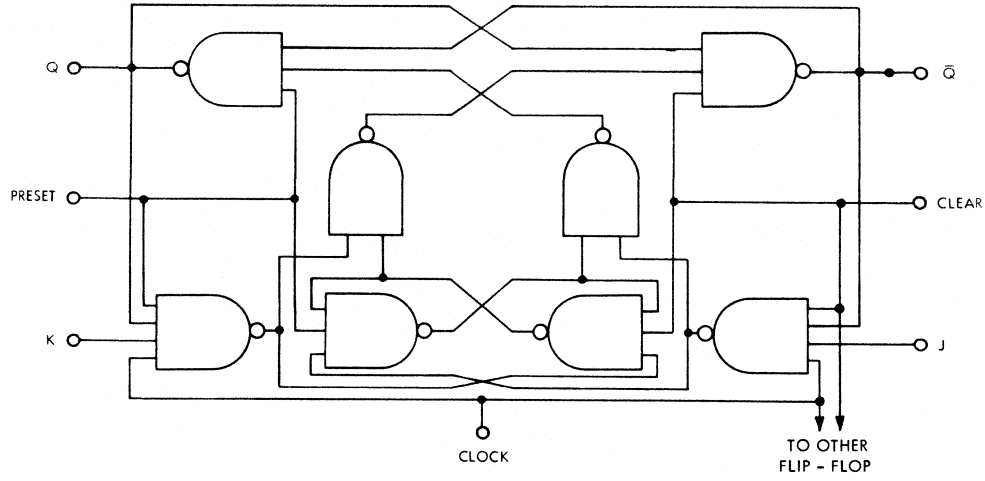
§ All typical values are at V_{CC} = 5 V, T_A = 25°C.

switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10

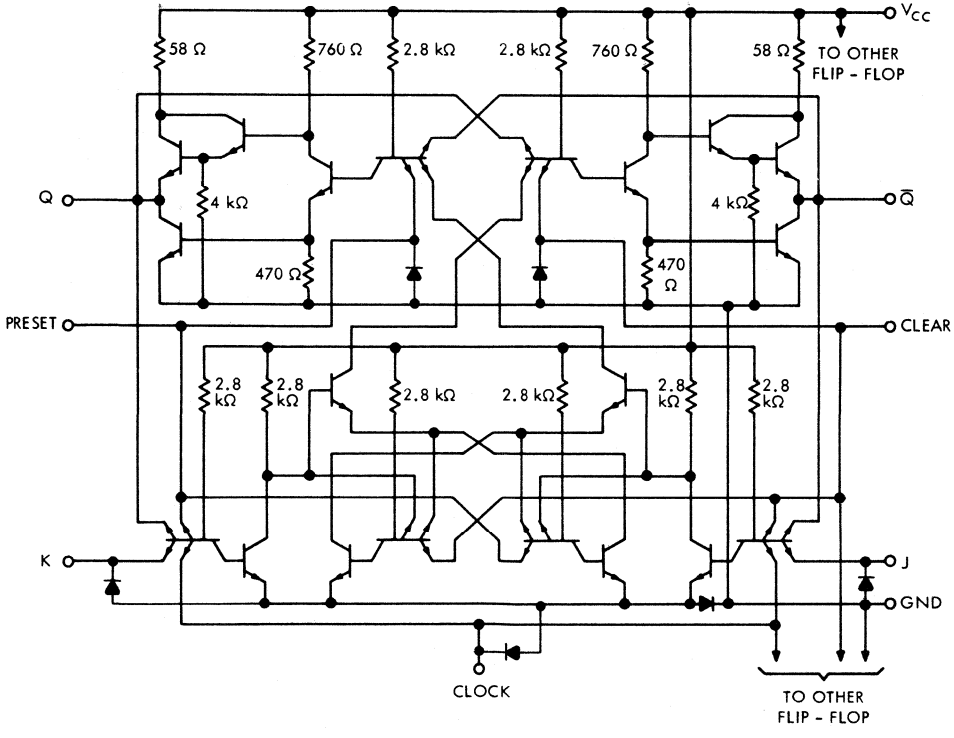
PARAMETER		TEST FIGURE	TEST CONDITIONS		MIN	TYP	MAX	UNIT
f_{clock}	Maximum clock frequency	77	C_L = 25 pF,	R_L = 280 Ω	25	30		MHz
t_{pd1}	Propagation delay time to logical 1 level from clear to output	78	C_L = 25 pF,	R_L = 280 Ω		6	13	ns
t_{pd0}	Propagation delay time to logical 0 level from clear to output	78	C_L = 25 pF,	R_L = 280 Ω		12	24	ns
t_{pd1}	Propagation delay time to logical 1 level from clock to output	77	C_L = 25 pF,	R_L = 280 Ω		16	21	ns
t_{pd0}	Propagation delay time to logical 0 level from clock to output	77	C_L = 25 pF,	R_L = 280 Ω		22	27	ns

—SEE ORDERING INSTRUCTIONS PAGE 1-1—

functional block diagram (each flip-flop)



schematic (each flip-flop)



Component values shown are nominal.

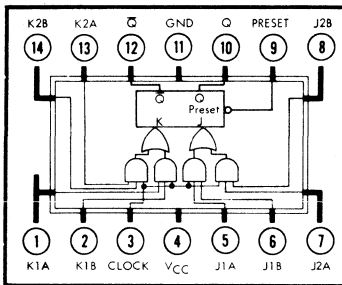
CIRCUIT TYPES SN54H101, SN74H101
J-K EDGE-TRIGGERED FLIP-FLOPS

logic

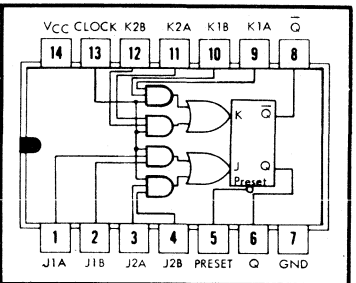
TRUTH TABLE		
t_n		t_{n+1}
J	K	Q
0	0	Q_n
0	1	0
1	0	1
1	1	$\overline{Q}_n$

NOTES: 1. J = (J1A • J1B) + (J2A • J2B)
2. K = (K1A • K1B) + (K2A • K2B)
3. t_n = Bit time before clock pulse
4. t_{n+1} = Bit time after clock pulse

S
FLAT PACKAGE (TOP VIEW)



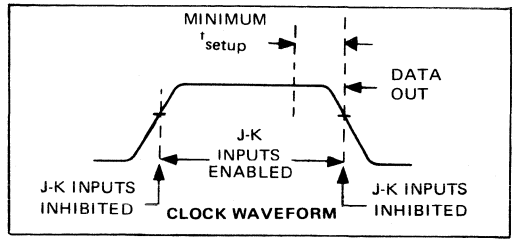
J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



positive logic: Low input to preset sets Q to logical 1
Preset is independent of clock.

description

These monolithic J-K flip-flops are negative-edge-triggered. The AND-OR gate inputs are inhibited while the clock input is low; when the clock goes high, the inputs are enabled and data will be accepted. Logical state of J and K inputs may be allowed to change when the clock pulse is in a high state and bistable will perform according to the truth table as long as minimum set-up times are observed. Input data is transferred to the outputs on the negative edge of the clock pulse.



recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply Voltage V_{CC}: SN54H101 Circuits	4.5	5	5.5	V
SN74H101 Circuits	4.75	5	5.25	V
Operating Free-Air Temperature Range, T_A: SN54H101 Circuits	−55	25	125	°C
SN74H101 Circuits	0	25	70	°C
Normalized Fan-Out From Each Output, N			10	
Width of Clock Pulse, $t_{p(clock)}$ (See Figure 77)	10			ns
Width of Preset Pulse, $t_{p(preset)}$ (See Figure 78)	16			ns
Input Setup Time, t_{setup} (See Above): Logical 1	10			ns
Logical 0	13			ns
Input Hold Time, t_{hold}	0			ns
Clock Pulse Transition Time, t_0 (See Figure 77)			150	ns

—SEE ORDERING INSTRUCTIONS PAGE 1-1—

electrical characteristics (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS†	MIN	TYP§	MAX	UNIT
$V_{in(1)}$	Input voltage required to ensure logical 1 at any input terminal	54 and 55	V_{CC} = MIN	2			V
$V_{in(0)}$	Input voltage required to ensure logical 0 at any input terminal	54 and 55	V_{CC} = MIN			0.8	V
$V_{out(1)}$	Logical 1 output voltage	54	V_{CC} = MIN, I_{load} = −500 μA	2.4	3.2		V
$V_{out(0)}$	Logical 0 output voltage	55	V_{CC} = MIN, I_{sink} = 20 mA		0.25	0.4	V
$I_{in(0)}$	Logical 0 level input current at J1A, J1B, J2A, J2B, K1A, K1B, K2A, K2B,or preset	56	V_{CC} = MAX, V_{in} = 0.4 V		−1	−2	mA
$I_{in(0)}$	Logical 0 level input current at J1A, J1B, J2A, J2B, K1A, K1B, K2A, or K2B	56	V_{CC} = MAX, V_{in} = 0.4 V		−3	−4.8	mA
$I_{in(1)}$	Logical 1 level input current at J or K	57	V_{CC} = MAX, V_{in} = 2.4 V			50	μA
			V_{CC} = MAX, V_{in} = 5.5 V			1	mA
$I_{in(1)}$	Logical 1 level input current at preset	57	V_{CC} = MAX, V_{in} = 2.4 V			100	μA
			V_{CC} = MAX, V_{in} = 5.5 V			1	mA
$I_{in(1)}$	Logical 1 level input current at clock	70	V_{CC} = MAX, V_{in} = 2.4 V			100	μA
		57	V_{CC} = MAX, V_{in} = 2.4 V	0		−1	mA
			V_{CC} = MAX, V_{in} = 5.5 V			1	mA
I_{OS}	Short-circuit output current‡	58	V_{CC} = MAX, V_{in} = 0	−40		−100	mA
I_{CC}	Supply current	57	V_{CC} = MAX		20	38	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

‡ Not more than one output should be shorted at a time, and duration of short-circuit test should not exceed 1 second.

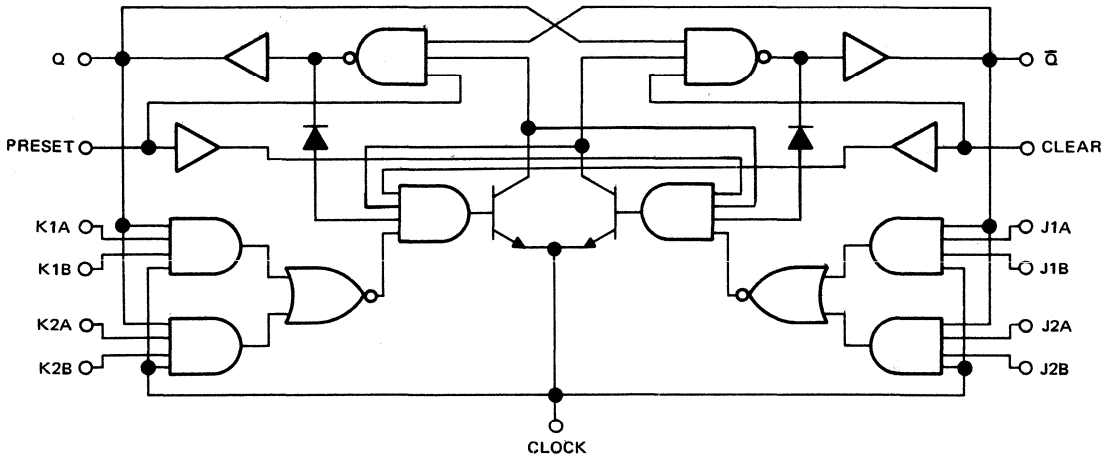
§ All typical values are at V_{CC} = 5 V, T_A = 25°C.

switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10

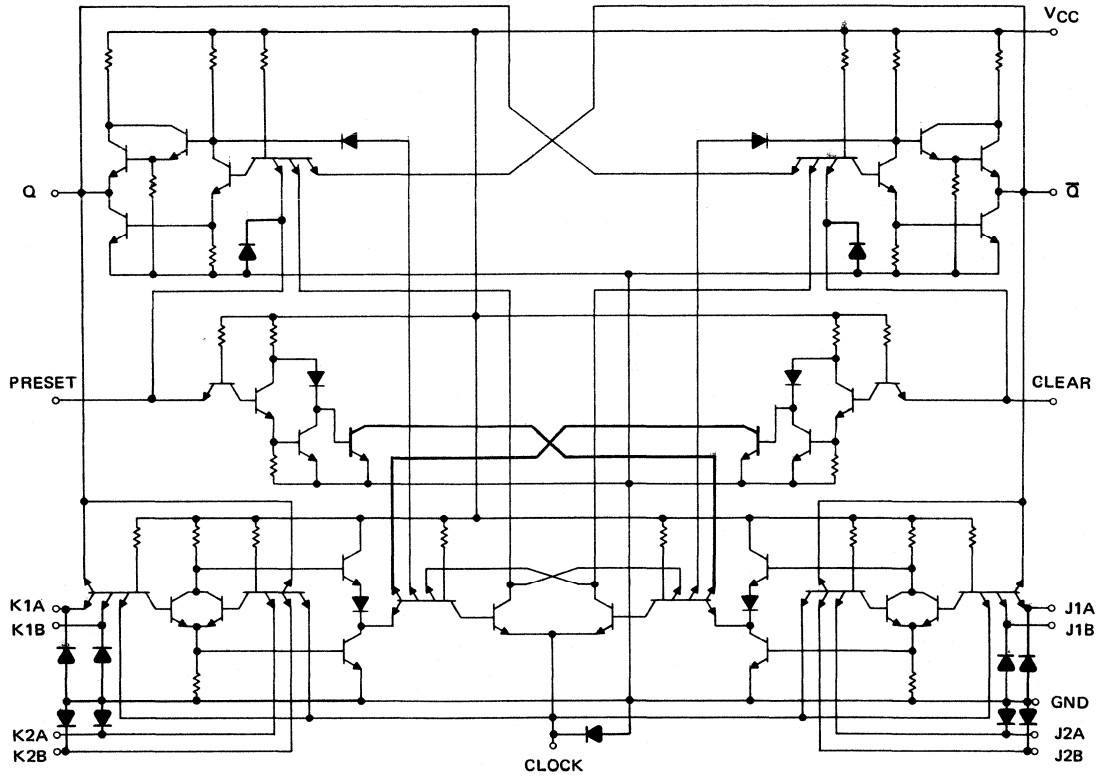
PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{clock}	Maximum input clock frequency	77	C_L = 25 pF, R_L = 280 Ω	40	50		MHz
t_{pd1}	Propagation delay time to logical 1 level from preset to output	78	C_L = 25 pF, R_L = 280 Ω		8	12	ns
t_{pd0}	Propagation delay time to logical 0 level from preset to output (clock low)	78	C_L = 25 pF, R_L = 280 Ω		23	35	ns
t_{pd0}	Propagation delay time to logical 0 level from preset to output (clock high)	78	C_L = 25 pF, R_L = 280 Ω		15	20	ns
t_{pd1}	Propagation delay time to logical 1 level from clock to output	77	C_L = 25 pF, R_L = 280 Ω		10	15	ns
t_{pd0}	Propagation delay time to logical 0 level from clock to output	77	C_L = 25 pF, R_L = 280 Ω		16	20	ns

—SEE ORDERING INSTRUCTIONS PAGE 1-1—

functional block diagram



schematic

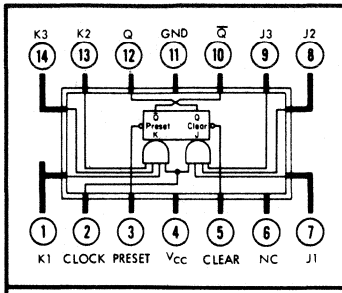


logic

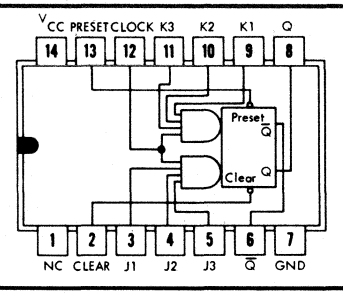
TRUTH TABLE		
t_n		t_{n+1}
J	K	Q
0	0	Q_n
0	1	0
1	0	1
1	1	$\overline{Q}_n$

NOTES: 1. J = J1 • J2 • J3
2. K = K1 • K2 • K3
3. t_n = Bit time before clock pulse
4. t_{n+1} = Bit time after clock pulse
5. NC—No Internal Connection

S
FLAT PACKAGE (TOP VIEW)



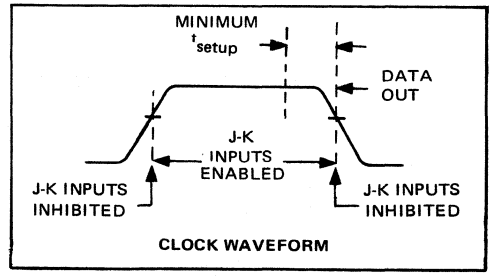
J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



positive logic: Low input to preset sets Q to logical 1
Low input to clear sets Q to logical 0
Preset and clear are independent of clock

description

These monolithic J-K flip-flops are negative edge-triggered. They feature gated J-K inputs and an asynchronous clear input. The AND gate inputs are inhibited while the clock input is low; when the clock goes high, the inputs are enabled and data will be accepted. Logical state of J and K inputs may be allowed to change when the clock pulse is in a high state and bistable will perform according to the truth table as long as minimum set-up times are observed. Input data is transferred to the outputs on the negative edge of the clock pulse.



CLOCK WAVEFORM

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply Voltage V_{CC}: SN54H102 Circuits	4.5	5	5.5	V
SN74H102 Circuits	4.75	5	5.25	V
Operating Free-Air Temperature Range, T_A: SN54H102 Circuits	−55	25	125	°C
SN74H102 Circuits	0	25	70	°C
Normalized Fan-Out From Each Output, N			10	
Width of Clock Pulse, $t_{p(clock)}$ (See Figure 77)	10			ns
Width of Preset Pulse, $t_{p(preset)}$ (See Figure 78)	15			ns
Width of Clear Pulse, $t_{p(clear)}$ (See Figure 78)	15			ns
Input Setup Time, t_{setup} (See Above): Logical 1	10			ns
Logical 0	13			ns
Input Hold Time, t_{hold}	0			ns
Clock Pulse Transition Time, t_0 (See Figure 77)			150	ns

—SEE ORDERING INSTRUCTIONS PAGE 1-1—

electrical characteristics (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS†	MIN	TYP§	MAX	UNIT
$V_{in(1)}$	Input voltage required to ensure logical 1 at any input terminal	59 and 60	V_{CC} = MIN	2			V
$V_{in(0)}$	Input voltage required to ensure logical 0 at any input terminal	59 and 60	V_{CC} = MIN			0.8	V
$V_{out(1)}$	Logical 1 output voltage	59	V_{CC} = MIN, I_{load} = −500 μA	2.4	3.2		V
$V_{out(0)}$	Logical 0 output voltage	60	V_{CC} = MIN, I_{sink} = 20 mA		0.25	0.4	V
$I_{in(0)}$	Logical 0 level input current at J1, J2, J3, K1, K2, K3, preset, or clear	61	V_{CC} = MAX, V_{in} = 0.4 V		−1	−2	mA
$I_{in(0)}$	Logical 0 level input current clock	61	V_{CC} = MAX, V_{in} = 0.4 V		−3	−4.8	mA
$I_{in(1)}$	Logical 1 level input current at J1, J2, J3, K1, K2, or K3	62	V_{CC} = MAX, V_{in} = 2.4 V			50	μA
			V_{CC} = MAX, V_{in} = 5.5 V			1	mA
$I_{in(1)}$	Logical 1 level input current at clock	71	V_{CC} = MAX, V_{in} = 2.4 V			100	μA
		62	V_{CC} = MAX, V_{in} = 2.4 V	0		−1	mA
			V_{CC} = MAX, V_{in} = 5.5 V			1	mA
$I_{in(1)}$	Logical 1 level input current at preset or clear	62	V_{CC} = MAX, V_{in} = 2.4 V			100	μA
			V_{CC} = MAX, V_{in} = 5.5 V			1	mA
I_{OS}	Short-circuit output current‡	63	V_{CC} = MAX, V_{in} = 0	−40		−100	mA
I_{CC}	Supply current	62	V_{CC} = MAX		20	38	mA

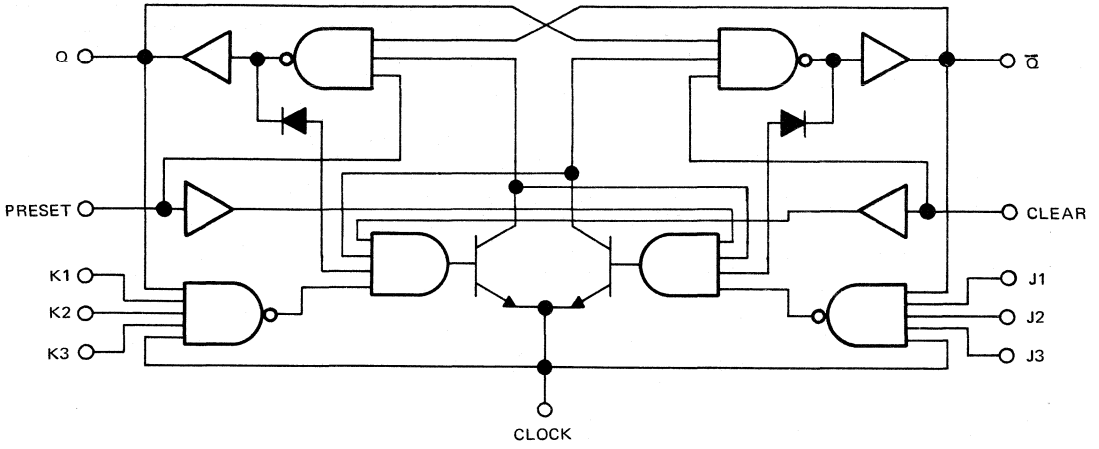
† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
‡ Not more than one output should be shorted at a time, and duration of short-circuit test should not exceed 1 second.
§ All typical values are at V_{CC} = 5 V, T_A = 25°C.

switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10

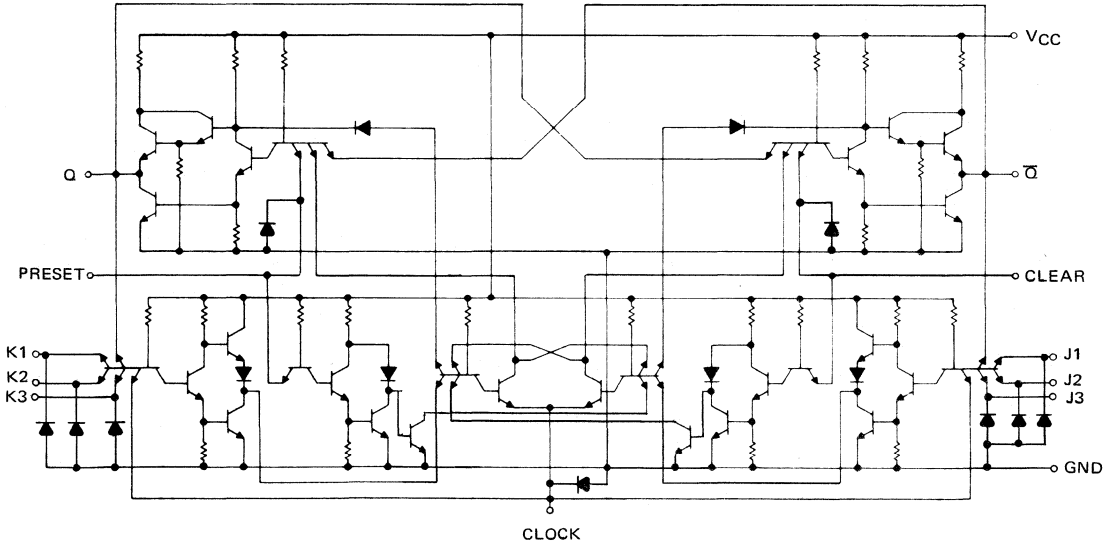
PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{clock}	Maximum input clock frequency	77	C_L = 25 pF, R_L = 280 Ω	40	50		MHz
t_{pd1}	Propagation delay time to logical 1 level from preset to output	78	C_L = 25 pF, R_L = 280 Ω		8	12	ns
t_{pd0}	Propagation delay time to logical 0 level from clear or preset to output (clock low)	78	C_L = 25 pF, R_L = 280 Ω		23	35	ns
t_{pd0}	Propagation delay time to logical 0 level from clear or preset to output (clock high)	78	C_L = 25 pF, R_L = 280 Ω		15	20	ns
t_{pd1}	Propagation delay time to logical 1 level from clock to output	77	C_L = 25 pF, R_L = 280 Ω		10	15	ns
t_{pd0}	Propagation delay time to logical 0 level from clock to output	77	C_L = 25 pF, R_L = 280 Ω		16	20	ns

–SEE ORDERING INSTRUCTIONS PAGE 1-1–

functional block diagram



schematic



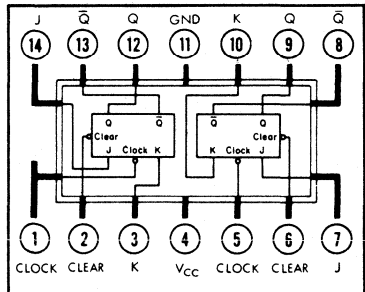
CIRCUIT TYPES SN54H103, SN74H103
DUAL J-K EDGE-TRIGGERED FLIP-FLOPS

logic

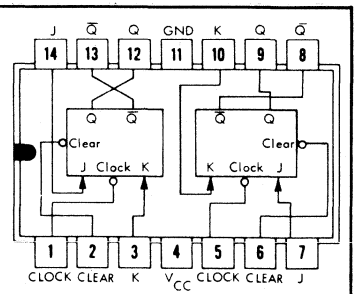
TRUTH TABLE		
t_n		t_{n+1}
J	K	Q
0	0	Q_n
0	1	0
1	0	1
1	1	$\bar{Q}_n$

NOTES: 1. t_n = Bit time before clock pulse
2. t_{n+1} = Bit time after clock pulse

S
FLAT PACKAGE (TOP VIEW)



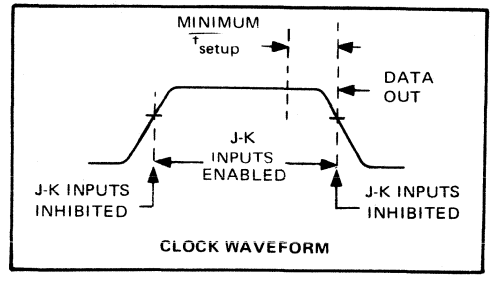
J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



positive logic: Low input to clear sets Q to logical 0
Clear is independent of clock

description

These dual monolithic J-K flip-flops are negative-edge-triggered. They feature individual J, K, clock, and asynchronous clear inputs to each flip-flop. When the clock goes high, the inputs are enabled and data will be accepted. Logical state of J and K inputs may be allowed to change when the clock pulse is in a high state and bistable will perform according to the truth table as long as minimum set-up times are observed. Input data is transferred to the outputs on the negative edge of the clock pulse.



recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply Voltage V_{CC}: SN54H103 Circuits	4.5	5	5.5	V
SN74H103 Circuits	4.75	5	5.25	V
Operating Free-Air Temperature Range, T_A: SN54H103 Circuits	−55	25	125	°C
SN74H103 Circuits	0	25	70	°C
Normalized Fan-Out From Each Output, N			10	
Width of Clock Pulse, $t_{p(clock)}$ (See Figure 77)	.10			ns
Width of Clear Pulse, $t_{p(clear)}$ (See Figure 78)	16			ns
Input Setup Time, t_{setup} (See Figure 79): Logical 1	10			ns
Logical 0	13			ns
Input Hold Time, t_{hold}	0			ns
Clock Pulse Transition Time, t_0 (See Figure 77)			150	ns

—SEE ORDERING INSTRUCTIONS PAGE 1-1—

electrical characteristics (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS†	MIN	TYP§	MAX	UNIT
$V_{in(1)}$	Input voltage required to ensure logical 1 at any input terminal	64 and 65	V_{CC} = MIN	2			V
$V_{in(0)}$	Input voltage required to ensure logical 0 at any input terminal	64 and 65	V_{CC} = MIN			0.8	V
$V_{out(1)}$	Logical 1 output voltage	64	V_{CC} = MIN, I_{load} = −500 μA	2.4	3.2		V
$V_{out(0)}$	Logical 0 output voltage	65	V_{CC} = MIN, I_{sink} = 20 mA		0.25	0.4	V
$I_{in(0)}$	Logical 0 level input current at J, K, or clear	66	V_{CC} = MAX, V_{in} = 0.4 V		−1	−2	mA
$I_{in(0)}$	Logical 0 level input current at clock	66	V_{CC} = MAX, V_{in} = 0.4 V		−3	−4.8	mA
$I_{in(1)}$	Logical 1 level input current at J or K	67	V_{CC} = MAX, V_{in} = 2.4 V			50	μA
			V_{CC} = MAX, V_{in} = 5.5 V			1	mA
$I_{in(1)}$	Logical 1 level input current at clock	72	V_{CC} = MAX, V_{in} = 2.4 V			100	μA
		67	V_{CC} = MAX, V_{in} = 2.4 V	0		−1	mA
			V_{CC} = MAX, V_{in} = 5.5 V			1	mA
$I_{in(1)}$	Logical 1 level input current at clear	67	V_{CC} = MAX, V_{in} = 2.4 V			100	μA
			V_{CC} = MAX, V_{in} = 5.5 V			1	mA
I_{OS}	Short-circuit output current‡	68	V_{CC} = MAX, V_{in} = 0	−40		−100	mA
I_{CC}	Supply current	67	V_{CC} = MAX		40	76	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

‡Not more than one output should be shorted at a time, and duration of short-circuit test should not exceed 1 second.

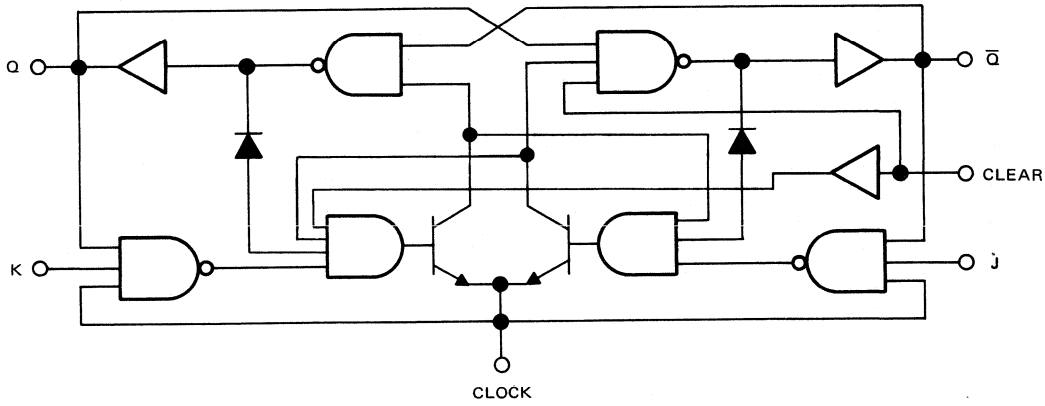
§ All typical values are at V_{CC} = 5 V, T_A = 25°C.

switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10

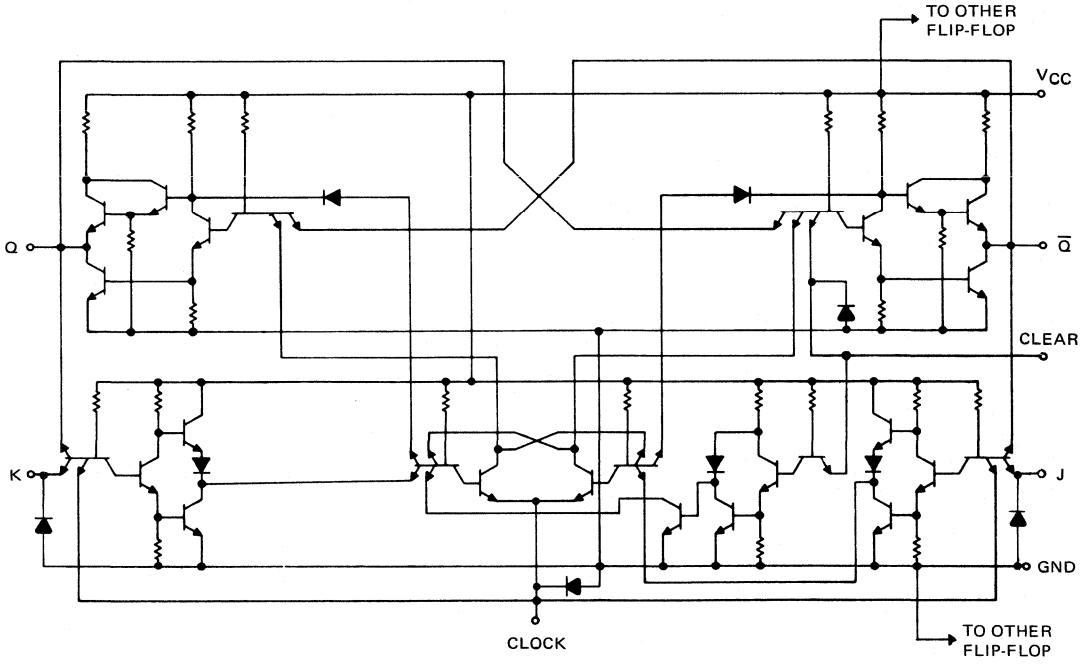
PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{clock}	Maximum input clock frequency	77	C_L = 25 pF, R_L = 280 Ω	40	50		MHz
t_{pd1}	Propagation delay time to logical 1 level from clear to output	78	C_L = 25 pF, R_L = 280 Ω		8	12	ns
t_{pd0}	Propagation delay time to logical 0 level from clear to output (Clock low)	78	C_L = 25 pF, R_L = 280 Ω		23	35	ns
t_{pd0}	Propagation delay time to logical 0 level from clear to output (clock high)	78	C_L = 25 pF, R_L = 280 Ω		15	20	ns
t_{pd1}	Propagation delay time to locical 1 level from clock to output	77	C_L = 25 pF, R_L = 280 Ω		10	15	ns
t_{pd0}	Propagation delay time to locical 0 level from clock to output	77	C_L = 25 pF, R_L = 280 Ω		16	20	ns

—SEE ORDERING INSTRUCTIONS PAGE 1-1—

functional block diagram (each flip-flop)



schematic (each flip-flop)

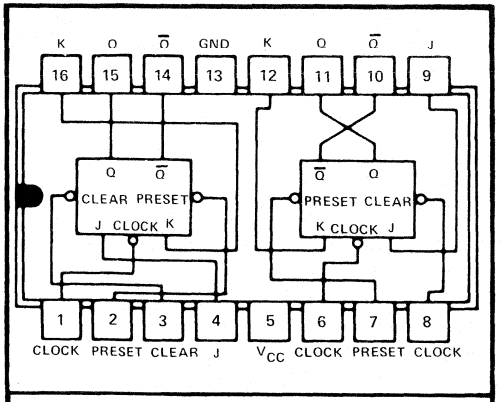


logic

TRUTH TABLE		
t_n		t_{n+1}
J	K	Q
0	0	Q_n
0	1	0
1	0	1
1	1	$\bar{Q}_n$

NOTES: 1. t_n = Bit time before clock pulse
2. t_{n+1} = Bit time after clock pulse

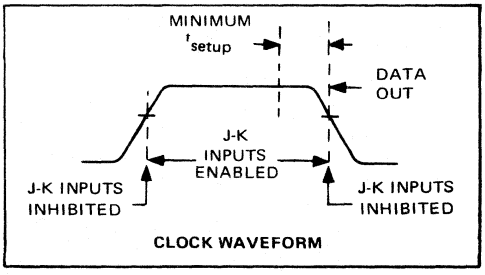
J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



positive logic:
Low input to preset sets Q to logical 1
Low input to clear sets Q to logical 0
Clear and preset are independent of clock

description

These dual monolithic J-K flip-flops are negative-edge-triggered. They feature individual J, K, clock, and asynchronous preset and clear inputs to each flip-flop. When the clock goes high, the inputs are enabled and data will be accepted. Logical state of J and K inputs may be allowed to change when the clock pulse is in a high state and bistable will perform according to the truth table as long as minimum set-up times are observed. Input data is transferred to the outputs on the negative edge of the clock pulse.



CLOCK WAVEFORM

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply Voltage V_{CC}: SN54H106 Circuits	4.5	5	5.5	V
SN74H106 Circuits	4.75	5	5.25	V
Operating Free-Air Temperature Range, T_A: SN54H106 Circuits	−55	25	125	°C
SN74H106 Circuits	0	25	70	°C
Normalized Fan-Out From Each Output, N			10	
Width of Clock Pulse, $t_{p(clock)}$ (See Figure 77)	10			ns
Width of Preset Pulse, $t_{p(preset)}$ (See Figure 78)	16			ns
Width of Clear Pulse, $t_{p(clear)}$ (See Figure 78)	16			ns
Input Setup Time, t_{setup} (See Above): Logical 1	10			ns
Logical 0	13			ns
Input Hold Time, t_{hold}	0			ns
Clock Pulse Transition Time, t_0 (See Figure 77)			150	ns

—SEE ORDERING INSTRUCTIONS PAGE 1-1—

electrical characteristics (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS†	MIN	TYP§	MAX	UNIT
$V_{in(1)}$	Input voltage required to ensure logical 1 at any input terminal	64 and 65	V_{CC} = MIN	2			V
$V_{in(0)}$	Input voltage required to ensure logical 0 at any input terminal	64 and 65	V_{CC} = MIN			0.8	V
$V_{out(1)}$	Logical 1 output voltage	64	V_{CC} = MIN, I_{load} = −500 μA	2.4	3.2		V
$V_{out(0)}$	Logical 0 output voltage	65	V_{CC} = MIN, I_{sink} = 20 mA		0.25	0.4	V
$I_{in(0)}$	Logical 0 level input current at J, K, preset, or clear	66	V_{CC} = MAX, V_{in} = 0.4 V		−1	−2	mA
$I_{in(0)}$	Logical 0 level input current at clock	66	V_{CC} = MAX, V_{in} = 0.4 V		−3	−4.8	mA
$I_{in(1)}$	Logical 1 level input current at J or K	67	V_{CC} = MAX, V_{in} = 2.4 V			50	μA
			V_{CC} = MAX, V_{in} = 5.5 V			1	mA
$I_{in(1)}$	Logical 1 level input current at preset or clear	67	V_{CC} = MAX, V_{in} = 2.4 V			100	μA
			V_{CC} = MAX, V_{in} = 5.5 V			1	mA
$I_{in(1)}$	Logical 1 level input current at clock	73	V_{CC} = MAX, V_{in} = 2.4 V			100	μA
		67	V_{CC} = MAX, V_{in} = 2.4 V	0		−1	mA
			V_{CC} = MAX, V_{in} = 5.5 V			1	mA
I_{OS}	Short-circuit output current‡	69	V_{CC} = MAX, V_{in} = 0	−40		−100	mA
I_{CC}	Supply current	67	V_{CC} = MAX		40	76	mA

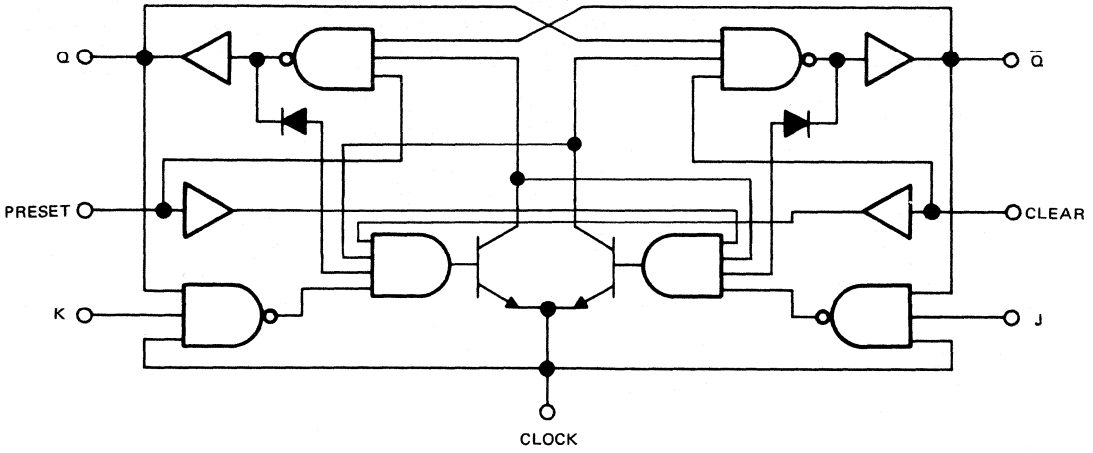
† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
‡ Not more than one output should be shorted at a time, and duration of short-circuit test should not exceed 1 second.
§ All typical values are at V_{CC} = 5 V, T_A = 25°C.

switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10

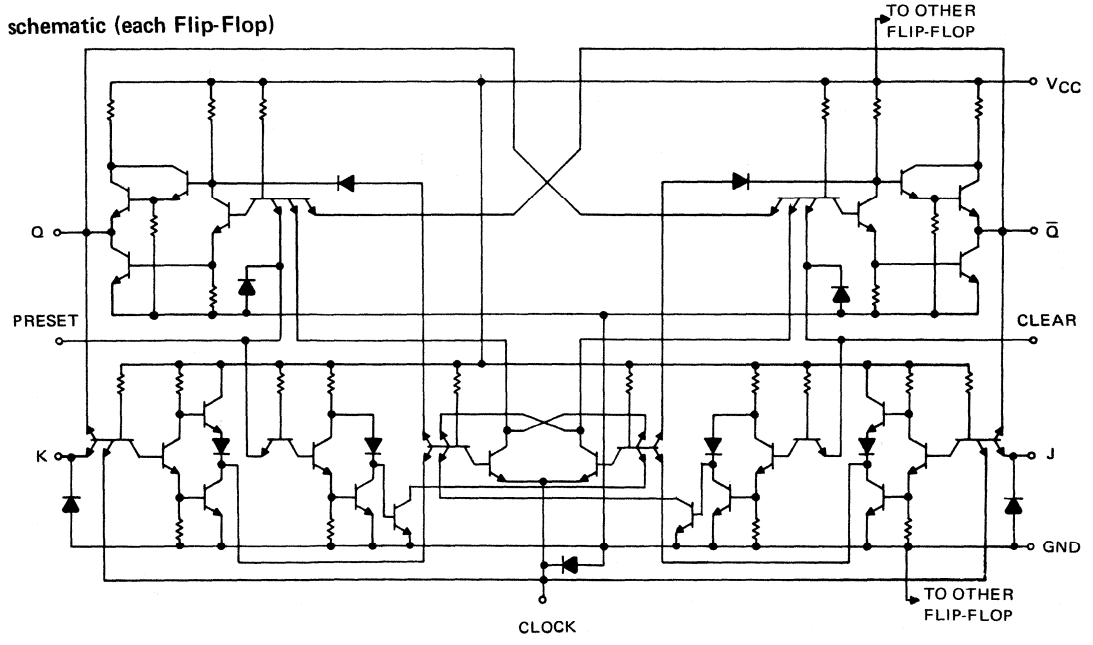
PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{clock}	Maximum input clock frequency	77	C_L = 25 pF, R_L = 280 Ω	40	50		MHz
t_{pd1}	Propagation delay time to logical 1 level from preset or clear to output	78	C_L = 25 pF, R_L = 280 Ω		8	12	ns
t_{pd0}	Propagation delay time to logical 0 level from preset or clear to output (clock low)	78	C_L = 25 pF, R_L = 280 Ω		23	35	ns
t_{pd0}	Propagation delay time to logical 0 level from preset or clear to output (clock high)	78	C_L = 25 pF, R_L = 280 Ω		15	20	ns
t_{pd1}	Propagation delay time to logical 1 level from clock to output	77	C_L = 25 pF, R_L = 280 Ω		10	15	ns
t_{pd0}	Propagation delay time to logical 0 level from clock to output	77	C_L = 25 pF, R_L = 280 Ω		16	20	ns

—SEE ORDERING INSTRUCTIONS PAGE 1-1—

functional block diagram (each Flip-Flop)



schematic (each Flip-Flop)



CIRCUIT TYPES SN54H108, SN74H108
DUAL J-K EDGE-TRIGGERED FLIP-FLOPS

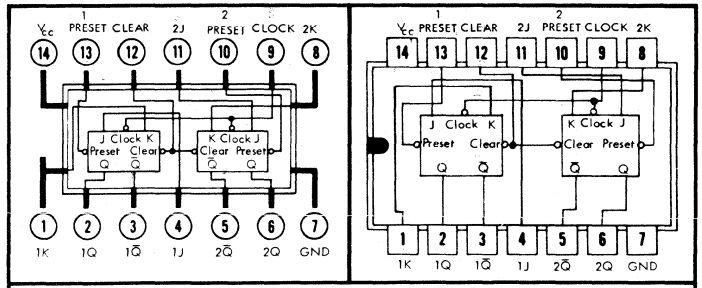
logic

TRUTH TABLE		
t_n		t_{n+1}
J	K	Q
0	0	Q_n
0	1	0
1	0	1
1	1	$\bar{Q}_n$

NOTES: 1. t_n = Bit time before clock pulse
2. t_{n+1} = Bit time after clock pulse

S
FLAT PACKAGE (TOP VIEW)

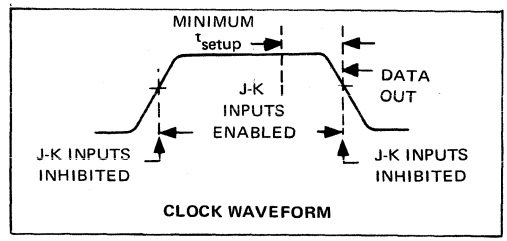
J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



positive logic: Low input to preset sets Q to logical 1
Low input to clear sets Q to logical 0
Preset and clear are independent of clock

description

These dual monolithic J-K flip-flops are negative-edge-triggered. They feature individual J, K, and asynchronous preset inputs to each flip-flop as well as common clock and asynchronous clear inputs. When the clock goes high, the inputs are enabled and data will be accepted. Logical state of J and K inputs may be allowed to change when the clock pulse is in a high state and bistable will perform according to the truth table as long as minimum set-up times are observed. Input data is transferred to the outputs on the negative edge of the clock pulse.



CLOCK WAVEFORM

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply Voltage V_{CC}: SN54H108 Circuits	4.5	5	5.5	V
SN74H108 Circuits	4.75	5	5.25	V
Operating Free-Air Temperature Range, T_A: SN54H108 Circuits	−55	25	125	°C
SN74H108 Circuits	0	25	70	°C
Normalized Fan-Out From Each Output, N			10	
Width of Clock Pulse, $t_{p(clock)}$ (See Figure 77)	10			ns
Width of Preset Pulse, $t_{p(preset)}$ (See Figure 78)	15			ns
Width of Clear Pulse, $t_{p(clear)}$ (See Figure 78)				ns
Input Setup Time, t_{setup} (See above): Logical 1	10			ns
Logical 0	13			ns
Input Hold Time, t_{hold}	0			ns
Clock Pulse Transition Time, t_0 (See Figure 77)			150	ns

—SEE ORDERING INSTRUCTIONS PAGE 1-1—

electrical characteristics (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS†	MIN	TYP§	MAX	UNIT
$V_{in(1)}$	Input voltage required to ensure logical 1 at any input terminal	64 and 65	V_{CC} = MIN	2			V
$V_{in(0)}$	Input voltage required to ensure logical 0 at any input terminal	64 and 65	V_{CC} = MIN			0.8	V
$V_{out(1)}$	Logical 1 output voltage	64	V_{CC} = MIN, I_{load} = −500 μA	2.4	3.2		V
$V_{out(0)}$	Logical 0 output voltage	65	V_{CC} = MIN, I_{sink} = 20 mA		0.25	0.4	V
$I_{in(0)}$	Logical 0 level input current at J, K, or preset	66	V_{CC} = MAX, V_{in} = 0.4 V		−1	−2	mA
$I_{in(0)}$	Logical 0 level input current at clock	66	V_{CC} = MAX, V_{in} = 0.4 V		−6	−9.6	mA
$I_{in(0)}$	Logical 0 level input current at clear	66	V_{CC} = MAX, V_{in} = 0.4 V		−2	−4	mA
$I_{in(1)}$	Logical 1 level input current at J or K	67	V_{CC} = MAX, V_{in} = 2.4 V			50	μA
			V_{CC} = MAX, V_{in} = 5.5 V			1	mA
$I_{in(1)}$	Logical 1 level input current at clock	73	V_{CC} = MAX, V_{in} = 2.4 V			200	μA
		67	V_{CC} = MAX, V_{in} = 2.4 V	0		−1	mA
			V_{CC} = MAX, V_{in} = 5.5 V			1	mA
$I_{in(1)}$	Logical 1 level input current at preset	67	V_{CC} = MAX, V_{in} = 2.4 V			100	μA
			V_{CC} = MAX, V_{in} = 5.5 V			1	mA
$I_{in(1)}$	Logical 1 level input current at clear	67	V_{CC} = MAX, V_{in} = 2.4 V			200	μA
			V_{CC} = MAX, V_{in} = 5.5 V			1	mA
I_{OS}	Short-circuit output current‡	69	V_{CC} = MAX, V_{in} = 0	−40		−100	mA
I_{CC}	Supply current	67	V_{CC} = MAX		40	76	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

‡ Not more than one output should be shorted at a time, and duration of short-circuit test should not exceed 1 second.

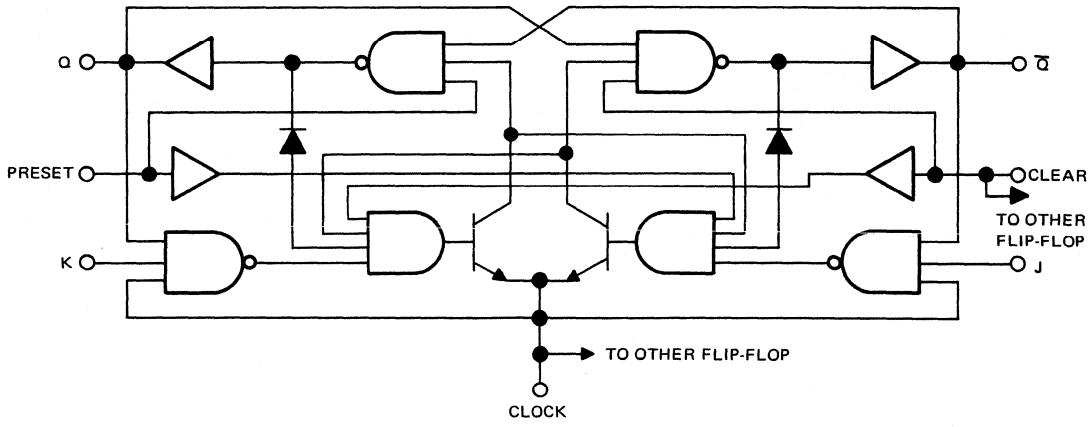
§ All typical values are at V_{CC} = 5 V, T_A = 25°C.

switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10

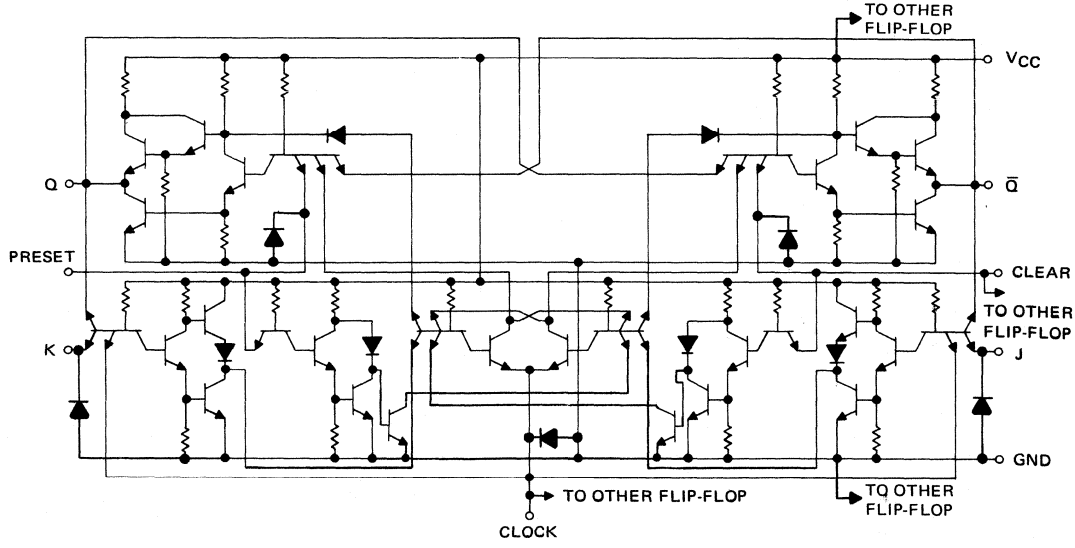
PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{clock}	Maximum input clock frequency	77	C_L = 25 pF, R_L = 280 Ω	40	50		MHz
t_{pd1}	Propagation delay time to logical 1 level from preset or clear to output	78	C_L = 25 pF, R_L = 280 Ω		8	12	ns
t_{pd0}	Propagation delay time to logical 0 level from preset or clear to output output (clock low)	78	C_L = 25 pF, R_L = 280 Ω		23	35	ns
t_{pd0}	Propagation delay time to logical 0 level from preset or clear to output output (clock high)	78	C_L = 25 pF, R_L = 280 Ω		15	20	ns
t_{pd1}	Propagation delay time to logical 1 level from clock to output	77	C_L = 25 pF, R_L = 280 Ω		10	15	ns
t_{pd0}	Propagation delay time to logical 0 level from clock to output	77	C_L = 25 pF, R_L = 280 Ω		16	20	ns

—SEE ORDERING INSTRUCTIONS PAGE 1-1—

functional block diagram (each flip-flop)



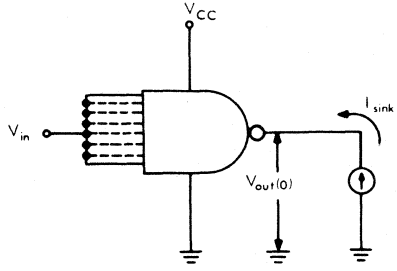
schematic (each flip-flop)



–SEE ORDERING INSTRUCTIONS PAGE 1-1–

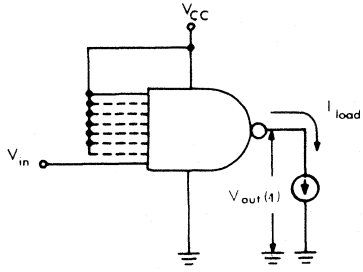
PARAMETER MEASUREMENT INFORMATION

d-c test circuits§



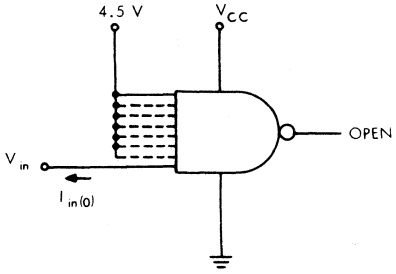
1. All inputs are tested simultaneously.

FIGURE 1



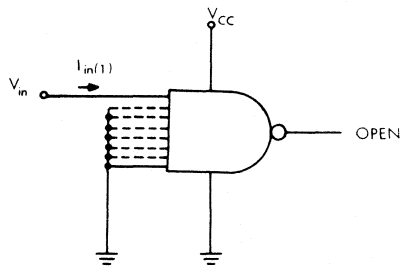
1. Each input is tested separately.

FIGURE 2



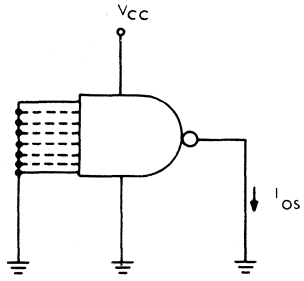
1. Each input is tested separately.

FIGURE 3



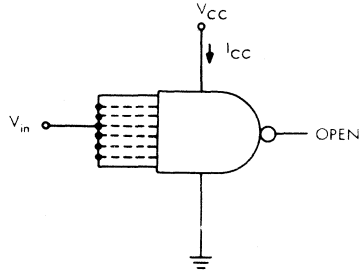
1. Each input is tested separately.

FIGURE 4



1. Each gate is tested separately.

FIGURE 5



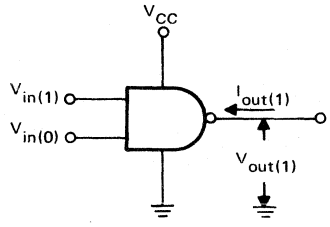
1. Logical 0 and logical 1 conditions are tested.
2. All gates are tested simultaneously. Average-per-gate value $= \frac{I_{CC}\ \text{total}}{\text{number of gates in package}}$

FIGURE 6

§Arrows indicate actual direction of current flow.

PARAMETER MEASUREMENT INFORMATION

d-c test circuits§ (continued)



1. Each input is tested separately.

FIGURE 7

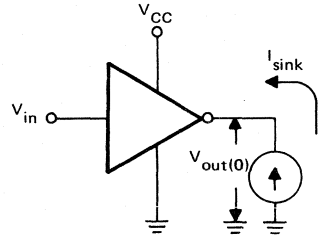
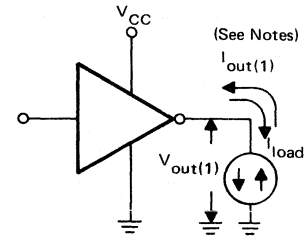


FIGURE 8



1. I_{load} is measured for Darlington outputs.
2. $I_{out(1)}$ is measured for open-collector outputs.

FIGURE 9

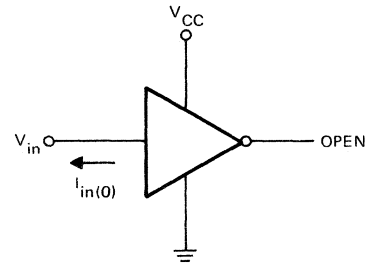


FIGURE 10

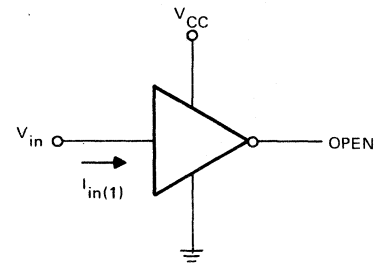
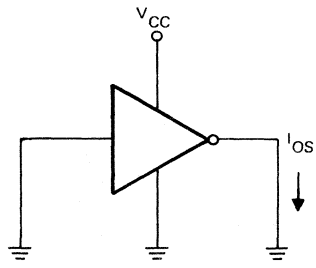
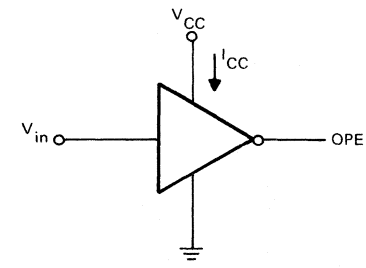


FIGURE 11



1. Each inverter is tested separately.

FIGURE 12



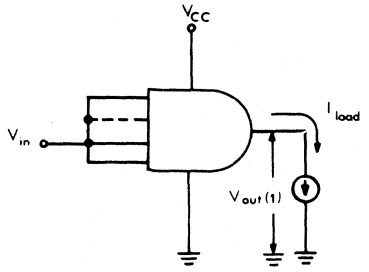
1. All inverters are tested simultaneously.

FIGURE 13

§ Arrows indicate actual direction of current flow.

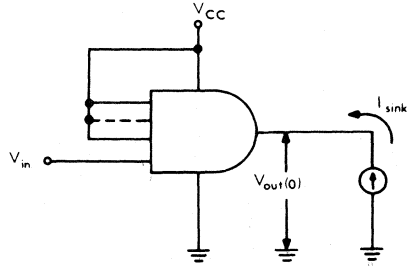
PARAMETER MEASUREMENT INFORMATION

d-c test circuits§ (continued)



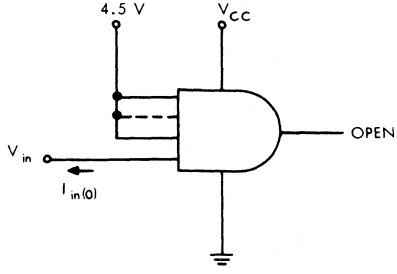
1. All inputs are tested simultaneously.

FIGURE 14



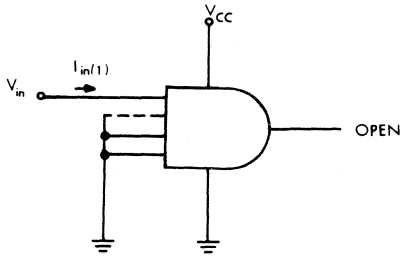
1. Each input is tested separately.

FIGURE 15



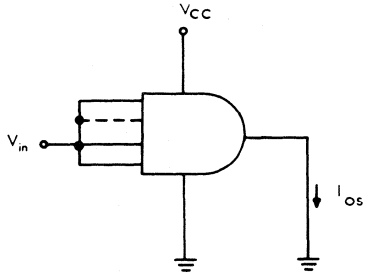
1. Each input is tested separately.

FIGURE 16



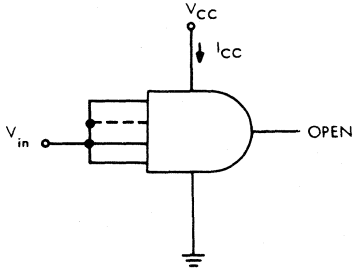
1. Each input is tested separately.

FIGURE 17



1. Each gate is tested separately.

FIGURE 18



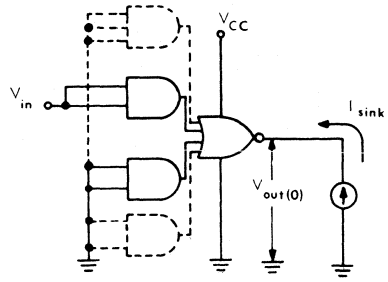
1. Logical 0 and logical 1 conditions are tested.
2. All gates are tested simultaneously.

FIGURE 19

§Arrows indicate actual direction of current flow.

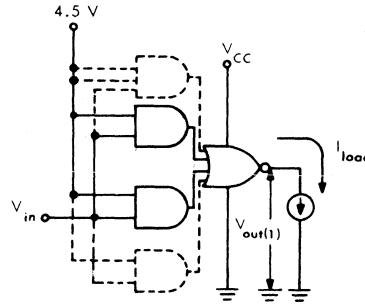
PARAMETER MEASUREMENT INFORMATION

d-c test circuits§ (continued)



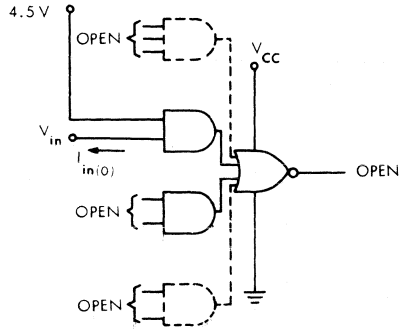
1. Each AND section is tested separately.

FIGURE 20



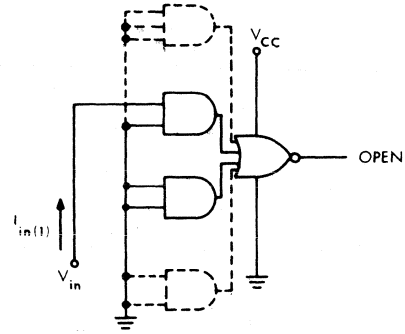
1. Each set of inputs is tested separately.

FIGURE 21



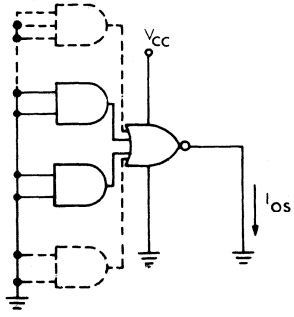
1. Each input is tested separately.

FIGURE 22



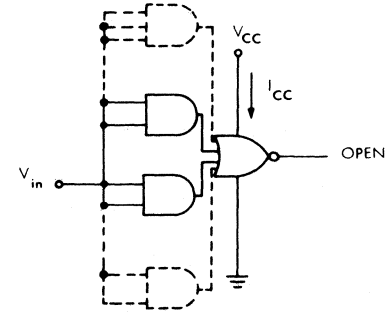
1. Each input is tested separately.

FIGURE 23



1. Each gate is tested separately.

FIGURE 24



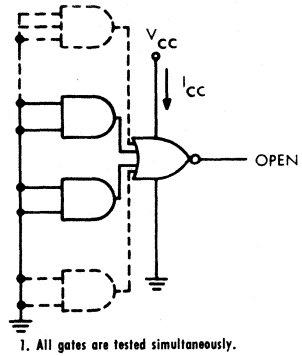
1. All gates are tested simultaneously

FIGURE 25

§Arrows indicate actual direction of current flow.

PARAMETER MEASUREMENT INFORMATION

d-c test circuits§ (continued)



1. All gates are tested simultaneously.

FIGURE 26

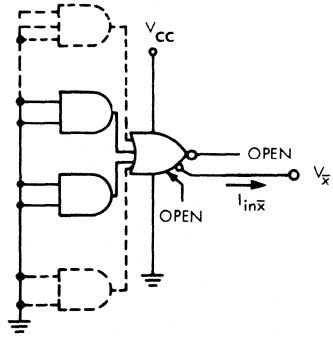


FIGURE 27

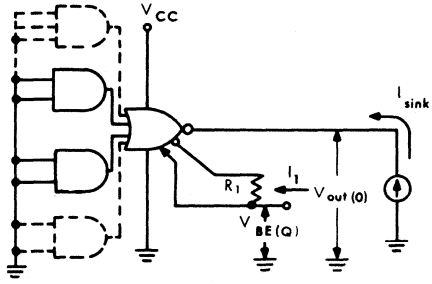


FIGURE 28

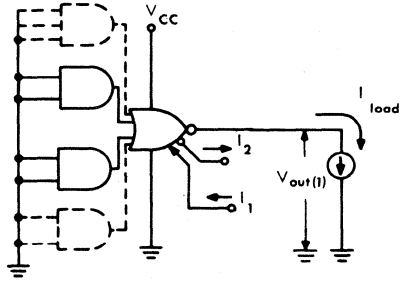
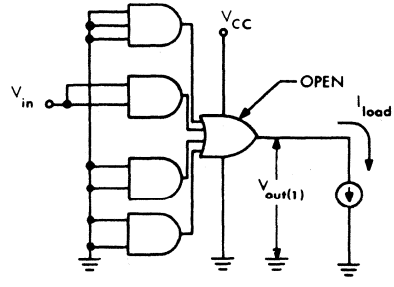
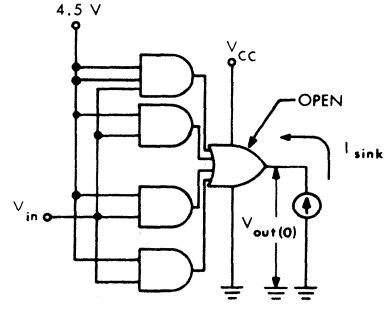


FIGURE 29



1. Each AND section is tested separately.

FIGURE 30



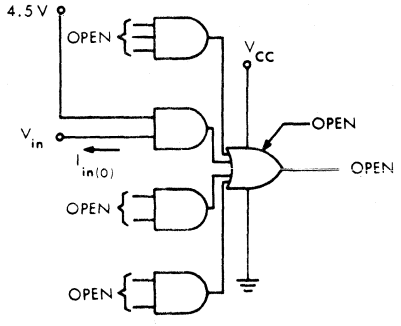
1. Each set of inputs is tested separately.

FIGURE 31

§Arrows indicate actual direction of current flow.

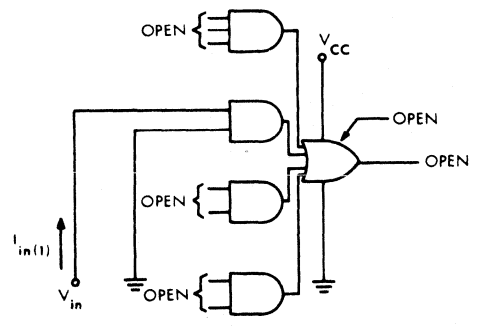
PARAMETER MEASUREMENT INFORMATION

d-c test circuits§ (continued)



1. Each input of each AND section is tested separately.

FIGURE 32



1. Each input of each AND section is tested separately.

FIGURE 33

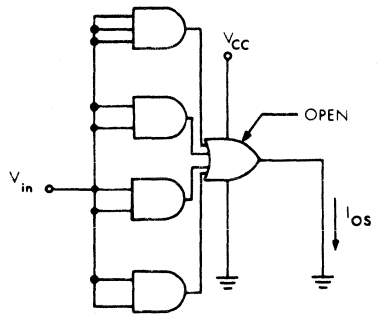
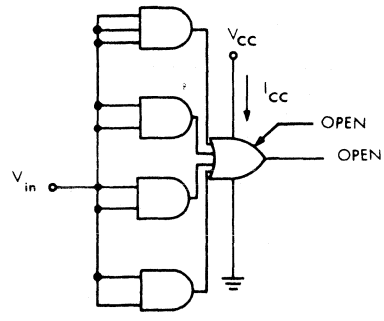


FIGURE 34



1. Logical 0 and logical 1 conditions are tested.

FIGURE 35

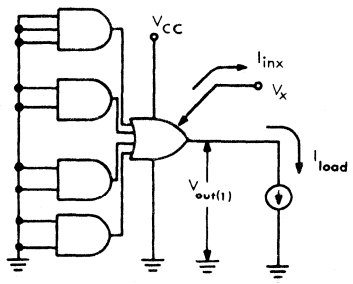


FIGURE 36

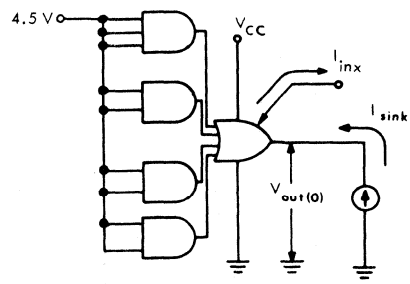
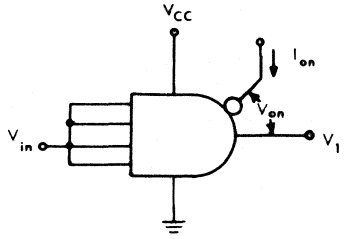


FIGURE 37

§Arrows indicate actual direction of current flow.

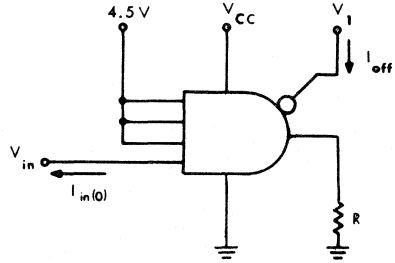
PARAMETER MEASUREMENT INFORMATION

d-c test circuits§ (continued)



1. All inputs are tested simultaneously.

FIGURE 38



1. Each input is tested separately.

FIGURE 39

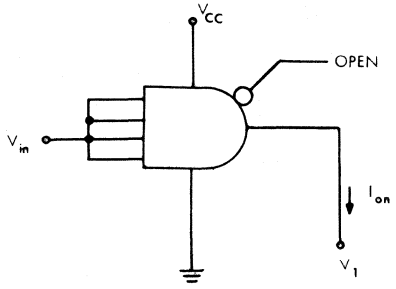
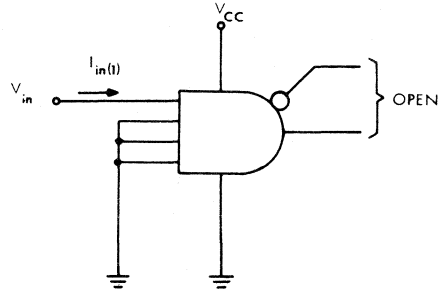
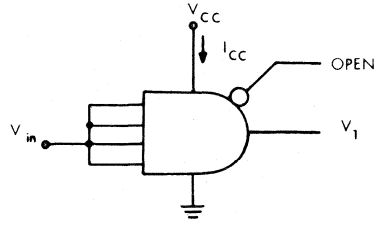


FIGURE 40



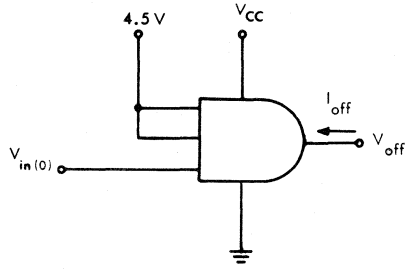
1. Each input is tested separately.

FIGURE 41



1. On and off conditions are tested separately.
2. All gates are tested simultaneously.

FIGURE 42



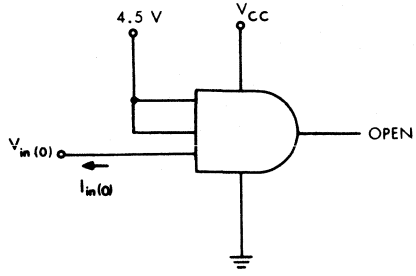
1. Each input is tested separately.

FIGURE 43

§Arrows indicate actual direction of current flow.

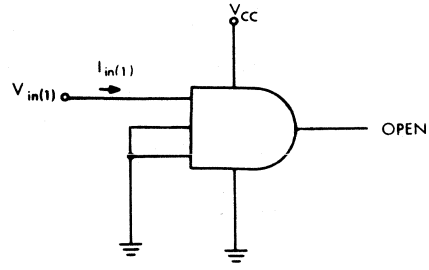
PARAMETER MEASUREMENT INFORMATION

d-c test circuits§ (continued)



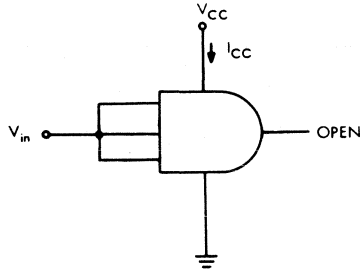
1. Each input is tested separately.

FIGURE 44



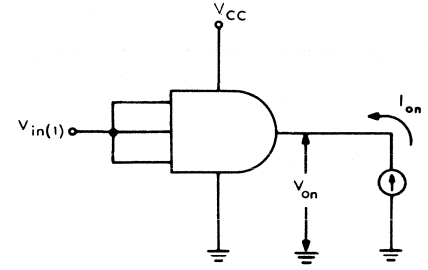
1. Each input is tested separately.

FIGURE 45



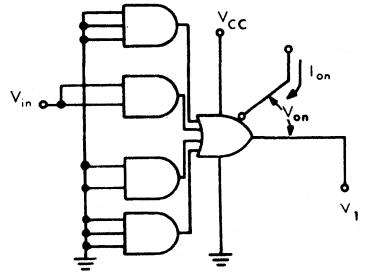
1. On and off conditions are tested separately.
2. All gates are tested simultaneously.

FIGURE 46



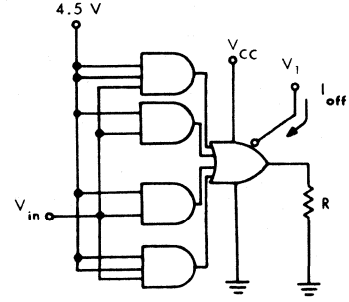
1. All inputs are tested simultaneously.

FIGURE 47



1. Each AND section is tested separately.

FIGURE 48



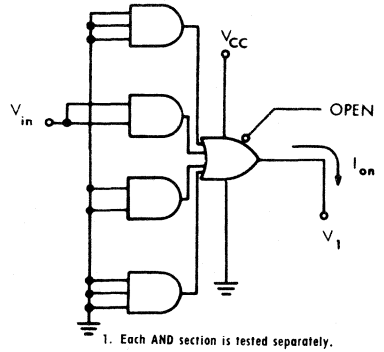
1. Each set of inputs is tested separately.

FIGURE 49

§Arrows indicate actual direction of current flow.

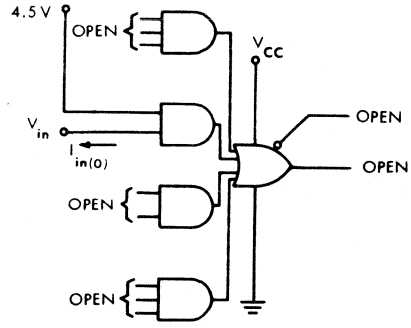
PARAMETER MEASUREMENT INFORMATION

d-c test circuits§ (continued)



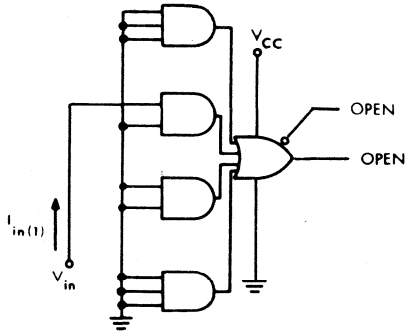
1. Each AND section is tested separately.

FIGURE 50



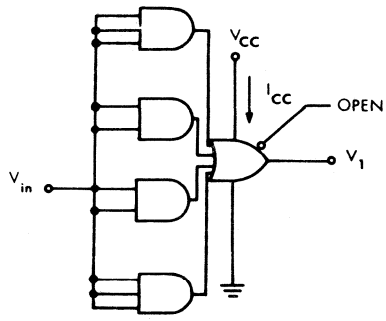
1. Each input is tested separately.

FIGURE 51



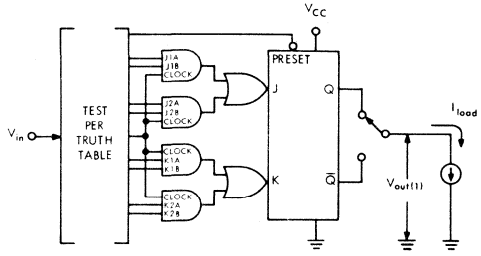
1. Each input is tested separately.

FIGURE 52



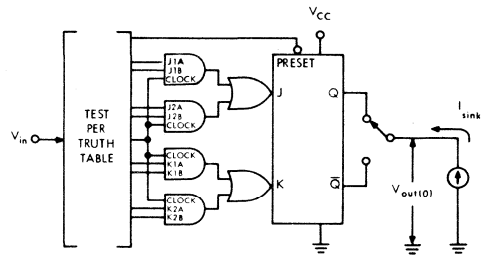
1. On and off conditions are tested separately.

FIGURE 53



1. Each output is tested separately.

FIGURE 54



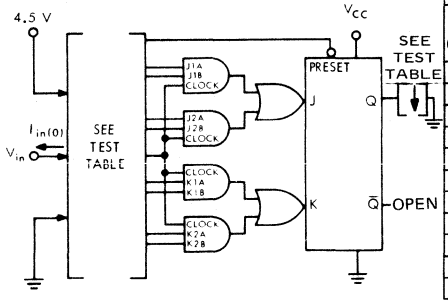
1. Each output is tested separately.

FIGURE 55

§Arrows indicate actual direction of current flow.

PARAMETER MEASUREMENT INFORMATION

d-c test circuits§ (continued)

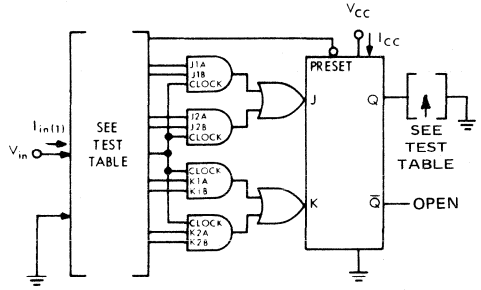


TEST TABLE†			
Apply V_{in} (Test $I_{in(0)}$)	Apply 4.5 V	Apply Momentary GND then 4.5 V	GND
Clock	J1A, J1B, J2A, J2B, K1A, K1B, K2A, and K2B	Preset	None
Clock‡	J1A, J1B, J2A, J2B, K1A, K1B, K2A, K2B,and Preset	None	Q
Preset	J1A, J1B, J2A, J2B, K1A, K1B, K2A, K2B, and Clock	None	None
J1A‡	J1B and Clock	None	Q
J1B‡	J1A and Clock	None	Q
J2A‡	J2B and Clock	None	Q
J2B‡	J2A and Clock	None	Q
K1A	K1B and Clock	Preset	None
K1B	K1A and Clock	Preset	None
K2A	K2B and Clock	Preset	None
K2B	K2A and Clock	Preset	None

†Inputs and output not specified are open.
‡Duration of this test should not exceed 1 second.

1. Each input is tested separately.

FIGURE 56

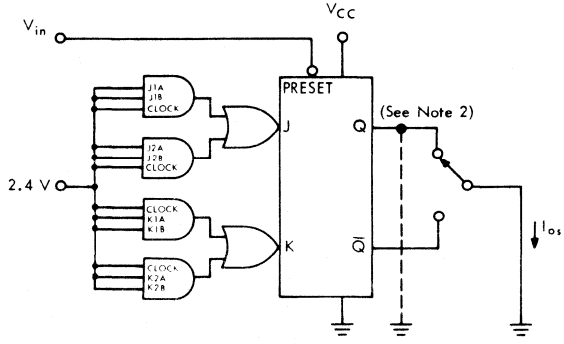


TEST TABLE†	
Apply V_{in} (Test $I_{in(1)}$)	Ground
Clock	J1A, J1B, J2A, J2B, K1A, K1B, K2A, K2B, and Preset
Clock‡¶	J1A, J1B, J2A, J2B, K1A, K1B, K2A, K2B, Preset,and Q
Preset	K1A, K1B, K2A K2B, Clock, and Q
J1A	J1B, Clock, and Preset
J1B	J1A, Clock, and Preset
J2A	J2B, Clock, and Preset
J2B	J2A, Clock, and Preset
K1A ¶	K1B, Clock, Preset, and Q
K1B ¶	K1A, Clock, Preset, and Q
K2A ¶	K2B, Clock, Preset, and Q
K2B ¶	K2A, Clock, Preset, and Q

†Inputs and outputs not specified are open.
¶Duration of this test should not exceed 1 second.
‡ SN54H71/SN74H71 only.

1. Each input is tested separately.
2. I_{CC} is measured for each of the following conditions:
   a. J1A = J1B = J2A = J2B = K1A = K1B = K2A = K2B = Clock = Preset = Gnd.
   b. J1A = J1B = J2A = J2B = Gnd, K1A = K1B = K2A = K2B = Preset = 4.5 V, and Clock = momentary 4.5 V, then Gnd.

FIGURE 57



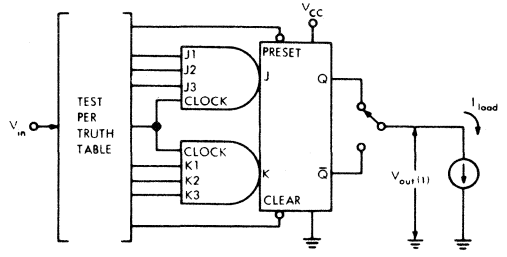
1. Each output is tested separately.
2. Test circuit shows setup for testing Q. When testing $\bar{Q}$, apply 2.4 V to Preset, ground Q, and limit duration of test to 100 ms.

FIGURE 58

§Arrows indicate actual direction of current flow.

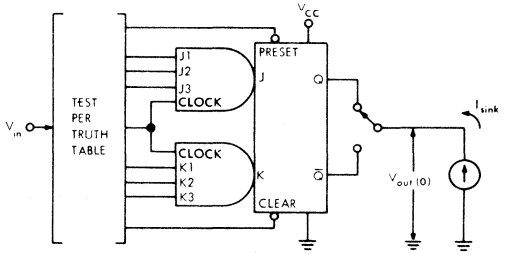
PARAMETER MEASUREMENT INFORMATION

d-c test circuits§ (continued)



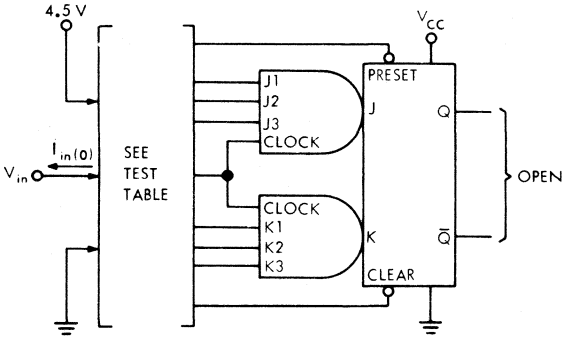
1. Each output is tested separately.

FIGURE 59



1. Each output is tested separately.

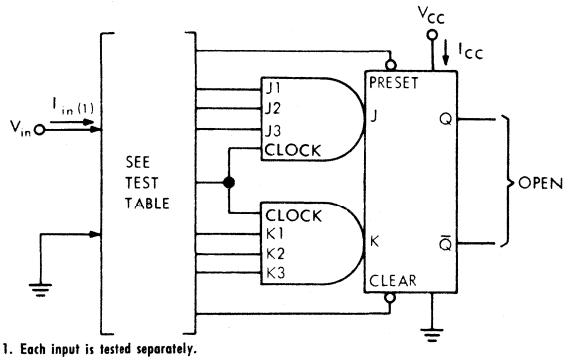
FIGURE 60



1. Each input is tested separately.

FIGURE 61

TEST TABLE		
Apply V_{in} (Test $I_{in(0)}$)	Apply Momentary GND, then 4.5 V	Apply 4.5 V
Clock	Preset	J1, J2, J3, K1, K2, and K3
Clock	Clear	J1, J2, J3, K1, K2, and K3
Preset	None	J1, J2, J3, K1, K2, and K3
Clear	None	J1, J2, J3, K1, K2, and K3
J1	Clear	Clock, J2, and J3
J2	Clear	Clock, J1, and J3
J3	Clear	Clock, J1, and J2
K1	Preset	Clock, K2, and K3
K2	Preset	Clock, K1, and K3
K3	Preset	Clock, K1, and K2



1. Each input is tested separately.
2. I_{CC} is measured for each of the following conditions:
   a. J1 = J2 = J3 = K1 = K2 = K3 = Clock = Preset = Gnd.
   b. J1 = J2 = J3 = K1 = K2 = K3 = Clock = Clear = Gnd.

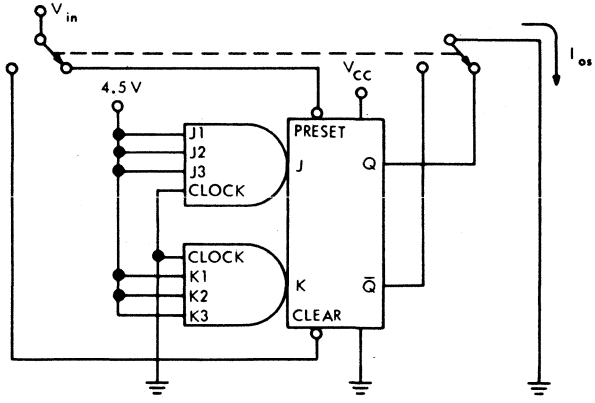
FIGURE 62

TEST TABLE	
Apply V_{in} (Test $I_{in(1)}$)	Ground
Clock	Preset, Clear, J1, J2, J3, K1, K2, and K3
Preset	Clock, K1, K2,and K3
Clear	Clock,J1, J2, and J3
J1	Clock, Clear, J2,and J3
J2	Clock, Clear, J1, and J3
J3	Clock, Clear, J1, and J2
K1	Clock, Preset, K2, and K3
K2	Clock, Preset, K1, and K3
K3	Clock, Preset, K1, and K2

§Arrows indicate actual direction of current flow.

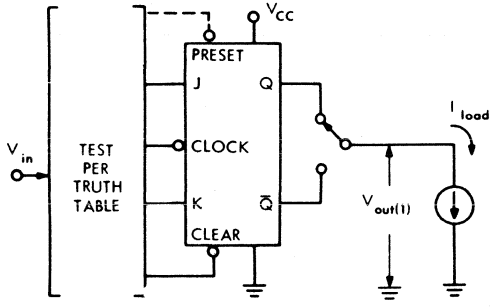
PARAMETER MEASUREMENT INFORMATION

d-c test circuits§ (continued)



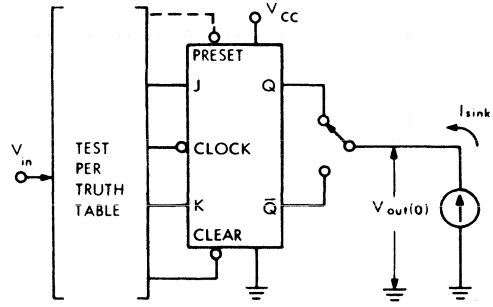
1. Each output is tested separately.

FIGURE 63



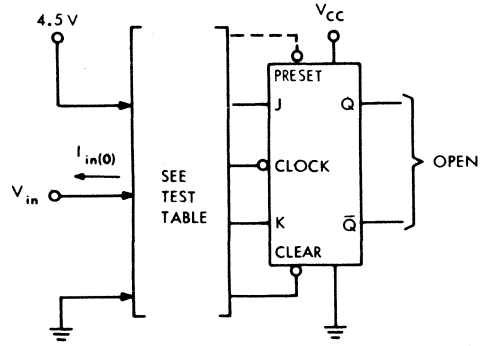
1. Each flip-flop is tested separately.
2. Each output is tested separately.
3. Preset is applicable for SN54H78/SN74H78 circuits only.

FIGURE 64



1. Each flip-flop is tested separately.
2. Each output is tested separately.
3. Preset is applicable for SN54H78/SN74H78 circuits only.

FIGURE 65



TEST TABLE		
Apply V_{in} (Test $I_{in(0)}$)	Apply Momentary GND	Apply 4.5 V
Clock	Clear (See Note 2)	J and K
Clear	None	Clock and J
Preset	None (See Note 5)	Clock and K
J	Q (See Note 3)	Clock and Clear
K	$\overline{Q}$ (See Note 3)	Clock and Clear

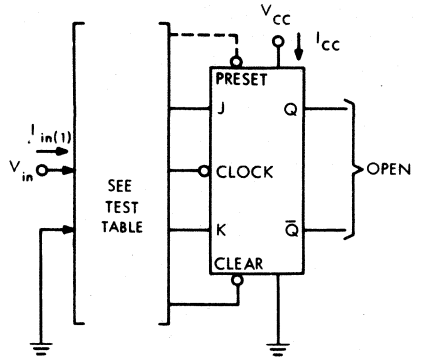
1. Each flip-flop is tested separately.
2. Apply momentary ground, then 4.5 V.
3. After application of momentary ground, Q and $\overline{Q}$ are left floating.
4. Ground all inputs of the unused flip-flop.
5. Preset is applicable for SN54H78/SN74H78 circuits only.

FIGURE 66

§Arrows indicate actual direction of current flow.

PARAMETER MEASUREMENT INFORMATION

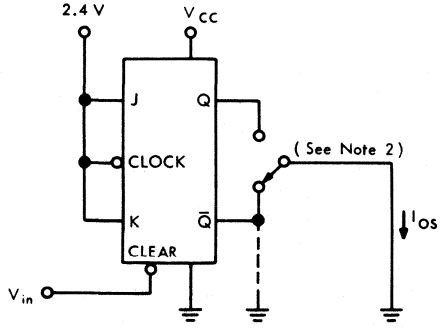
d-c test circuits§ (continued)



TEST TABLE		
Apply V_{in} (Test $I_{in(1)}$)	Ground	Apply Momentary GND, then 4.5 V
Clock	Clear, J, and K	None
Clear	Clock and J	None
Preset (See Note 1)	Clock and K	None
J (See Note 1)	Clock and Clear	Preset
K (See Note 1)	Clock and Preset	Clear

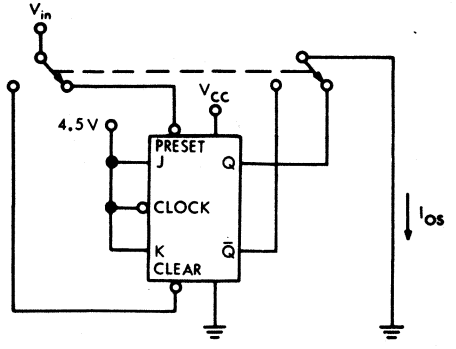
1. Preset is applicable for SN54H78/SN74H78 and SN54H108/SN74H108 circuits only.
2. I_{CC} is measured (simultaneously for both flip-flops) for the following conditions:
   a. J = K = Clock = Clear = Gnd. For SN54H78/SN74H78 and SN54H108/SN74H108: Preset = 4.5 V.
   b. For SN54H73/SN74H73 and SN54H103/SN74H103: J = Clear = 4.5 V, K = Gnd, and apply momentary 4.5 V, then Gnd, to Clock.
   For SN54H78/SN74H78 and SN54H108/SN74H108 J = K = Clock = Preset = Gnd, and Clear = 4.5 V.
3. Each flip-flop is tested separately for $I_{in(1)}$.

FIGURE 67



1. Each flip-flop is tested separately.
2. Test circuit shows setup for testing $\bar{Q}$. When testing Q, apply 2.4 V to Clear, ground $\bar{Q}$, and limit duration of test to 100 ms.

FIGURE 68



1. Each flip-flop is tested separately.

FIGURE 69

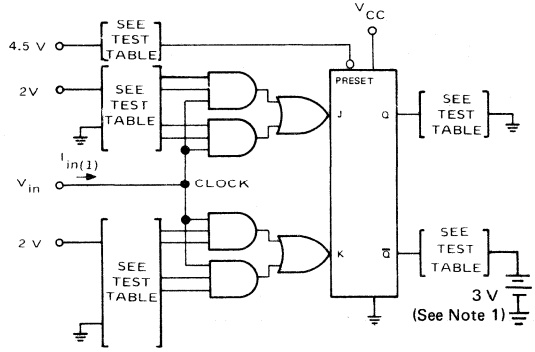
§Arrows indicate actual direction of current flow.

PARAMETER MEASUREMENT INFORMATION

d-c test circuits§ (continued)

TEST TABLE

APPLY V_{in} (TEST $I_{in(1)}$)	CONDITIONS ON OTHER INPUTS AND OUTPUTS			
	4.5 V	3 V @ 1 mA	2 V	GND
Clock	None	None	All K inputs	All J inputs and Preset
Clock	Preset	$\overline{Q}$ with I_{load} = 1 mA	All J inputs	All K inputs, and momentarily GND Q, then open



1. This supply is limited to 1 mA maximum.

FIGURE 70

TEST TABLE

Apply V_{in} (TEST $I_{in(1)}$)	CONDITIONS ON OTHER INPUTS		
	4.5 V	2 V	GND
Clock	Clear	All K inputs	All J inputs and Preset
Clock	Preset	All J inputs	All K inputs and Clear

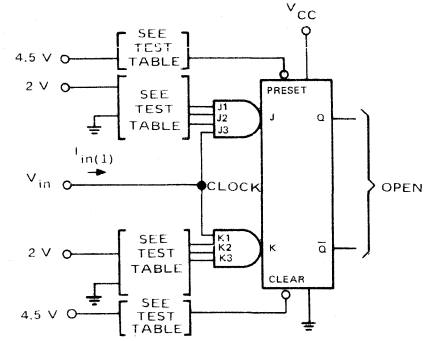
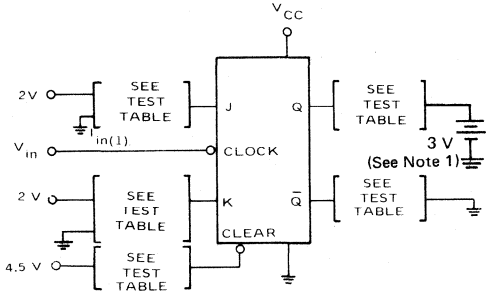


FIGURE 71

TEST TABLE

APPLY V_{in} (TEST $I_{in(1)}$)	CONDITIONS ON OTHER INPUTS AND OUTPUTS			
	4.5 V	3 V @ 1 mA	2 V	GND
Clock	None	None	J	K and Clear
Clock	Clear	$\overline{Q}$ with I_{load} = 1 mA	K	J, and momentarily GND A, then open



1. This supply is limited to 1 mA maximum.

FIGURE 72

TEST TABLE

APPLY V_{in} (TEST $I_{in(1)}$)	CONDITIONS ON OTHER INPUTS		
	4.5 V	2 V	GND
Clock	Clear	K	J and Preset
Clock	Preset	J	K and Clear

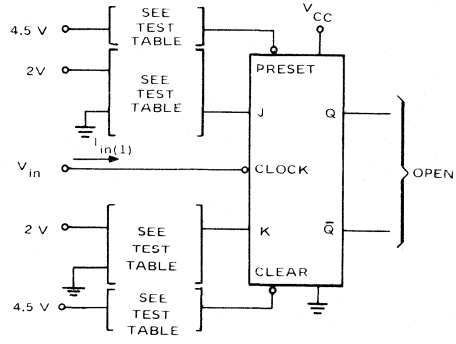
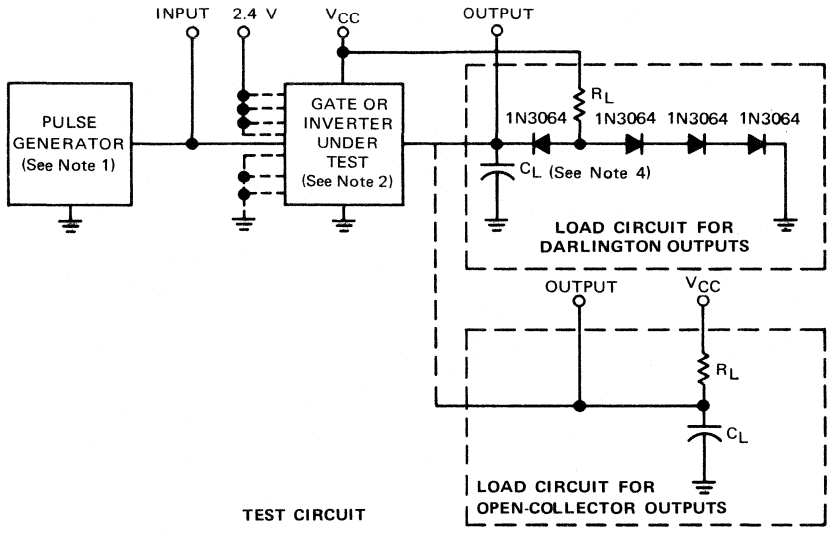


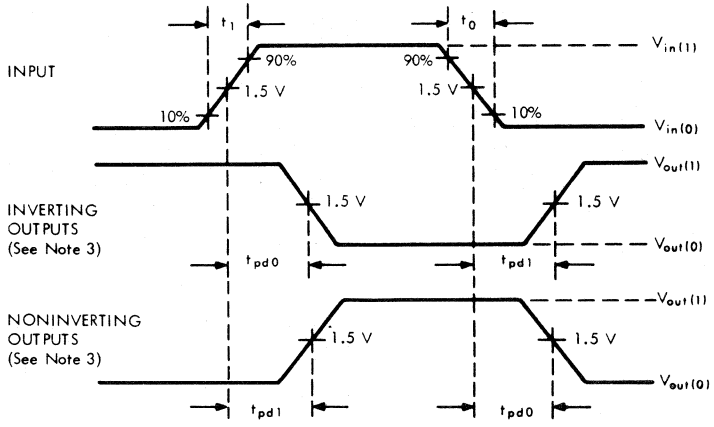
FIGURE 73

§ Arrows indicate actual direction of current flow.

PARAMETER MEASUREMENT INFORMATION

switching characteristics





VOLTAGE WAVEFORMS

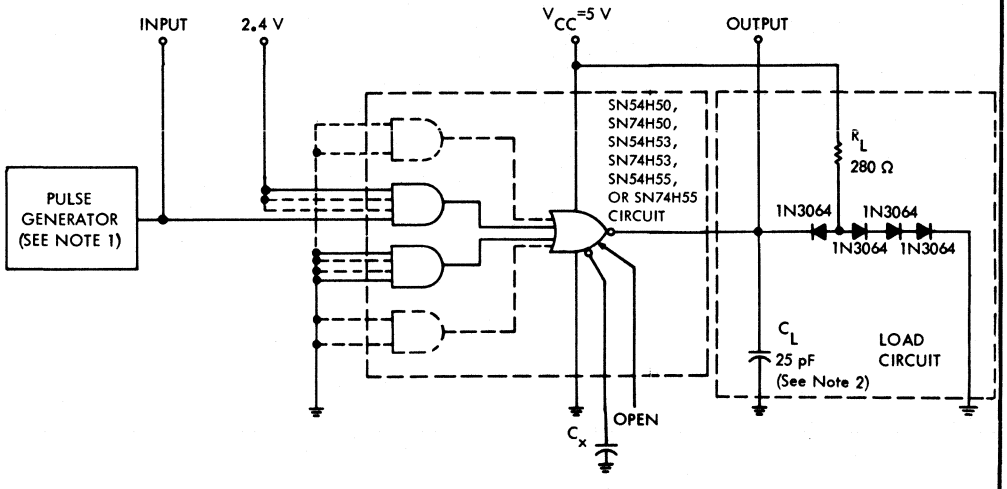
NOTES: 1. The pulse generator has the following characteristics: $V_{in(1)}$ = 3 V, $V_{in(0)}$ = 0 V, $t_1 = t_0$ = 7 ns, PRR = 1 MHz, duty cycle = 50%, and $Z_{out} \approx$ 50 Ω.

2. Input conditions are established for each gate as follows:
   a. Input pulse is applied to one input and 2.4 V is applied to all unused inputs of the SN54H00/SN74H00, SN54H01/SN74H01, SN54H04/SN74H04, SN54H05/SN74H05, SN54H10/SN74H10, SN54H11/SN74H11, SN54H20/SN74H20, SN54H21/SN74H21, SN54H22/SN74H22, SN54H30/SN74H30, or SN54H40/SN74H40 gate.
   b. Input pulse is applied to one input of one AND section, and 2.4 V is applied to all unused inputs of that AND section of the SN54H50/SN74H50, SN54H51/SN74H51, SN54H52/SN74H52, SN54H53/SN74H53, SN54H54/SN74H54, or SN54H55/SN74H55 gate. All inputs of all unused AND sections are grounded.
3. All gates are inverting except the SN54H11/SN74H11, SN54H21/SN74H21, and SN54H52/SN74H52 only.
4. C_L includes probe and jig capacitance.

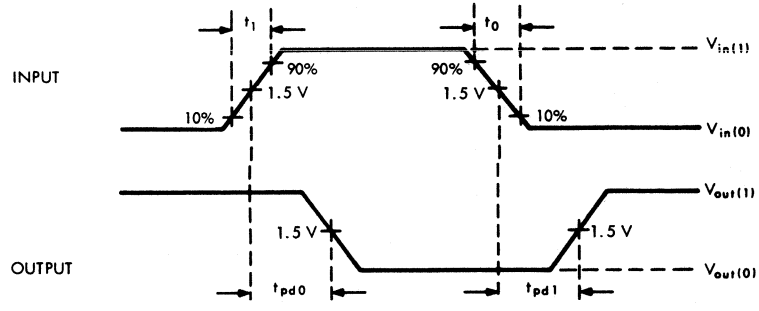
FIGURE 74 – GATE PROPAGATION DELAY TIMES

PARAMETER MEASUREMENT INFORMATION

switching characteristics (continued)



TEST CIRCUIT



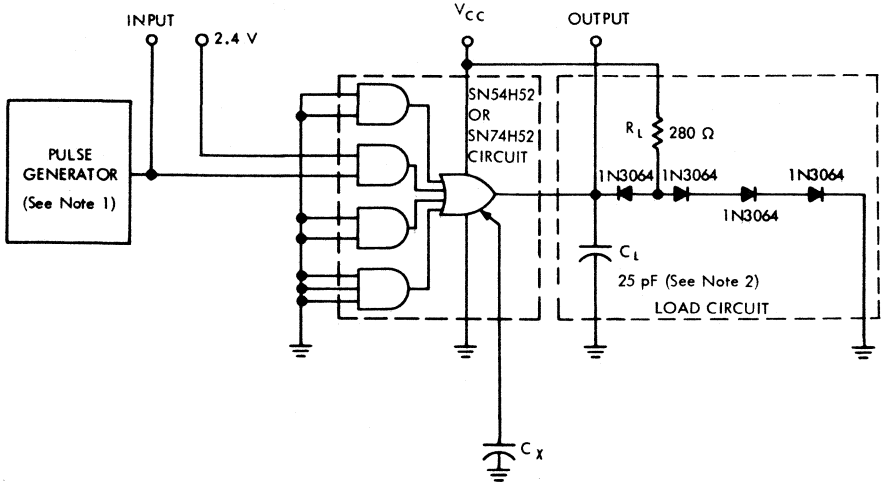
VOLTAGE WAVEFORMS

NOTES: 1. The generator has the following characteristics: $V_{in(1)} = 3$ V, $V_{in(0)} = 0$ V, $t_0 = t_1 = 7$ ns, duty cycle = 50%, PRR = 1 MHz, $Z_{out} \approx 50\ \Omega$.
2. C_L includes probe and jig capacitance.
3. C_x includes jig capacitance.

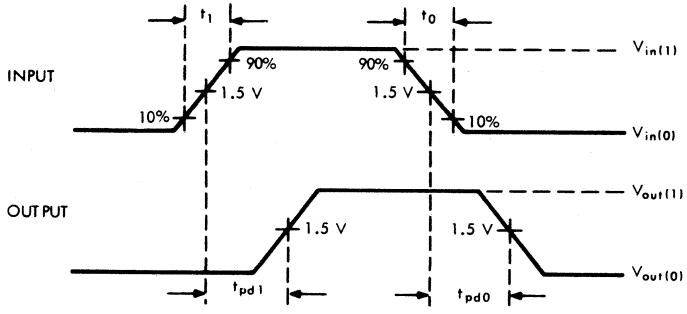
FIGURE 75 – SN54H50/SN74H50, SN54H53/SN74H53, SN54H55/SN74H55 PROPAGATION DELAY TIMES

PARAMETER MEASUREMENT INFORMATION

switching characteristics (continued)



TEST CIRCUIT



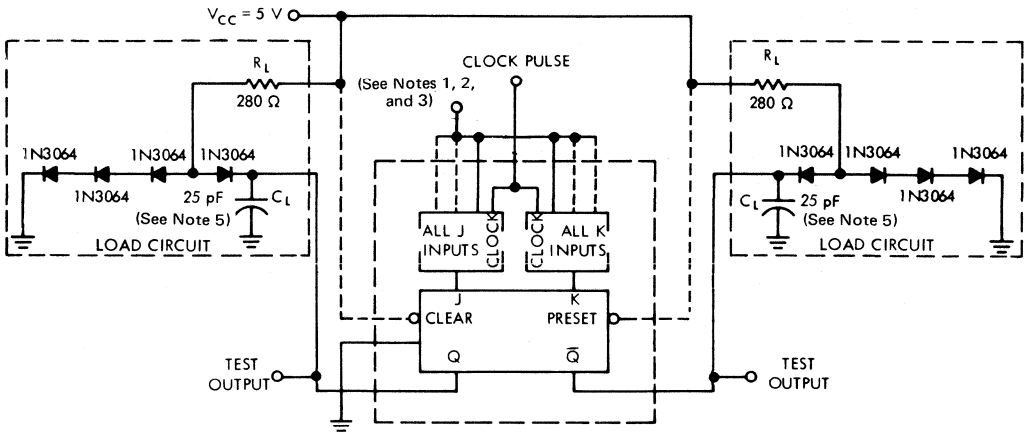
VOLTAGE WAVEFORMS

NOTES: 1. The generator has the following characteristics: $V_{in(1)} = 3$ V, $V_{in(0)} = 0$ V, $t_0 = t_1 = 7$ ns, duty cycle = 50%, PRR = 1 MHz, $Z_{out} \approx 50\ \Omega$.
2. C_L includes probe and jig capacitance.
3. C_X includes jig capacitance.

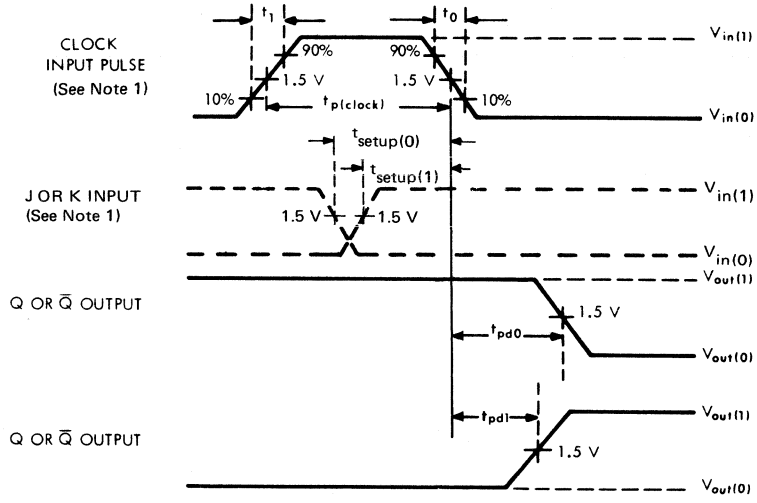
FIGURE 76 – SN54H52/SN74H52 PROPAGATION DELAY TIMES

PARAMETER MEASUREMENT INFORMATION

switching characteristics (continued)



TEST CIRCUIT



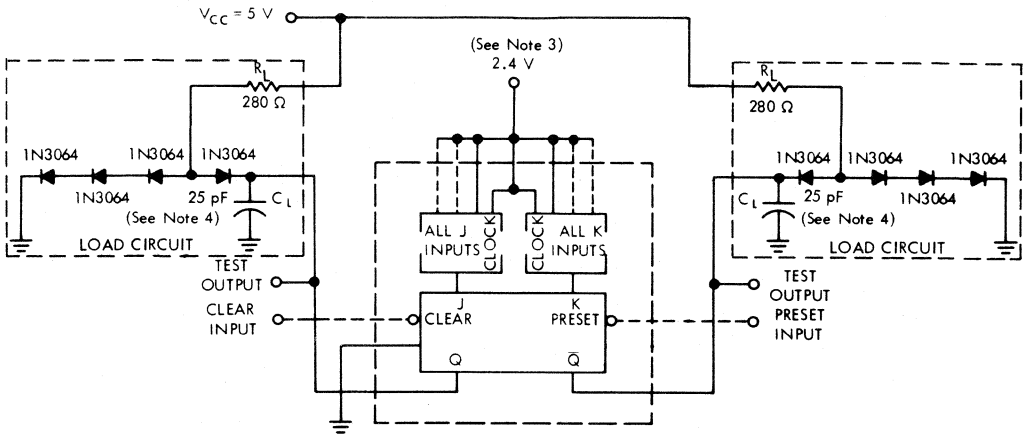
VOLTAGE WAVEFORMS

NOTES:
1. When testing t_{pd0} and t_{pd1} (all types), the clock input pulse characteristics are: $V_{in(1)}$ = 3 V, $V_{in(0)}$ = 0 V, $t_1 = t_0$ = 7ns, $t_{p(clock)}$ = 20 ns, and PRR = 1 MHz. When testing SN54H71/SN74H71, SN54H72/SN74H72, SN54H73/SN74H73, SN54H76/SN74H76, and SN54H78/SN74H78, all J and K inputs are at 2.4 V. When testing SN54H101/SN74H101, SN54H102/SN74H102, SN54H103/ SN74H103, SN54H106/SN74H106, and SN54H108/SN74H108, conditions are established to ensure that minimum setup times are verified.
2. When testing f_{clock} of SN54H71/SN74H71, SN54H72/SN74H72, SN54H73/SN74H73, SN54H76/SN74H76, and SN54H78/SN74H78, the clock input characteristics are: $V_{in(1)}$ = 3 V, $V_{in(0)}$ = 0 V, $t_1 = t_0$ = 3 ns, $t_{p(clock)}$ = 12 ns, and PRR = 25 MHz. All J and K inputs are at 2.4 V.
3. When testing f_{clock} of SN54H101/SN74H101, SN54H102/SN74H102, SN54H103/SN74H103, SN54H106/SN74H106, and SN54H108/SN74H108, the clock input characteristics are: $V_{in(1)}$ = 3 V, $V_{in(0)}$ = 0, $t_1 = t_0$ = 3 ns, $t_{p(clock)}$ = 10 ns, and PRR = 40 MHz. All J and K inputs are at 2.4 V.
4. See applicable circuit type for actual J and K input configuration and presence of preset or clear functions.
5. C_L includes probe and jig capacitance.

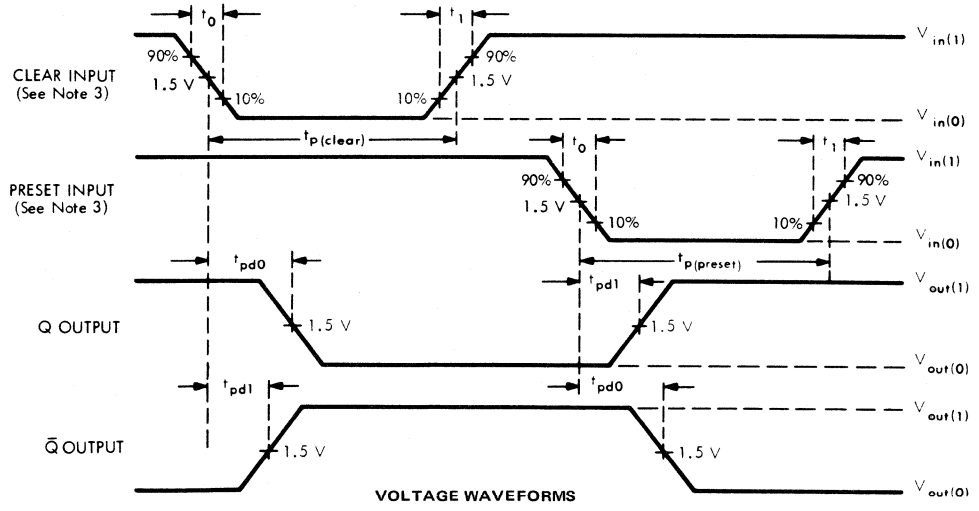
FIGURE 77—FLIP-FLOP PROPAGATION DELAY TIMES

PARAMETER MEASUREMENT INFORMATION

switching characteristics (continued)



TEST CIRCUIT



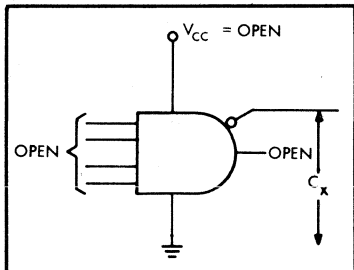
VOLTAGE WAVEFORMS

NOTES: 1. Clear or Preset inputs dominate regardless of the state of Clock or J-K inputs.
2. Clear or Preset input pulse characteristics: $V_{in(1)} = 3$ V, $V_{in(0)} = 0$ V, $t_1 = t_0 = 7$ ns, $t_{p(clear)} = t_{p(preset)} = 16$ ns, and PRR = 1 MHz.
3. See applicable circuit type for actual J and K input configuration and presence of Preset or Clear functions.
4. C_L includes probe and jig capacitance.

FIGURE 78—FLIP-FLOP PERSET/CLEAR PROPAGATION DELAY TIMES

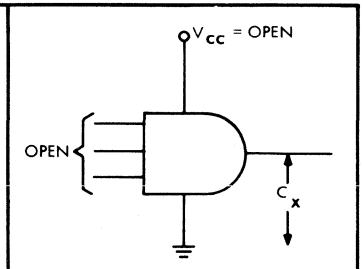
PARAMETER MEASUREMENT INFORMATION

switching time data test circuits



1. Each output is tested separately.

FIGURE 79

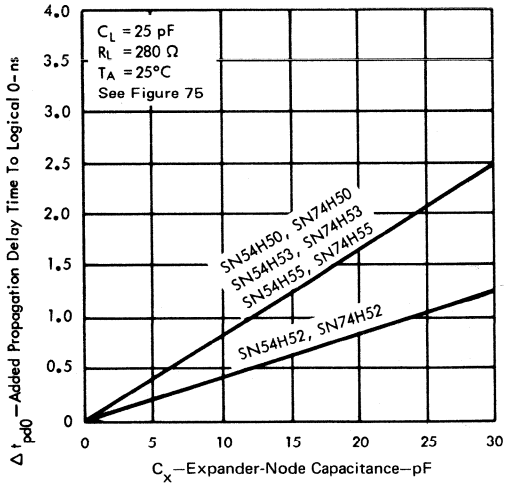


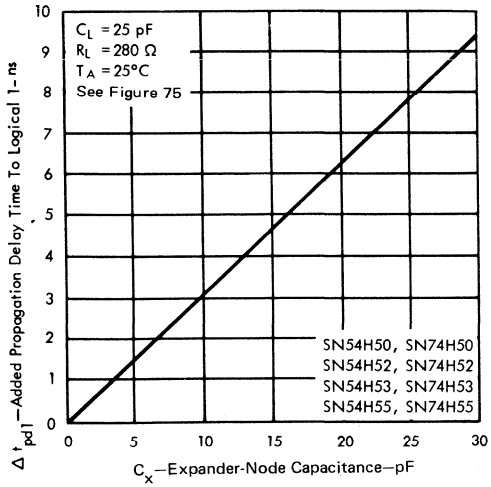
1. Each output is tested separately.

FIGURE 80

TYPICAL CHARACTERISTICS

ADDED PROPAGATION DELAY TIME vs EXPANDER-NODE CAPACITANCE





LOW-POWER TRANSISTOR-TRANSISTOR LOGIC CIRCUITS

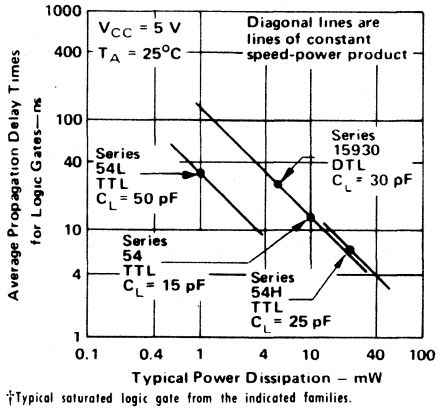
FOR AEROSPACE, MILITARY, OR INDUSTRIAL COMPUTER AND CONTROL SYSTEM APPLICATIONS

description

Series 54L/74L integrated circuits have been designed for aerospace, military, and industrial applications where high d-c noise margin, low power dissipation, improved speed-power relationships, and high reliability are important system considerations. This logic family includes small-scale integration (SSI) circuits and medium-scale integration (MSI) circuits needed to perform most functions of general-purpose digital systems. Definitive specifications for Series 54L/74L SSI circuits (gates and flip-flops) are provided in this section, and 54L/74L MSI circuits are included in Sections 7, 8, and 9.

Series 54L circuits are characterized for operation over the full military temperature range of −55°C to 125°C, and Series 74L circuits are characterized for operation over the temperature range of 0°C to 70°C.

SPEED-POWER RELATIONSHIPS OF DIGITAL IC FAMILIES†



†Typical saturated logic gate from the indicated families.

features

CHOICE OF PACKAGES

- **available in flat (T) and dual-in-line package (J or N)**
- **maximum number of circuits per package through use of 14-lead package**

OPTIMUM CIRCUIT PERFORMANCE

- **very low power dissipation—typically 1 mW per gate at 50% duty cycle**
- **relatively high speed—typically gate propagation delay time of 33 ns**
- **high d-c noise margin—typically one volt at T_A = 25°C**
- **low output impedance provides low a-c noise susceptibility**
- **waveform integrity over full range of loading and temperature conditions**
- **fan-out—10 Series 54L loads**
  - **—1 Series 54 load and 2 Series 54L loads**
  - **—1 Series 54H load**
- **a standard Series 54 output will drive 40 Series 54L loads**
- **logic levels are compatible with most bipolar saturated integrated circuits**

CONTENTS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply Voltage V_{CC} (See Note 1) . . . . . 8 V
Input Voltage V_{in} (See Notes 1 and 2) . . . . . 5.5 V
Operating Free-Air Temperature Range: Series 54L . . . . . −55°C to 125°C
Series 74L . . . . . 0°C to 70°C
Storage Temperature Range . . . . . −65°C to 150°C

NOTES: 1. Voltage values are with respect to network ground terminal.
2. Input signals must be zero or positive with respect to network ground terminal.

logic definition

Series 54L and 74L logic is defined in terms of standard POSITIVE LOGIC using the following definitions:

HIGH VOLTAGE = LOGICAL 1
LOW VOLTAGE = LOGICAL 0

unused gates

Inputs of unused gates should be connected to ground. This sets the gate output to logical 1 to ensure minimum power dissipation.

unused inputs

Unused inputs, including preset and clear, must be maintained at a positive voltage greater than 2.4 V but not to exceed the absolute maximum rating of 5.5 V.

Some possible ways of handling unused inputs are:

a. Connect unused inputs to an independent supply voltage. Preferably, this voltage should be between 2.4 V and 3.5 V.
b. Connect unused inputs, except preset or clear, to a used input of the same gate if maximum fan-out of the driving output will not be exceeded.
c. Connect unused inputs to the logical 1 output of an unused gate.
d. Connect unused inputs to V_{CC} through a 1-kΩ resistor so that if a transient which exceeds the 5.5-V maximum rating should occur, the impedance will be high enough to protect the input. One to 25 unused inputs may be connected to each 1-kΩ resistor.

input-current requirements

Input-current requirements reflect worst-case V_{CC} and temperature conditions. Each input of the multiple-emitter input transistor requires no more than a 0.18-mA flow out of the input at a logical 0 voltage level; therefore, one load (N = 1) is −0.18 mA maximum. Each input (except the clock inputs of the flip-flops) requires current into the terminal at a logical 1 voltage level. This current is 10 μA maximum for each. See fan-out capabilities (below) and typical characteristics (page 4-35) for flip-flop clock input current requirements. Currents into the input terminals are specified as positive values.

Circuit inputs requiring current drive in excess of one normalized load are indicated by shading in the electrical characteristics tables.

fan-out capacity

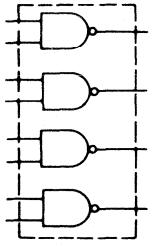
Fan-out (N) reflects the ability of an output to sink current from a number of Series 54L and 74L loads at a logical 0 voltage level and to supply current at a logical 1 voltage level. Each output is capable of sinking current or supplying current to 10 Series 54L/74L loads (N = 10), or one Series 54/74 load and two 54L/74L loads. Load currents (out of the output terminal) are specified as negative values.

A Series 54 or 74 output is capable of sinking current or supplying current to 40 Series 54L or 74L loads (N = 40). The Series 54/74 buffer gate circuit (SN5440/SN7440) is capable of driving 120 Series 54L/74L loads. The carry outputs of the Series 54/74 adders are capable of driving 20 Series 54L/74L loads and the A★ and B★ nodes of the SN5480/SN7480 may be used to drive 12 loads.

When fanning out into Series 54L/74L flip-flop clock inputs, no load current (I_{load}) is drawn at $V_{in(clock)} = 2.4$ V. Therefore, the fan-out limitation is the I_{sink} capability of the driving output. A Series 54/74 output will sink sufficient current to drive 44 clock inputs (88 loads), and the SN5440/SN7440 circuit will sink sufficient current to drive 133 clock inputs (266 loads). The Series 54L/74L output is capable of driving five 54L/74L clock inputs and one additional load. See Section 12 for more detailed explanation of drive capabilities.

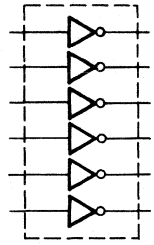
standard low-power TTL circuits

SN54L00
SN74L00
See page 4-4



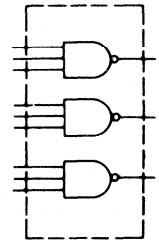
QUADRUPLE 2-INPUT
POSITIVE NAND GATES

SN54L04
SN74L04
See page 4-5



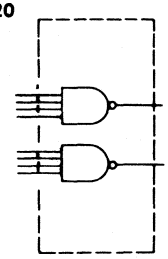
HEX INVERTERS

SN54L10
SN74L10
See page 4-6



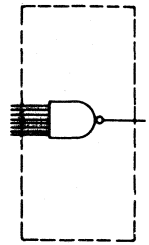
TRIPLE 3-INPUT
POSITIVE NAND GATES

SN54L20
SN74L20
See page 4-7



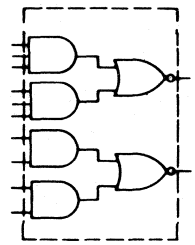
DUAL 4-INPUT
POSITIVE NAND GATES

SN54L30
SN74L30
See page 4-8



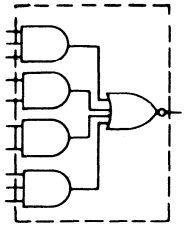
8-INPUT
POSITIVE NAND GATES

SN54L51
SN74L51
See page 4-9



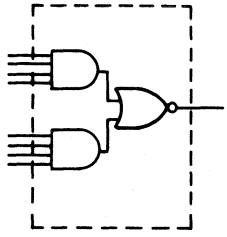
DUAL 2-WIDE
AND-OR-INVERT GATES

SN54L54
SN74L54
See page 4-10



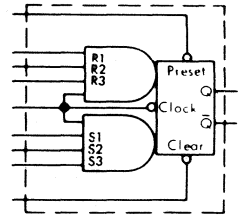
4-WIDE 3-2-2-3-INPUT
AND-OR-INVERT GATES

SN54L55
SN74L55
See page 4-11



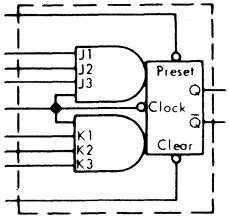
2-WIDE 4-INPUT
AND-OR-INVERT GATES

SN54L71
SN74L71
See page 4-12



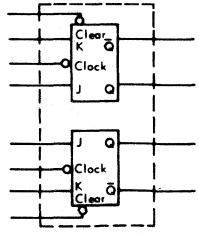
R-S MASTER-SLAVE
FLIP-FLOPS

SN54L72
SN74L72
See page 4-15



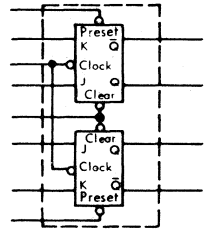
J-K MASTER-SLAVE
FLIP-FLOPS

SN54L73
SN74L73
See page 4-18



DUAL J-K
MASTER-SLAVE FLIP-FLOPS

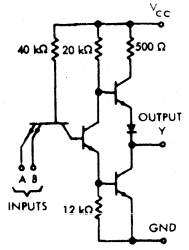
SN54L78
SN74L78
See page 4-21



DUAL J-K
MASTER-SLAVE FLIP-FLOPS

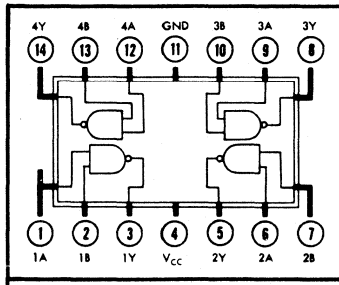
CIRCUIT TYPES SN54L00, SN74L00
QUADRUPLE 2-INPUT POSITIVE NAND GATES

schematic (each gate)

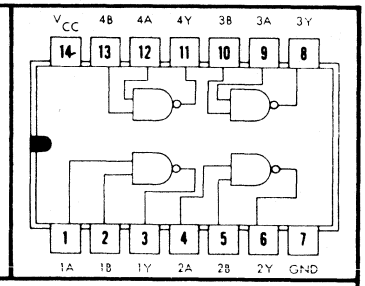


NOTE: Component values shown are nominal.

T
FLAT PACKAGE (TOP VIEW)



J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



positive logic

$Y = \overline{AB}$

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply Voltage V_{CC}: SN54L00 Circuits	4.5	5	5.5	V
SN74L00 Circuits	4.75	5	5.25	V
Normalized Fan-Out From Each Output, N			10	
Operating Free-Air Temperature Range, T_A: SN54L00 Circuits	−55	25	125	°C
SN74L00 Circuits	0	25	70	°C

electrical characteristics (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS†	MIN	MAX	UNIT
$V_{in(1)}$	Logical 1 input voltage required at all input terminals to ensure logical 0 level at output	1	V_{CC} = MIN	2		V
$V_{in(0)}$	Logical 0 input voltage required at any input terminal to ensure logical 1 level at output	2	V_{CC} = MIN		0.7	V
$V_{out(1)}$	Logical 1 output voltage	2	V_{CC} = MIN, V_{in} = 0.7 V, I_{load} = −100 μA	2.4		V
$V_{out(0)}$	Logical 0 output voltage	1	V_{CC} = MIN, V_{in} = 2 V, I_{sink} = 2 mA		0.3	V
$I_{in(0)}$	Logical 0 level input current (each input)	3	V_{CC} = MAX, V_{in} = 0.3 V		−0.18	mA
$I_{in(1)}$	Logical 1 level input current (each input)	4	V_{CC} = MAX, V_{in} = 2.4 V		10	μA
			V_{CC} = MAX, V_{in} = 5.5 V		100	μA
I_{OS}	Short-circuit output current	5	V_{CC} = MAX, V_{in} = 0, V_{out} = 0	−3	−15	mA
$I_{CC(0)}$	Logical 0 level supply current (average per gate)	6	V_{CC} = MAX, V_{in} = 5 V		0.51	mA
$I_{CC(1)}$	Logical 1 level supply current (average per gate)	6	V_{CC} = MAX, V_{in} = 0		0.2	mA

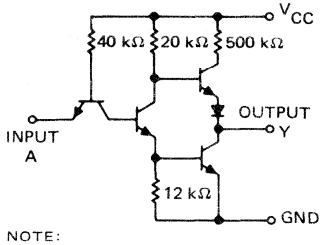
switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{pd0}	Propagation delay time to logical 0 level	35	C_L = 50 pF, R_L = 4 kΩ		31	60	ns
t_{pd1}	Propagation delay time to logical 1 level	35	C_L = 50 pF, R_L = 4 kΩ		35	60	ns

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable circuit type.

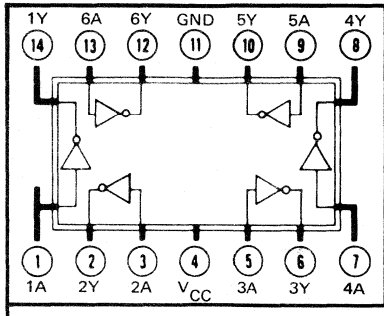
— SEE ORDERING INSTRUCTIONS PAGE 1-1 —

schematic (each inverter)

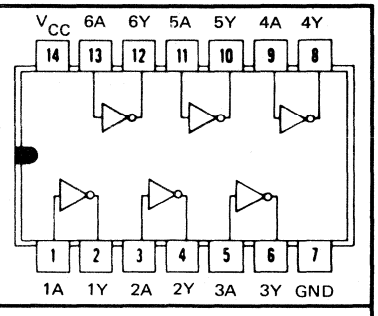


NOTE:
Component values shown are nominal.

T
FLAT PACKAGE (TOP VIEW)



J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



positive logic
$Y = \overline{A}$

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply Voltage V_{CC}:	SN54L04 Circuits	4.5	5	5.5	V
	SN74L04 Circuits	4.75	5	5.25	V
Normalized Fan-Out From Each Output, N				10	
Operating Free-Air Temperature Range, T_A:	SN54L04 Circuits	−55	25	125	°C
	SN74L04 Circuits	0	25	70	°C

electrical characteristics (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS†	MIN	MAX	UNIT
$V_{in(1)}$	Logical 1 input voltage required at input terminal to ensure logical 0 level at output	7	V_{CC} = MIN	2		V
$V_{in(0)}$	Logical 0 input voltage required at input terminal to ensure logical 1 level at output	8	V_{CC} = MIN		0.7	V
$V_{out(1)}$	Logical 1 output voltage	8	V_{CC} = MIN, V_{in} = 0.7 V, I_{load} = −100 μA	2.4		V
$V_{out(0)}$	Logical 0 output voltage	7	V_{CC} = MIN, V_{in} = 2 V, I_{sink} = 2 mA		0.3	V
$I_{in(0)}$	Logical 0 level input current	9	V_{CC} = MAX, V_{in} = 0.3 V		−0.18	mA
$I_{in(1)}$	Logical 1 level input current	10	V_{CC} = MAX, V_{in} = 2.4 V		10	μA
			V_{CC} = MAX, V_{in} = 5.5 V		100	
I_{OS}	Short-circuit output current	11	V_{CC} = MAX, V_{in} = 0, V_{out} = 0	−3	−15	mA
$I_{CC(0)}$	Logical 0 level supply current (Average per inverter)	12	V_{CC} = MAX, V_{in} = 5 V		0.51	mA
$I_{CC(1)}$	Logical 1 level supply current (Average per inverter)	12	V_{CC} = MAX, V_{in} = 0		0.2	mA

switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10

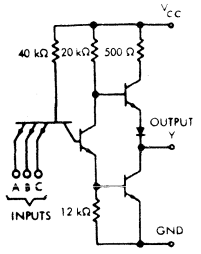
PARAMETER		TEST FIGURE	TEST CONDITIONS†	MIN	TYP	MAX	UNIT
t_{pd0}	Propagation delay time to logical 0 level	35	C_L = 50 pF, R_L = 4 kΩ		31	60	ns
t_{pd1}	Propagation delay time to logical 1 level	35	C_L = 50 pF, R_L = 4 kΩ		35	60	ns

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

–SEE ORDERING INSTRUCTIONS PAGE 1-1–

CIRCUIT TYPES SN54L10, SN74L10
TRIPLE 3-INPUT POSITIVE NAND GATES

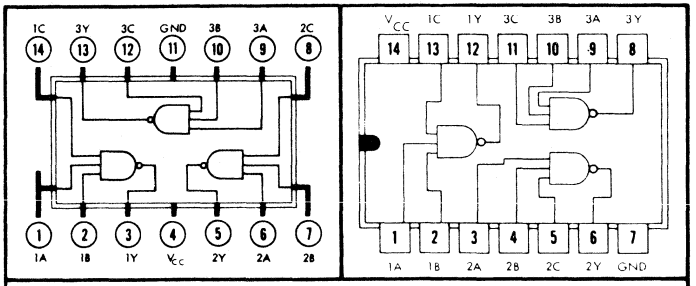
schematic (each gate)



NOTE: Component values shown are nominal.

T
FLAT PACKAGE (TOP VIEW)

J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



positive logic

$Y = \overline{ABC}$

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply Voltage V_{CC}: SN54L10 Circuits	4.5	5	5.5	V
SN74L10 Circuits	4.75	5	5.25	V
Normalized Fan-Out From Each Output, N			10	
Operating Free-Air Temperature Range, T_A: SN54L10 Circuits	−55	25	125	°C
SN74L10 Circuits	0	25	70	°C

electrical characteristics (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS†	MIN	MAX	UNIT
$V_{in(1)}$	Logical 1 input voltage required at all input terminals to ensure logical 0 level at output	1	V_{CC} = MIN	2		V
$V_{in(0)}$	Logical 0 input voltage required at any input terminal to ensure logical 1 level at output	2	V_{CC} = MIN		0.7	V
$V_{out(1)}$	Logical 1 output voltage	2	V_{CC} = MIN, V_{in} = 0.7 V, I_{load} = −100 μA	2.4		V
$V_{out(0)}$	Logical 0 output voltage	1	V_{CC} = MIN, V_{in} = 2 V, I_{sink} = 2 mA		0.3	V
$I_{in(0)}$	Logical 0 level input current (each input)	3	V_{CC} = MAX, V_{in} = 0.3 V		−0.18	mA
$I_{in(1)}$	Logical 1 level input current (each input)	4	V_{CC} = MAX, V_{in} = 2.4 V		10	μA
			V_{CC} = MAX, V_{in} = 5.5 V		100	μA
I_{OS}	Short-circuit output current	5	V_{CC} = MAX, V_{in} = 0, V_{out} = 0	−3	−15	mA
$I_{CC(0)}$	Logical 0 level supply current (average per gate)	6	V_{CC} = MAX, V_{in} = 5 V		0.51	mA
$I_{CC(1)}$	Logical 1 level supply current (average per gate)	6	V_{CC} = MAX, V_{in} = 0		0.2	mA

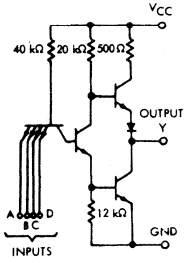
switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{pd0}	Propagation delay time to logical 0 level	35	C_L = 50 pF, R_L = 4 kΩ		31	60	ns
t_{pd1}	Propagation delay time to logical 1 level	35	C_L = 50 pF, R_L = 4 kΩ		35	60	ns

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable circuit type.

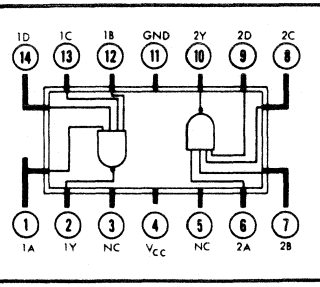
— SEE ORDERING INSTRUCTIONS PAGE 1-1 —

schematic (each gate)

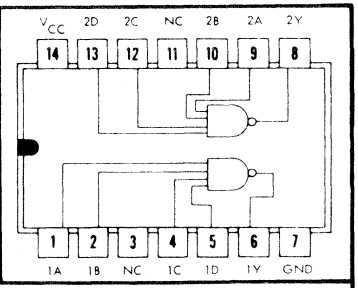


NOTES: 1. Component values shown are nominal.
2. NC — No internal connection.

T
FLAT PACKAGE (TOP VIEW)



J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



positive logic

$Y = \overline{ABCD}$

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply Voltage V_{CC}: SN54L20 Circuits	4.5	5	5.5	V
SN74L20 Circuits	4.75	5	5.25	V
Normalized Fan-Out From Each Output, N			10	
Operating Free-Air Temperature Range, T_A: SN54L20 Circuits	−55	25	125	°C
SN74L20 Circuits	0	25	70	°C

electrical characteristics (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS†	MIN	MAX	UNIT
$V_{in(1)}$	Logical 1 input voltage required at all input terminals to ensure logical 0 level at output	1	V_{CC} = MIN	2		V
$V_{in(0)}$	Logical 0 input voltage required at any input terminal to ensure logical 1 level at output	2	V_{CC} = MIN		0.7	V
$V_{out(1)}$	Logical 1 output voltage	2	V_{CC} = MIN, V_{in} = 0.7 V, I_{load} = −100 μA	2.4		V
$V_{out(0)}$	Logical 0 output voltage	1	V_{CC} = MIN, V_{in} = 2 V, I_{sink} = 2 mA		0.3	V
$I_{in(0)}$	Logical 0 level input current (each input)	3	V_{CC} = MAX, V_{in} = 0.3 V		−0.18	mA
$I_{in(1)}$	Logical 1 level input current (each input)	4	V_{CC} = MAX, V_{in} = 2.4 V		10	μA
			V_{CC} = MAX, V_{in} = 5.5 V		100	μA
I_{OS}	Short-circuit output current	5	V_{CC} = MAX, V_{in} = 0, V_{out} = 0	−3	−15	mA
$I_{CC(0)}$	Logical 0 level supply current (average per gate)	6	V_{CC} = MAX, V_{in} = 5 V		0.51	mA
$I_{CC(1)}$	Logical 1 level supply current (average per gate)	6	V_{CC} = MAX, V_{in} = 0		0.2	mA

switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10

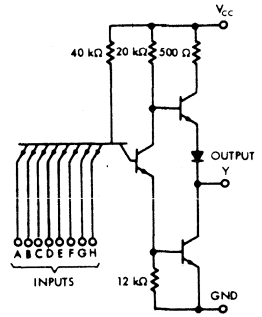
PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{pd0}	Propagation delay time to logical 0 level	35	C_L = 50 pF, R_L = 4 kΩ		31	60	ns
t_{pd1}	Propagation delay time to logical 1 level	35	C_L = 50 pF, R_L = 4 kΩ		35	60	ns

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable circuit type.

— SEE ORDERING INSTRUCTIONS PAGE 1-1 —

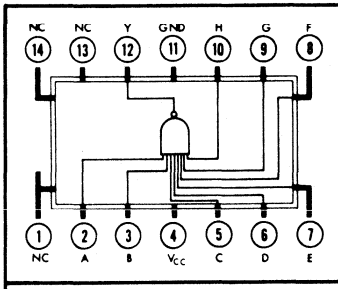
CIRCUIT TYPES SN54L30, SN74L30
8-INPUT POSITIVE NAND GATES

schematic

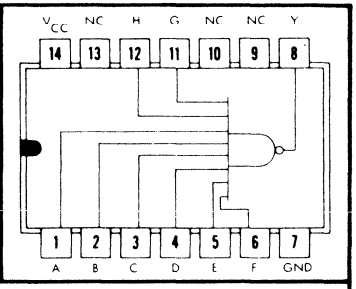


NOTES: 1. Component values shown are nominal.
2. NC — No internal connection

T
FLAT PACKAGE (TOP VIEW)



J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



positive logic

$Y = \overline{ABCDEFGH}$

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply Voltage V_{CC}: SN54L30 Circuits	4.5	5	5.5	V
SN74L30 Circuits	4.75	5	5.25	V
Normalized Fan-Out From Each Output, N			10	
Operating Free-Air Temperature Range, T_A: SN54L30 Circuits	−55	25	125	°C
SN74L30 Circuits	0	25	70	°C

electrical characteristics (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS†		MIN	MAX	UNIT
$V_{in(1)}$	Logical 1 input voltage required at all input terminals to ensure logical 0 level at output	1	V_{CC} = MIN		2		V
$V_{in(0)}$	Logical 0 input voltage required at any input terminal to ensure logical 1 level at output	2	V_{CC} = MIN			0.7	V
$V_{out(1)}$	Logical 1 output voltage	2	V_{CC} = MIN, V_{in} = 0.7 V, I_{load} = −100 μA		2.4		V
$V_{out(0)}$	Logical 0 output voltage	1	V_{CC} = MIN, V_{in} = 2 V, I_{sink} = 2 mA			0.3	V
$I_{in(0)}$	Logical 0 level input current (each input)	3	V_{CC} = MAX, V_{in} = 0.3 V			−0.18	mA
$I_{in(1)}$	Logical 1 level input current (each input)	4	V_{CC} = MAX, V_{in} = 2.4 V			10	μA
			V_{CC} = MAX, V_{in} = 5.5 V			100	μA
I_{os}	Short-circuit output current	5	V_{CC} = MAX, V_{in} = 0, V_{out} = 0		−3	−15	mA
$I_{CC(0)}$	Logical 0 level supply current	6	V_{CC} = MAX, V_{in} = 5 V			0.51	mA
$I_{CC(1)}$	Logical 1 level supply current	6	V_{CC} = MAX, V_{in} = 0	SN54L30		0.33	mA
				SN74L30		0.2	

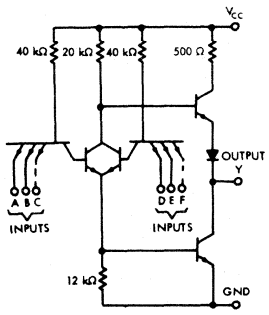
switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{pd0}	Propagation delay time to logical 0 level	35	C_L = 50 pF, R_L = 4 kΩ		70	100	ns
t_{pd1}	Propagation delay time to logical 1 level	35	C_L = 50 pF, R_L = 4 kΩ		35	60	ns

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable circuit type.

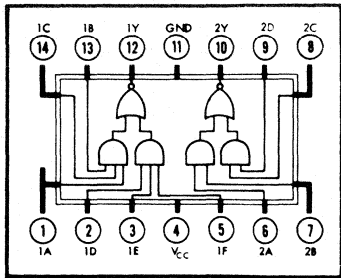
— SEE ORDERING INSTRUCTIONS PAGE 1-1 —

schematic (each gate)

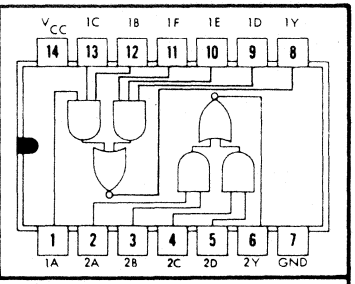


NOTES: 1. Component values shown are nominal.
2. Inputs C and F are available on gate 1 only.

T
FLAT PACKAGE (TOP VIEW)



J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



positive logic

$$1Y = \overline{(1A \cdot 1B \cdot 1C) + (1D \cdot 1E \cdot 1F)}$$

$$2Y = \overline{(2A \cdot 2B) + (2C \cdot 2D)}$$

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply Voltage V_{CC}: SN54L51 Circuits	4.5	5	5.5	V
SN74L51 Circuits	4.75	5	5.25	V
Normalized Fan-Out From Each Output, N			10	
Operating Free-Air Temperature Range, T_A: SN54L51 Circuits	−55	25	125	°C
SN74L51 Circuits	0	25	70	°C

electrical characteristics (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS†	MIN	MAX	UNIT
$V_{in(1)}$	Logical 1 input voltage required at all input terminals of either AND section to ensure logical 0 at output	13	V_{CC} = MIN	2		V
$V_{in(0)}$	Logical 0 input voltage required at one input terminal of each AND section to ensure logical 1 at output	14	V_{CC} = MIN		0.7	V
$V_{out(1)}$	Logical 1 output voltage	14	V_{CC} = MIN, V_{in} = 0.7 V, I_{load} = −100 μA	2.4		V
$V_{out(0)}$	Logical 0 output voltage	13	V_{CC} = MIN, V_{in} = 2 V, I_{sink} = 2 mA		0.3	V
$I_{in(0)}$	Logical 0 level input current (each input)	15	V_{CC} = MAX, V_{in} = 0.3 V		−0.18	mA
$I_{in(1)}$	Logical 1 level input current (each input)	16	V_{CC} = MAX, V_{in} = 2.4 V		10	μA
			V_{CC} = MAX, V_{in} = 5.5 V		100	μA
I_{os}	Short-circuit output current	17	V_{CC} = MAX, V_{in} = 0, V_{out} = 0	−3	−15	mA
$I_{CC(0)}$	Logical 0 level supply current (average per gate)	18	V_{CC} = MAX, V_{in} = 5 V		0.65	mA
$I_{CC(1)}$	Logical 1 level supply current (average per gate)	18	V_{CC} = MAX, V_{in} = 0		0.4	mA

switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10

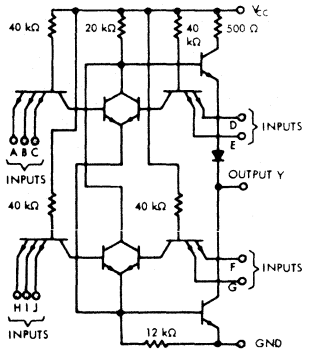
PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{pd0}	Propagation delay time to logical 0 level	35	C_L = 50 pF, R_L = 4 kΩ		35	60	ns
t_{pd1}	Propagation delay time to logical 1 level	35	C_L = 50 pF, R_L = 4 kΩ		50	90	ns

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable circuit type.

— SEE ORDERING INSTRUCTIONS PAGE 1-1 —

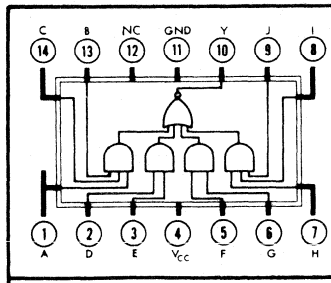
CIRCUIT TYPES SN54L54, SN74L54
4-WIDE 3-2-2-3-INPUT AND-OR-INVERT GATES

schematic



NOTE: 1. Component values shown are nominal.
2. NC — No internal connection

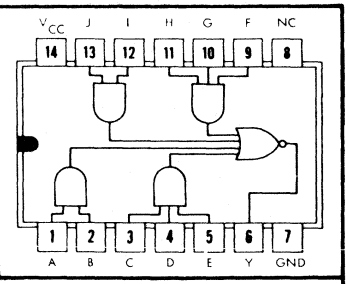
T
FLAT PACKAGE (TOP VIEW)



positive logic

$Y = \overline{(ABC) + (DE) + (FG) + (HIJ)}$

J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



positive logic:

$Y = \overline{(AB) + (CDE) + (FGH) + (IJ)}$

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply Voltage V_{CC}: SN54L54 Circuits	4.5	5	5.5	V
SN74L54 Circuits	4.75	5	5.25	V
Normalized Fan-Out From Each Output, N			10	
Operating Free-Air Temperature Range, T_A: SN54L54 Circuits	−55	25	125	°C
SN74L54 Circuits	0	25	70	°C

electrical characteristics (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER	TEST FIGURE	TEST CONDITIONS†	MIN	MAX	UNIT
$V_{in(1)}$ Logical 1 input voltage required at all input terminals of one AND section to ensure logical 0 at output	13	V_{CC} = MIN	2		V
$V_{in(0)}$ Logical 0 input voltage required at one input terminal of each AND section to ensure logical 1 at output	14	V_{CC} = MIN		0.7	V
$V_{out(1)}$ Logical 1 output voltage	14	V_{CC} = MIN, V_{in} = 0.7 V, I_{load} = −100 μA	2.4		V
$V_{out(0)}$ Logical 0 output voltage	13	V_{CC} = MIN, V_{in} = 2 V, I_{sink} = 2 mA		0.3	V
$I_{in(0)}$ Logical 0 level input current (each input)	15	V_{CC} = MAX, V_{in} = 0.3 V		−0.18	mA
$I_{in(1)}$ Logical 1 level input current (each input)	16	V_{CC} = MAX, V_{in} = 2.4 V		10	μA
		V_{CC} = MAX, V_{in} = 5.5 V		100	μA
I_{OS} Short-circuit output current	17	V_{CC} = MAX, V_{in} = 0, V_{out} = 0	−3	−15	mA
$I_{CC(0)}$ Logical 0 level supply current	18	V_{CC} = MAX, V_{in} = 5 V		0.99	mA
$I_{CC(1)}$ Logical 1 level supply current	18	V_{CC} = MAX, V_{in} = 0		0.8	mA

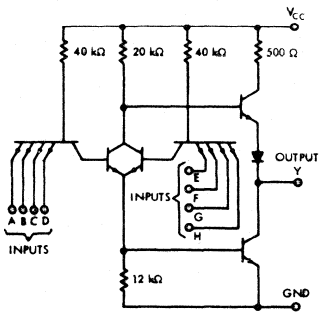
switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10

PARAMETER	TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{pd0} Propagation delay time to logical 0 level	35	C_L = 50 pF, R_L = 4 kΩ		35	60	ns
t_{pd1} Propagation delay time to logical 1 level	35	C_L = 50 pF, R_L = 4 kΩ		50	90	ns

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable circuit type.

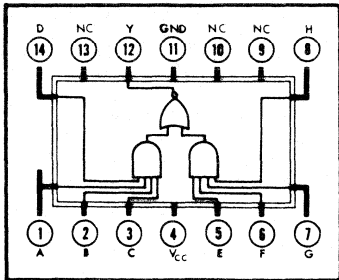
— SEE ORDERING INSTRUCTIONS PAGE 1-1 —

schematic

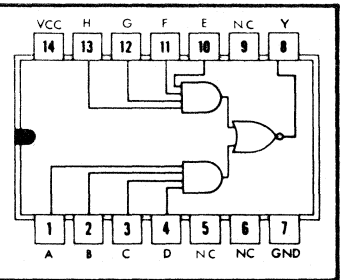


NOTE: 1. Component values shown are nominal.
2. NC — No internal connection

T
FLAT PACKAGE (TOP VIEW)



J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



positive logic

$Y = \overline{(ABCD) + (EFGH)}$

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply Voltage V_{CC}: SN54L55 Circuits	4.5	5	5.5	V
SN74L55 Circuits	4.75	5	5.25	V
Normalized Fan-Out From Each Output, N			10	
Operating Free-Air Temperature Range, T_A: SN54L55 Circuits	−55	25	125	°C
SN74L55 Circuits	0	25	70	°C

electrical characteristics (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS†	MIN	MAX	UNIT
$V_{in(1)}$	Logical 1 input voltage required at all input terminals of either AND section to ensure logical 0 at output	13	V_{CC} = MIN	2		V
$V_{in(0)}$	Logical 0 input voltage required at one input terminal of each AND section to ensure logical 1 at output	14	V_{CC} = MIN		0.7	V
$V_{out(1)}$	Logical 1 output voltage	14	V_{CC} = MIN, V_{in} = 0.7 V, I_{load} = −100 μA	2.4		V
$V_{out(0)}$	Logical 0 output voltage	13	V_{CC} = MIN, V_{in} = 2 V, I_{sink} = 2 mA		0.3	V
$I_{in(0)}$	Logical 0 level input current (each input)	15	V_{CC} = MAX, V_{in} = 0.3 V		−0.18	mA
$I_{in(1)}$	Logical 1 level input current (each input)	16	V_{CC} = MAX, V_{in} = 2.4 V		10	μA
			V_{CC} = MAX, V_{in} = 5.5 V		100	μA
I_{OS}	Short-circuit output current	17	V_{CC} = MAX, V_{in} = 0, V_{out} = 0	−3	−15	mA
$I_{CC(0)}$	Logical 0 level supply current	18	V_{CC} = MAX, V_{in} = 5 V		0.65	mA
$I_{CC(1)}$	Logical 1 level supply current	18	V_{CC} = MAX, V_{in} = 0		0.4	mA

switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{pd0}	Propagation delay time to logical 0 level	35	C_L = 50 pF, R_L = 4 kΩ		35	60	ns
t_{pd1}	Propagation delay time to logical 1 level	35	C_L = 50 pF, R_L = 4 kΩ		50	90	ns

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable circuit type.

— SEE ORDERING INSTRUCTIONS PAGE 1-1 —

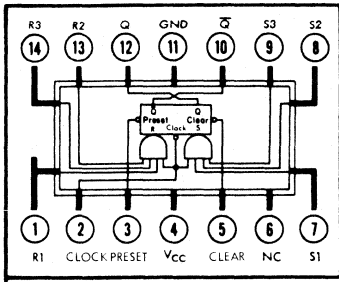
CIRCUIT TYPES SN54L71, SN74L71
R-S MASTER-SLAVE FLIP-FLOPS

logic

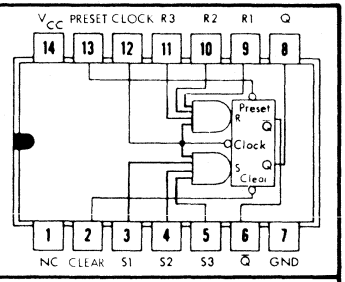
TRUTH TABLE		
t_n		t_{n+1}
R	S	Q
0	0	Q_n
0	1	1
1	0	0
1	1	Indeterminate

NOTES: 1. $R = \overline{R1} \cdot \overline{R2} \cdot \overline{R3}$
2. $S = S1 \cdot S2 \cdot S3$
3. t_n = Bit time before clock pulse.
4. t_{n+1} = Bit time after clock pulse.
5. NC — No internal connection.

T
FLAT PACKAGE (TOP VIEW)



J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)

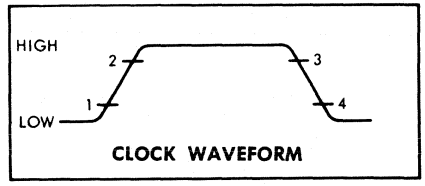


positive logic
Low input to preset sets Q to logical 1
Low input to clear sets Q to logical 0
Preset and clear are independent of clock

description

These R-S flip-flop circuits are based on the master-slave principle. The AND gate inputs for entry into the master section are controlled by the clock pulse. The clock pulse also regulates the state of the coupling transistors which connect the master and slave sections. The sequence of operation is as follows:

1. Isolate slave from master
2. Enter information from AND gate inputs to master
3. Disable AND gate inputs
4. Transfer information from master to slave.



CLOCK WAVEFORM

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply Voltage V_{CC}: SN54L71 Circuits	4.5	5	5.5	V
SN74L71 Circuits	4.75	5	5.25	V
Normalized Fan-Out From Each Output, N			10	
Width of Clock Pulse, $t_{p(clock)}$ (See figure 36)	200			ns
Width of Preset Pulse, $t_{p(preset)}$ (See figure 37)	100			ns
Width of Clear Pulse, $t_{p(clear)}$ (See figure 37)	100			ns
Input Setup Time, t_{setup} (See figure 36)	100			ns
Input Hold Time, t_{hold}	0			
Operating Free-Air Temperature Range, T_A: SN54L71 Circuits	−55	25	125	°C
SN74L71 Circuits	0	25	70	°C

— SEE ORDERING INSTRUCTIONS PAGE 1-1 —

electrical characteristics (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS†	MIN	MAX	UNIT
$V_{in(1)}$	Input voltage required to ensure logical 1 at any input terminal	19 and 20	V_{CC} = MIN	2		V
$V_{in(0)}$	Input voltage required to ensure logical 0 at any input terminal except clock	19 and 20	V_{CC} = MIN		0.7	V
$V_{in(0)}$	Input voltage required to ensure logical 0 at clock input terminal	19 and 20	V_{CC} = MIN		0.6	V
$V_{out(1)}$	Logical 1 output voltage	19	V_{CC} = MIN, I_{load} = −100 μA	2.4		V
$V_{out(0)}$	Logical 0 output voltage	20	V_{CC} = MIN, I_{sink} = 2 mA		0.3	V
$I_{in(0)}$	Logical 0 level input current at R1, R2, R3, S1, S2, or S3	21	V_{CC} = MAX, V_{in} = 0.3 V		−0.18	mA
$I_{in(0)}$	Logical 0 level input current at preset, clear, or clock	21	V_{CC} = MAX, V_{in} = 0.3 V		−0.36∫	mA
$I_{in(1)}$	Logical 1 level input current at R1, R2, R3, S1, S2, or S3	22	V_{CC} = MAX, V_{in} = 2.4 V		10	μA
			V_{CC} = MAX, V_{in} = 5.5 V		100	μA
$I_{in(1)}$	Logical 1 level input current at preset or clear	22	V_{CC} = MAX, V_{in} = 2.4 V		20	μA
			V_{CC} = MAX, V_{in} = 5.5 V		200	μA
$I_{in(1)}$	Logical 1 level input current at clock	22	V_{CC} = MAX, V_{in} = 2.4 V	0∫	−0.2∫	mA
			V_{CC} = MAX, V_{in} = 5.5 V		200∫	μA
I_{OS}	Short-circuit output current	23	V_{CC} = MAX, V_{in} = 0, V_{out} = 0	−3	−15	mA
I_{CC}	Supply current	22	V_{CC} = MAX, $V_{in(clock)}$ = 0		1.44	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable circuit type.
∫For typical clock input current see page 4-35.

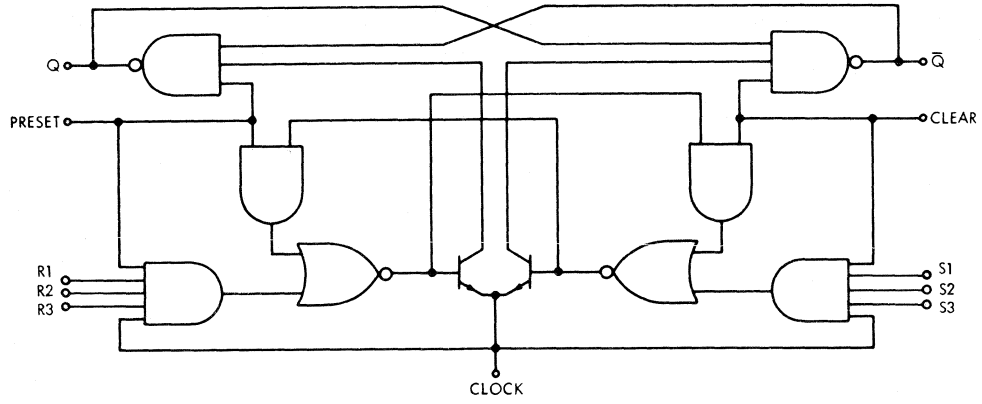
switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{clock}	Maximum clock frequency	36	C_L = 50 pF, R_L = 4 kΩ		3		MHz
t_{pd1}	Propagation delay time to logical 1 level from clear or preset to output	37	C_L = 50 pF, R_L = 4 kΩ		35	75	ns
t_{pd0}	Propagation delay time to logical 0 level from clear or preset to output	37	C_L = 50 pF, R_L = 4 kΩ, $V_{in(clock)}$ = 2.4 V		60	150	ns
			C_L = 50 pF, R_L = 4 kΩ, $V_{in(clock)}$ = 0 V			200	ns
t_{pd1}	Propagation delay time to logical 1 level from clock to output	36	C_L = 50 pF, R_L = 4 kΩ	10	35	75	ns
t_{pd0}	Propagation delay time to logical 0 level from clock to output	36	C_L = 50 pF, R_L = 4 kΩ	10	60	150	ns

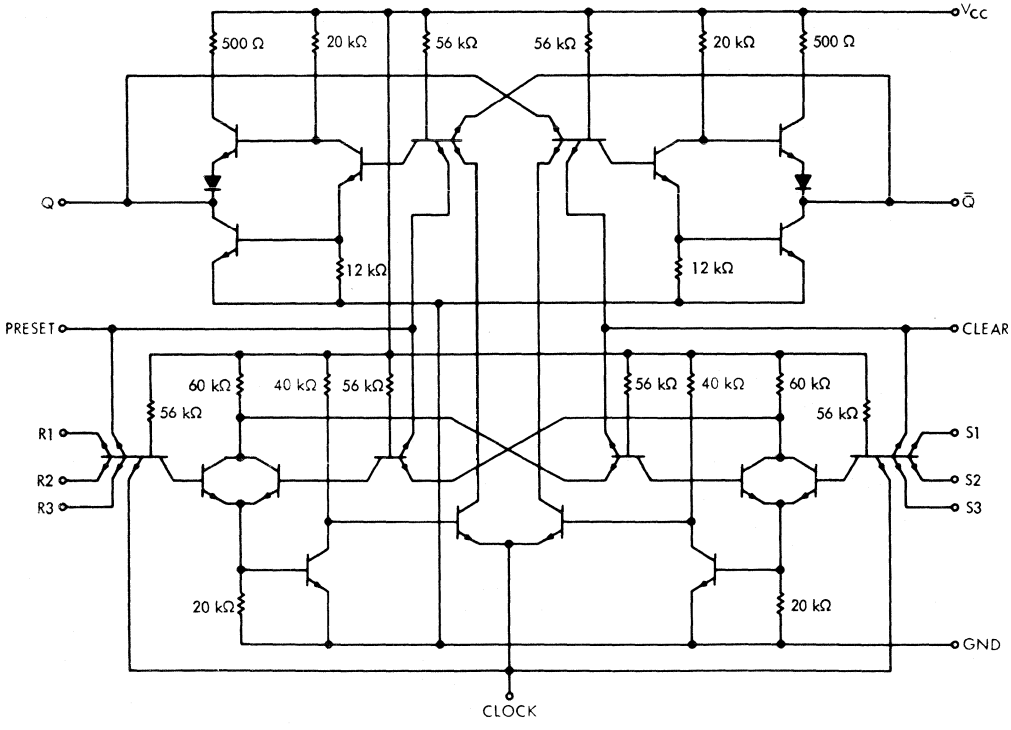
— SEE ORDERING INSTRUCTIONS PAGE 1-1 —

CIRCUIT TYPES SN54L71, SN74L71
R-S MASTER-SLAVE FLIP-FLOPS

functional block diagram



schematic



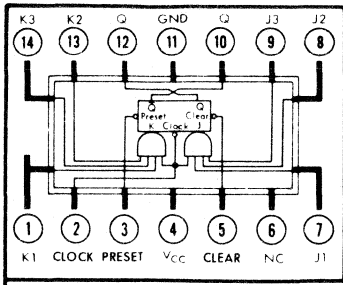
— SEE ORDERING INSTRUCTIONS PAGE 1-1 —

logic

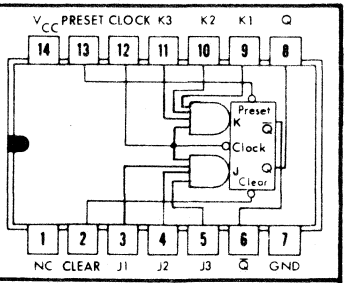
TRUTH TABLE		
t_n		t_{n+1}
J	K	Q
0	0	Q_n
0	1	0
1	0	1
1	1	$\overline{Q}_n$

NOTES: 1. J = J1 • J2 • J3
2. K = K1 • K2 • K3
3. t_n = Bit time before clock pulse.
4. t_{n+1} = Bit time after clock pulse.
5. NC — No internal connection.

T
FLAT PACKAGE (TOP VIEW)



J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



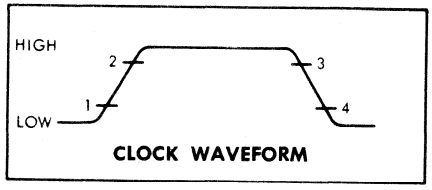
positive logic
Low input to preset sets Q to logical 1
Low input to clear sets Q to logical 0
Preset and clear are independent of clock

description

These J-K flip-flop circuits are based on the master-slave principle. The AND gate inputs for entry into the master section are controlled by the clock pulse. The clock pulse also regulates the state of the coupling transistors which connect the master and slave sections. The sequence of operation is as follows:

1. Isolate slave from master
2. Enter information from AND gate inputs to master
3. Disable AND gate inputs
4. Transfer information from master to slave.

Logical state of J and K inputs must not be allowed to change when the clock pulse is in a high state.



CLOCK WAVEFORM

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply Voltage V_{CC}: SN54L72 Circuits	4.5	5	5.5	V
SN74L72 Circuits	4.75	5	5.25	V
Normalized Fan-Out From Each Output, N			10	
Width of Clock Pulse, $t_{p(clock)}$ (See figure 36)	200			ns
Width of Preset Pulse, $t_{p(preset)}$ (See figure 37)	100			ns
Width of Clear Pulse, $t_{p(clear)}$ (See figure 37)	100			ns
Input Setup Time, t_{setup} (See figure 36)	$\geq t_{p(clock)}$			
Input Hold Time, t_{hold}	0			
Operating Free-Air Temperature Range, T_A: SN54L72 Circuits	−55	25	125	°C
SN74L72 Circuits	0	25	70	°C

— SEE ORDERING INSTRUCTIONS PAGE 1-1 —

electrical characteristics (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS†	MIN	MAX	UNIT
$V_{in(1)}$	Input voltage required to ensure logical 1 at any input terminal	24 and 25	V_{CC} = MIN	2		V
$V_{in(0)}$	Input voltage required to ensure logical 0 at any input terminal except clock	24 and 25	V_{CC} = MIN		0.7	V
$V_{in(0)}$	Input voltage required to ensure logical 0 at clock input terminal	24 and 25	V_{CC} = MIN		0.6	V
$V_{out(1)}$	Logical 1 output voltage	24	V_{CC} = MIN, I_{load} = −100 μA	2.4		V
$V_{out(0)}$	Logical 0 output voltage	25	V_{CC} = MIN, I_{sink} = 2 mA		0.3	V
$I_{in(0)}$	Logical 0 level input current at J1, J2, J3, K1, K2, or K3	26	V_{CC} = MAX, V_{in} = 0.3 V		−0.18	mA
$I_{in(0)}$	Logical 0 level input current at preset, clear, or clock	26	V_{CC} = MAX, V_{in} = 0.3 V		−0.36∫	mA
$I_{in(1)}$	Logical 1 level input current at J1, J2, J3, K1, K2, or K3	27	V_{CC} = MAX, V_{in} = 2.4 V		10	μA
			V_{CC} = MAX, V_{in} = 5.5 V		100	μA
$I_{in(1)}$	Logical 1 level input current at preset or clear	27	V_{CC} = MAX, V_{in} = 2.4 V		20	μA
			V_{CC} = MAX, V_{in} = 5.5 V		200	μA
$I_{in(1)}$	Logical 1 level input current at clock	27	V_{CC} = MAX, V_{in} = 2.4 V	0∫	−0.2∫	mA
			V_{CC} = MAX, V_{in} = 5.5 V		200∫	μA
I_{OS}	Short-circuit output current	28	V_{CC} = MAX, V_{in} = 0, V_{out} = 0	−3	−15	mA
I_{CC}	Supply current	27	V_{CC} = MAX, $V_{in(clock)}$ = 0		1.44	mA

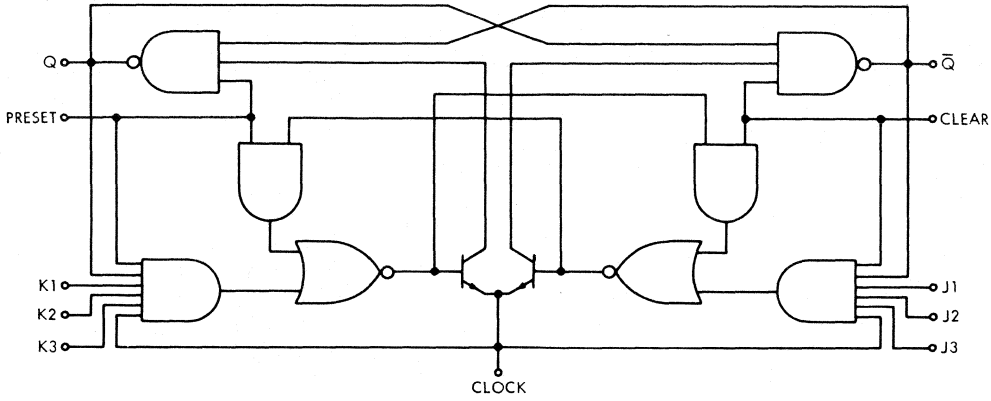
†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable circuit type.
∫For typical clock input current see page 4-35.

switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10

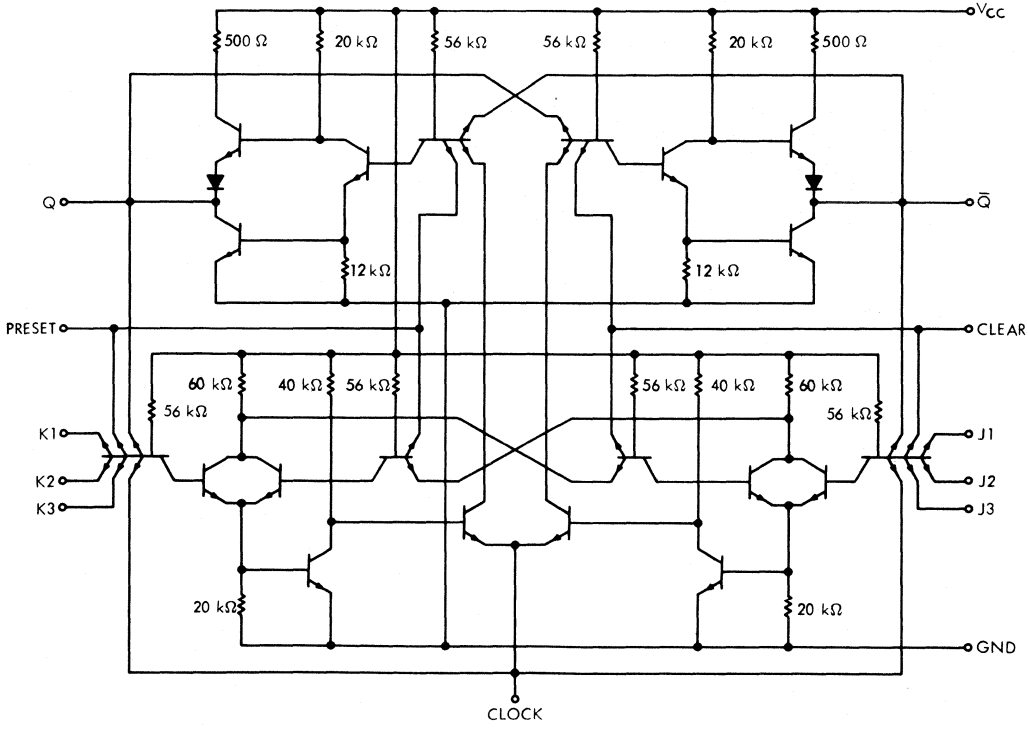
PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{clock}	Maximum clock frequency	36	C_L = 50 pF, R_L = 4 kΩ		3		MHz
t_{pd1}	Propagation delay time to logical 1 level from clear or preset to output	37	C_L = 50 pF, R_L = 4 kΩ		35	75	ns
t_{pd0}	Propagation delay time to logical 0 level from clear or preset to output	37	C_L = 50 pF, R_L = 4 kΩ, $V_{in(clock)}$ = 2.4 V		60	150	ns
			C_L = 50 pF, R_L = 4 kΩ, $V_{in(clock)}$ = 0 V			200	ns
t_{pd1}	Propagation delay time to logical 1 level from clock to output	36	C_L = 50 pF, R_L = 4 kΩ	10	35	75	ns
t_{pd0}	Propagation delay time to logical 0 level from clock to output	36	C_L = 50 pF, R_L = 4 kΩ	10	60	150	ns

— SEE ORDERING INSTRUCTIONS PAGE 1-1 —

functional block diagram



schematic



Component values shown are nominal.

— SEE ORDERING INSTRUCTIONS PAGE 1-1 —

CIRCUIT TYPES SN54L73, SN74L73
DUAL J-K MASTER-SLAVE FLIP-FLOPS

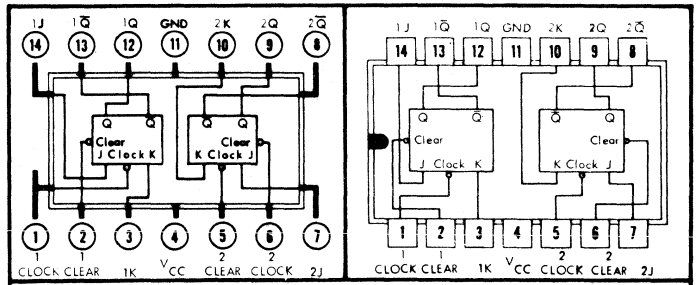
logic

TRUTH TABLE		
t_n		t_{n+1}
J	K	Q
0	0	Q_n
0	1	0
1	0	1
1	1	$\overline{Q}_n$

NOTES: 1. t_n = Bit time before clock pulse.
2. t_{n+1} = Bit time after clock pulse.

T
FLAT PACKAGE (TOP VIEW)

J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



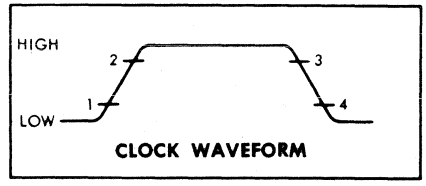
positive logic:
Low input to clear sets Q to logical 0
Clear is independent of clock

description

These J-K flip-flop circuits are based on the master-slave principle. The AND gate inputs for entry into the master section are controlled by the clock pulse. The clock pulse also regulates the state of the coupling transistors which connect the master and slave sections. The sequence of operation is as follows:

1. Isolate slave from master
2. Enter information from AND gate inputs to master
3. Disable AND gate inputs
4. Transfer information from master to slave.

Logical state of J and K inputs must not be allowed to change when the clock pulse is in a high state.



CLOCK WAVEFORM

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply Voltage V_{CC}: SN54L73 Circuits	4.5	5	5.5	V
SN74L73 Circuits	4.75	5	5.25	V
Normalized Fan-Out From Each Output, N			10	
Width of Clock Pulse, $t_{p(clock)}$ (See Figure 36)	200			ns
Width of Preset Pulse, $t_{p(preset)}$ (See Figure 37)	100			ns
Width of Clear Pulse, $t_{p(clear)}$ (See Figure 37)	100			ns
Input Setup Time, t_{setup} (See Figure 36)	$\geq t_{p(clock)}$			
Input Hold Time, t_{hold}	0			
Operating Free-Air Temperature Range, T_A: SN54L73 Circuits	−55	25	125	°C
SN74L73 Circuits	0	25	70	°C

— SEE ORDERING INSTRUCTIONS PAGE 1-1 —

electrical characteristics (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS†	MIN	MAX	UNIT
$V_{in(1)}$	Input voltage required to ensure logical 1 at any input terminal	29 and 30	V_{CC} = MIN	2		V
$V_{in(0)}$	Input voltage required to ensure logical 0 at any input terminal except clock	29 and 30	V_{CC} = MIN		0.7	V
$V_{in(0)}$	Input voltage required to ensure logical 0 at clock input terminal	29 and 30	V_{CC} = MIN		0.6	V
$V_{out(1)}$	Logical 1 output voltage	29	V_{CC} = MIN, I_{load} = −100 μA	2.4		V
$V_{out(0)}$	Logical 0 output voltage	30	V_{CC} = MIN, I_{sink} = 2 mA		0.3	V
$I_{in(0)}$	Logical 0 level input current at J or K	31	V_{CC} = MAX, V_{in} = 0.3 V		−0.18	mA
$I_{in(0)}$	Logical 0 level input current at clear or clock	31	V_{CC} = MAX, V_{in} = 0.3 V		−0.36∫	mA
$I_{in(1)}$	Logical 1 level input current at J or K	32	V_{CC} = MAX, V_{in} = 2.4 V		10	μA
			V_{CC} = MAX, V_{in} = 5.5 V		100	μA
$I_{in(1)}$	Logical 1 level input current at clear	32	V_{CC} = MAX, V_{in} = 2.4 V		20	μA
			V_{CC} = MAX, V_{in} = 5.5 V		200	μA
$I_{in(1)}$	Logical 1 level input current at clock	32	V_{CC} = MAX, V_{in} = 2.4 V	0∫	−0.2∫	mA
			V_{CC} = MAX, V_{in} = 5.5 V		200∫	μA
I_{OS}	Short-circuit output current	33	V_{CC} = MAX, V_{in} = 0, V_{out} = 0	−3	−15	mA
I_{CC}	Supply current (average per flip-flop)	32	V_{CC} = MAX, $V_{in(clock)}$ = 0		1.44	mA

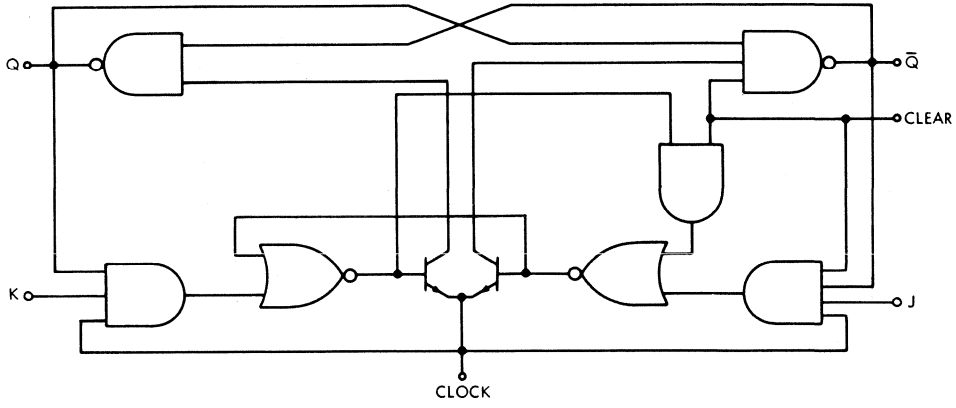
†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable circuit type.
∫For typical clock input current see page 4-35.

switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10

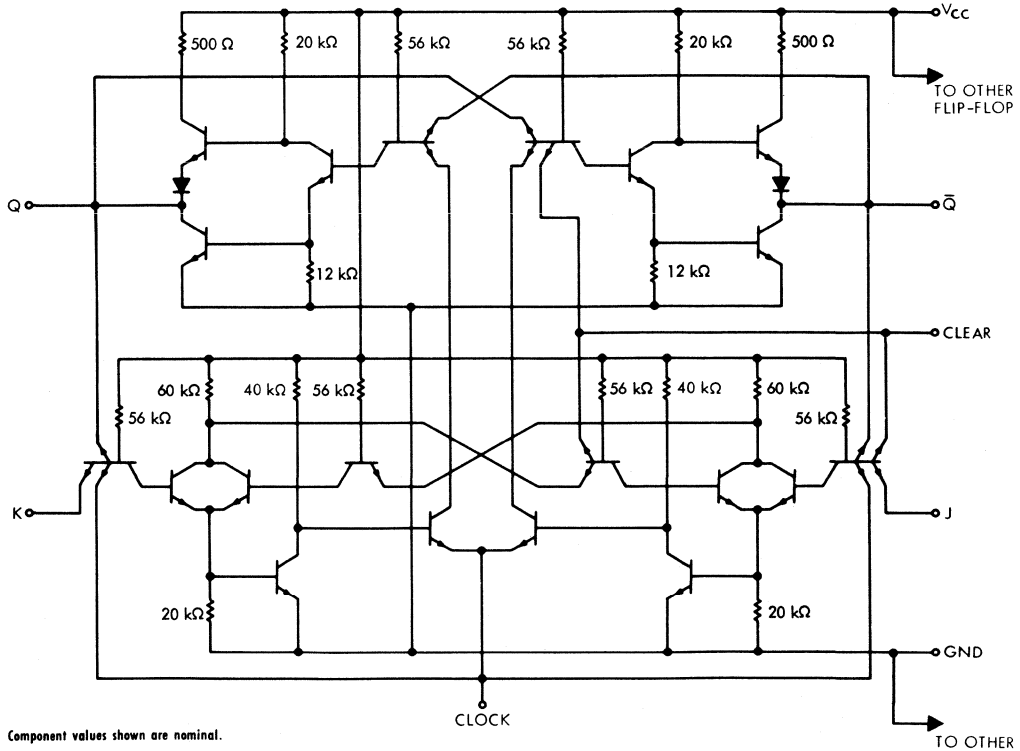
PARAMETER		TEST FIGURE	TEST CONDITIONS		MIN	TYP	MAX	UNIT
f_{clock}	Maximum clock frequency	36	C_L = 50 pF, R_L = 4 kΩ			3		MHz
t_{pd1}	Propagation delay time to logical 1 level from clear to output	37	C_L = 50 pF, R_L = 4 kΩ			35	75	ns
t_{pd0}	Propagation delay time to logical 0 level from clear to output	37	C_L = 50 pF, R_L = 4 kΩ,	$V_{in(clock)}$ = 2.4 V		60	150	ns
				$V_{in(clock)}$ = 0 V			200	
t_{pd0}	Propagation delay time to logical 0 level from clock to output	36	C_L = 50 pF, R_L = 4 kΩ		10	60	150	ns
t_{pd1}	Propagation delay time to logical 1 level from clock to output	36	C_L = 50 pF, R_L = 4 kΩ		10	35	75	ns

— SEE ORDERING INSTRUCTIONS PAGE 1-1 —

functional block diagram (each flip-flop)



schematic (each flip-flop)



NOTE: Component values shown are nominal.

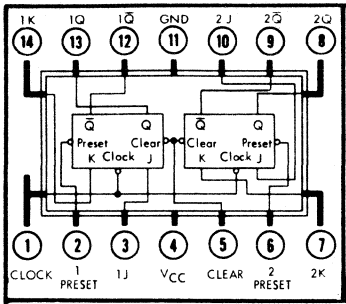
— SEE ORDERING INSTRUCTIONS PAGE 1-1 —

logic

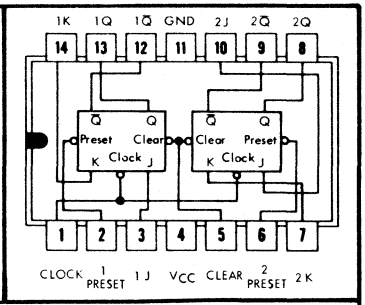
TRUTH TABLE		
t_n		t_{n+1}
J	K	Q
0	0	Q_n
0	1	0
1	0	1
1	1	$\overline{Q}_n$

NOTES: 1. t_n = Bit time before clock pulse.
2. t_{n+1} = Bit time after clock pulse.

T
FLAT PACKAGE (TOP VIEW)



J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



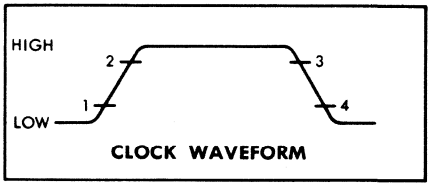
positive logic: Low input to preset sets Q to logical 1
Low input to clear sets Q to logical 0
Preset and clear are independent of clock

description

These J-K flip-flop circuits are based on the master-slave principle. Inputs to the master section are controlled by the clock pulse. The clock pulse also regulates the state of the coupling transistors which connect the master and slave sections. The sequence of operation is as follows:

1. Isolate slave from master
2. Enter information from J and K inputs to master
3. Disable J and K inputs
4. Transfer information from master to slave.

Logical state of J and K inputs must not be allowed to change when the clock pulse is in a high state.



CLOCK WAVEFORM

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply Voltage V_{CC}: SN54L78 Circuits	4.5	5	5.5	V
SN74L78 Circuits	4.75	5	5.25	V
Normalized Fan-Out From Each Output, N			10	
Width of Clock Pulse, $t_{p(clock)}$ (See Figure 36)	200			ns
Width of Preset Pulse, $t_{p(preset)}$ (See Figure 37)	100			ns
Width of Clear Pulse, $t_{p(clear)}$ (See Figure 37)	100			ns
Input Setup Time, t_{setup} (See Figure 36)	$\geq t_{p(clock)}$			
Input Hold Time, t_{hold}	0			
Operating Free-Air Temperature Range, T_A: SN54L78 Circuits	−55	25	125	°C
SN74L78 Circuits	0	25	70	°C

— SEE ORDERING INSTRUCTIONS PAGE 1-1 —

electrical characteristics (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS†	MIN	MAX	UNIT
$V_{in(1)}$	Input voltage required to ensure logical 1 at any input terminal	29 and 30	V_{CC} = MIN	2		V
$V_{in(0)}$	Input voltage required to ensure logical 0 at any input terminal except clock	29 and 30	V_{CC} = MIN		0.7	V
$V_{in(0)}$	Input voltage required to ensure logical 0 at clock input terminal	29 and 30	V_{CC} = MIN,		0.6	V
$V_{out(1)}$	Logical 1 output voltage	29	V_{CC} = MIN, I_{load} = −100 μA	2.4		V
$V_{out(0)}$	Logical 0 output voltage	30	V_{CC} = MIN, I_{sink} = 2 mA		0.3	V
$I_{in(0)}$	Logical 0 level input current at J or K	31	V_{CC} = MAX, V_{in} = 0.3 V		−0.18	mA
$I_{in(0)}$	Logical 0 level input current at preset	31	V_{CC} = MAX, V_{in} = 0.3 V		−0.36	mA
$I_{in(0)}$	Logical 0 level input current at clear or clock	31	V_{CC} = MAX, V_{in} = 0.3 V		−0.72	mA
$I_{in(1)}$	Logical 1 level input current at J or K	32	V_{CC} = MAX, V_{in} = 2.4 V		10	μA
			V_{CC} = MAX, V_{in} = 5.5 V		100	μA
$I_{in(1)}$	Logical 1 level input current at preset	32	V_{CC} = MAX, V_{in} = 2.4 V		20	μA
			V_{CC} = MAX, V_{in} = 5.5 V		200	μA
$I_{in(1)}$	Logical 1 level input current at clear	32	V_{CC} = MAX, V_{in} = 2.4 V		40	μA
			V_{CC} = MAX, V_{in} = 5.5 V		400	μA
$I_{in(1)}$	Logical 1 level input current at clock	32	V_{CC} = MAX, V_{in} = 2.4 V	0§	−0.4§	mA
			V_{CC} = MAX, V_{in} = 5.5 V		400§	μA
I_{os}	Short-circuit output current	34	V_{CC} = MAX, V_{in} = 0, V_{out} = 0	−3	−15	mA
I_{cc}	Supply current (average per flip-flop)	32	V_{CC} = MAX, $V_{in(clock)}$ = 0		1.44	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable circuit type.

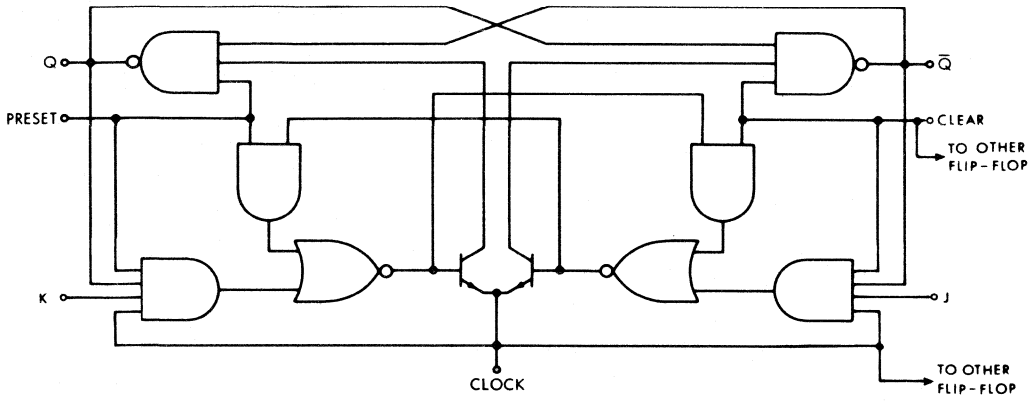
§For typical clock input current see page 4-35.

switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10

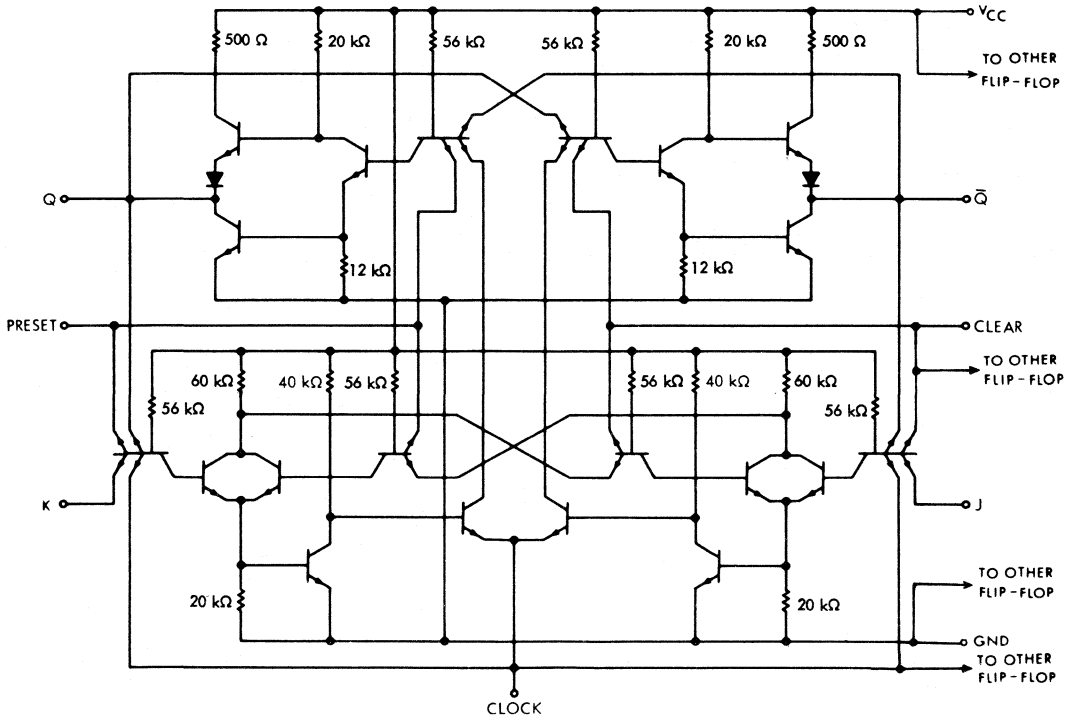
PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{clock}	Maximum clock frequency	36	C_L = 50 pF, R_L = 4 kΩ		3		MHz
t_{pd0}	Propagation delay time to logical 0 level from clear to output	37	C_L = 50 pF, R_L = 4 kΩ, $V_{in(clock)}$ = 2.4 V		60	150	ns
			C_L = 50 pF, R_L = 4 kΩ, $V_{in(clock)}$ = 0 V			200	ns
t_{pd1}	Propagation delay time to logical 1 level from clear to output	37	C_L = 50 pF, R_L = 4 kΩ		35	75	ns
t_{pd1}	Propagation delay time to logical 1 level from clock to output	36	C_L = 50 pF, R_L = 4 kΩ	10	35	75	ns
t_{pd0}	Propagation delay time to logical 0 level from clock to output	36	C_L = 50 pF, R_L = 4 kΩ	10	60	150	ns

— SEE ORDERING INSTRUCTIONS PAGE 1-1 —

functional block diagram (each flip-flop)



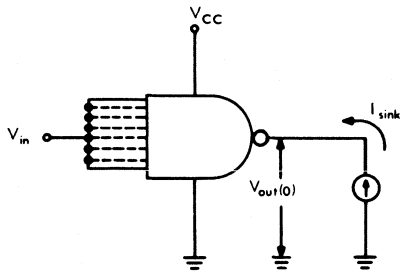
schematic (each flip-flop)



— SEE ORDERING INSTRUCTIONS PAGE 1-1 —

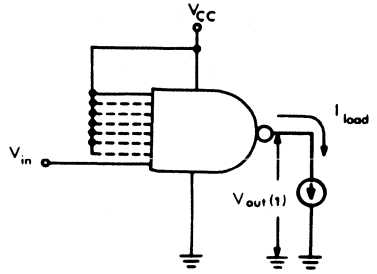
PARAMETER MEASUREMENT INFORMATION

d-c test circuits§



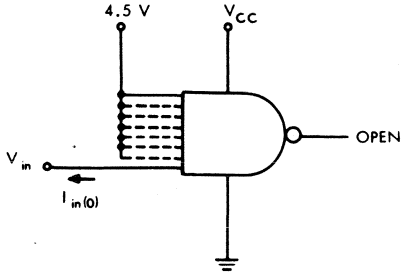
1. All inputs are tested simultaneously.

FIGURE 1



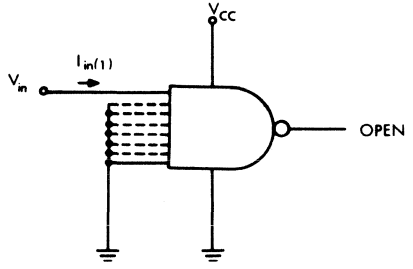
1. Each input is tested separately.

FIGURE 2



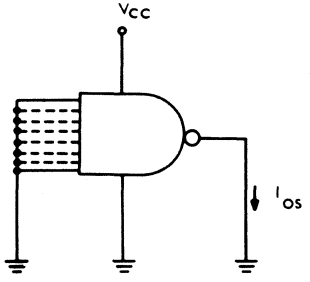
1. Each input is tested separately.

FIGURE 3



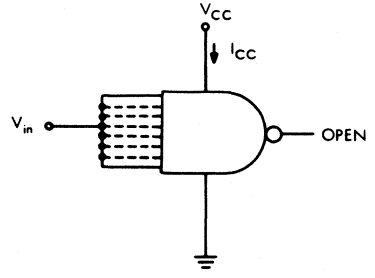
1. Each input is tested separately.

FIGURE 4



1. Each gate is tested separately.

FIGURE 5



1. Logical 0 and logical 1 conditions are tested.
2. All gates are tested simultaneously.

$$\text{Average-per-gate value} = \frac{I_{CC}\ \text{total}}{\text{number of gates in package}}$$

FIGURE 6

§Arrows indicate actual direction of current flow.

PARAMETER MEASUREMENT INFORMATION

d-c test circuits §

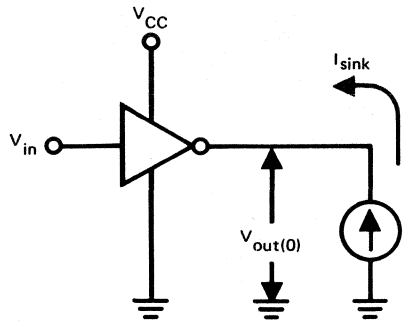


FIGURE 7

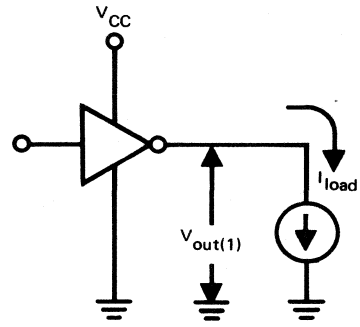


FIGURE 8

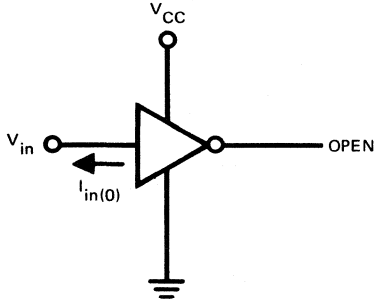


FIGURE 9

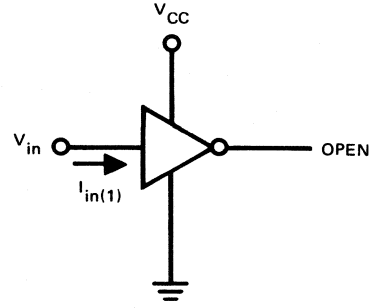
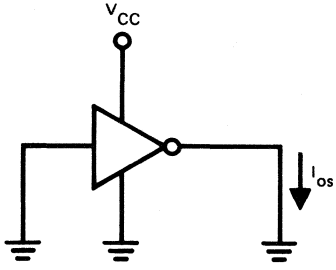
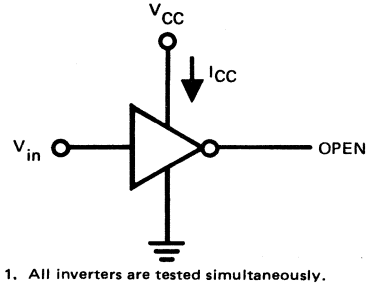


FIGURE 10



1. Each inverter is tested separately.

FIGURE 11



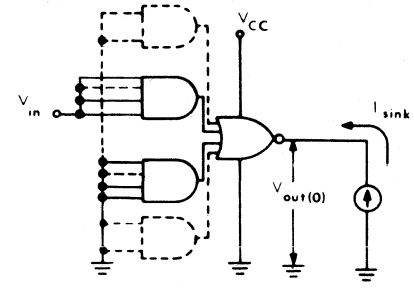
1. All inverters are tested simultaneously.
2. For SN54L04/SN74L04 the average-per-inverter value = $\frac{I_{CC}\text{ total}}{\text{number of inverters in package}}$

FIGURE 12

§ Arrows indicate actual direction of current flow.

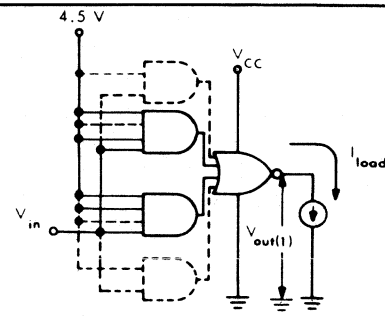
PARAMETER MEASUREMENT INFORMATION

d-c test circuits§ (continued)



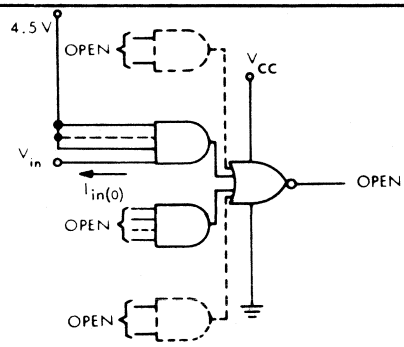
1. Each AND section is tested separately.

FIGURE 13



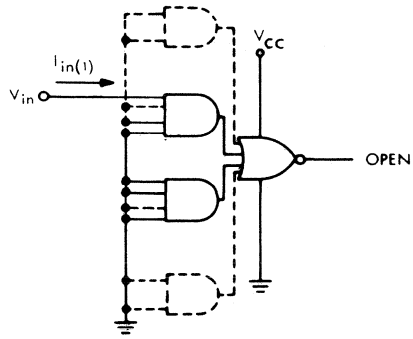
1. Each set of inputs is tested separately.

FIGURE 14



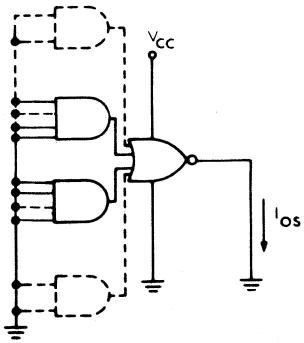
1. Each input is tested separately.

FIGURE 15



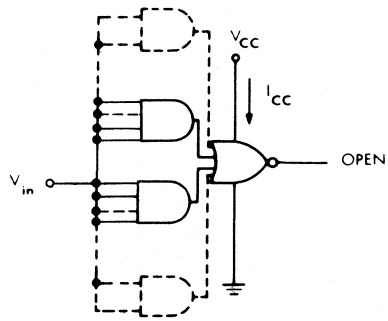
1. Each input is tested separately.

FIGURE 16



1. Each gate is tested separately.

FIGURE 17



1. All gates are tested simultaneously.

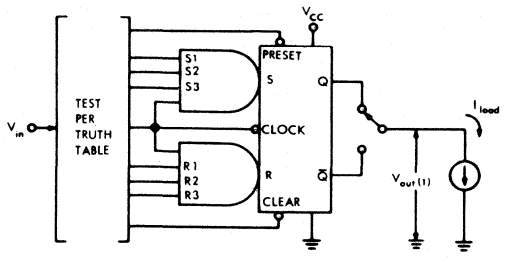
$$\text{Average-per-gate value} = \frac{I_{CC}\ \text{total}}{\text{number of gates in package}}$$

FIGURE 18

§Arrows indicate actual direction of current flow.

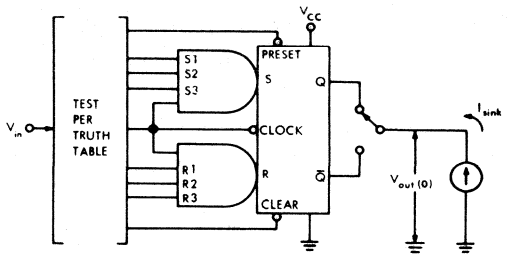
PARAMETER MEASUREMENT INFORMATION

d-c test circuits§ (continued)



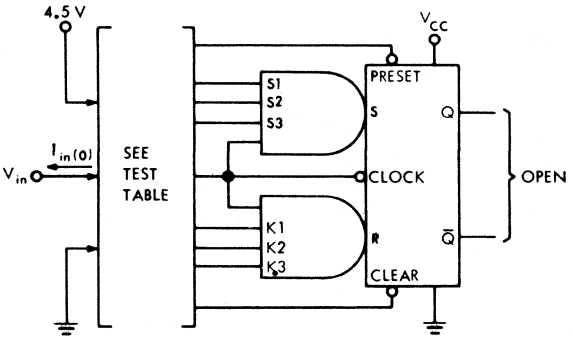
1. Each output is tested separately.

FIGURE 19



1. Each input is tested separately.

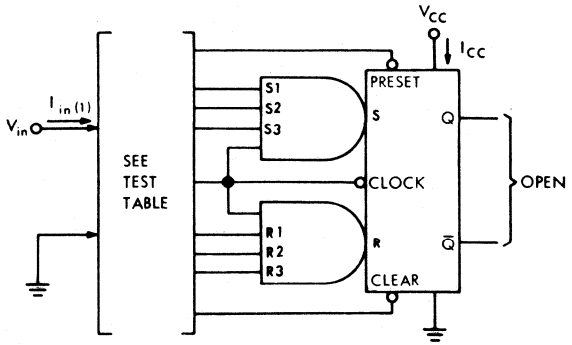
FIGURE 20



TEST TABLE	
Apply V_{in} (Test $I_{in(0)}$)	Apply 4.5 V
Clock	Preset, R1, R2, R3, S1, S2, and S3
Clock	Clear, R1, R2, R3, S1, S2, and S3
Preset	R1, R2, R3, S1, S2, and S3
Clear	R1, R2, R3, S1, S2, and S3
R1	Preset, Clock, R2, and R3
R2	Preset, Clock, R1, and R3
R3	Preset, Clock, R1, and R2
S1	Clear, Clock, S2, and S3
S2	Clear, Clock, S1, and S3
S3	Clear, Clock, S1, and S2

1. Each input is tested separately.

FIGURE 21



TEST TABLE	
Apply V_{in} (Test $I_{in(1)}$)	Ground
Clock	Preset, Clear, R1, R2, R3, S1, S2, and S3
Preset	Clock, R1, R2, and R3
Clear	Clock, S1, S2, and S3
R1	Clock, Preset, R2, and R3
R2	Clock, Preset, R1, and R3
R3	Clock, Preset, R1, and R2
S1	Clock, Clear, S2, and S3
S2	Clock, Clear, S1, and S3
S3	Clock, Clear, S1, and S2

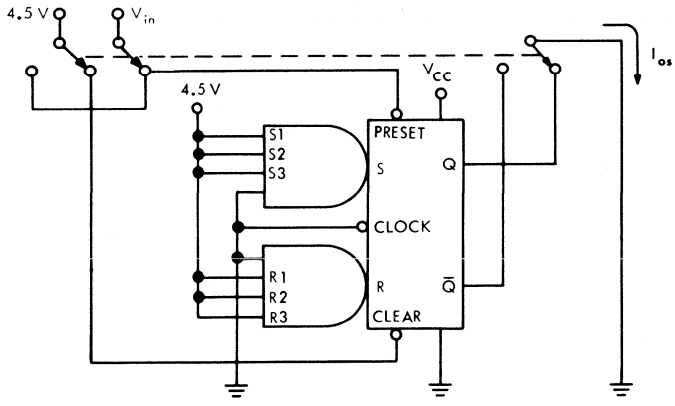
1. Each input is tested separately.

FIGURE 22

§Arrows indicate actual direction of current flow.

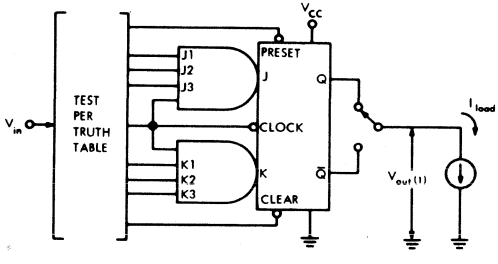
PARAMETER MEASUREMENT INFORMATION

d-c test circuits§ (continued)



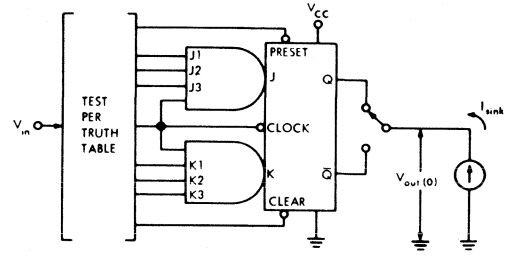
1. Each output is tested separately.

FIGURE 23



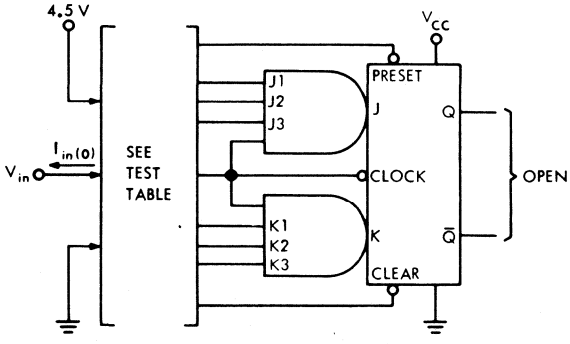
1. Each output is tested separately.

FIGURE 24



1. Each output is tested separately.

FIGURE 25



1. Each input is tested separately.

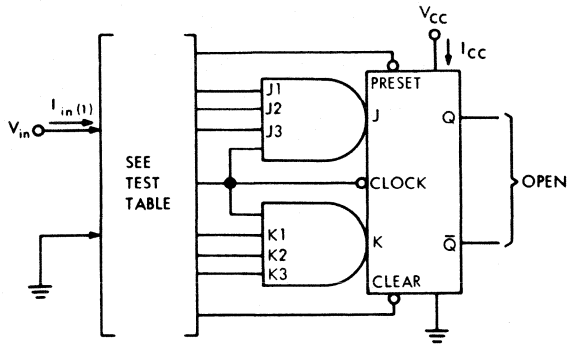
TEST TABLE		
Apply V_{in} (Test $I_{in(0)}$)	Apply Momentary GND, then 4.5 V	Apply 4.5 V
Clock	Preset	J1, J2, J3, K1, K2, and K3
Clock	Clear	J1, J2, J3, K1, K2, and K3
Preset	None	J1, J2, J3, K1, K2, and K3
Clear	None	J1, J2, J3, K1, K2, and K3
J1	Clear	Clock, J2, and J3
J2	Clear	Clock, J1, and J3
J3	Clear	Clock, J1, and J2
K1	Preset	Clock, K2, and K3
K2	Preset	Clock, K1, and K3
K3	Preset	Clock, K1, and K2

FIGURE 26

§Arrows indicate actual direction of current flow.

PARAMETER MEASUREMENT INFORMATION

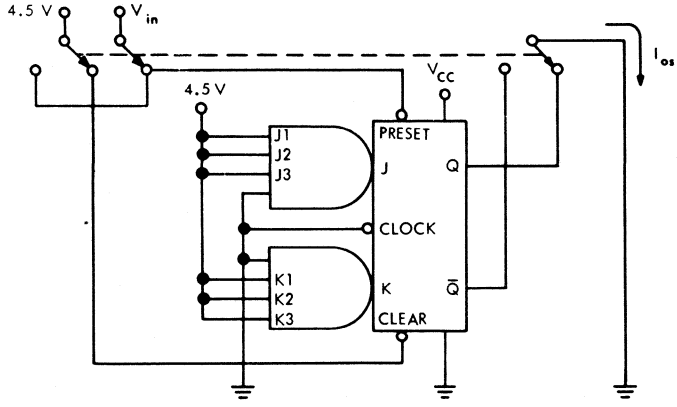
d-c test circuits § (continued)



TEST TABLE	
Apply V_{in} (Test $I_{in(1)}$)	Ground
Clock	Preset, Clear, J1, J2, J3, K1, K2, and K3
Preset	Clock, K1, K2, and K3
Clear	Clock, J1, J2, and J3
J1	Clock, Clear, J2, and J3
J2	Clock, Clear, J1, and J3
J3	Clock, Clear, J1, and J2
K1	Clock, Preset, K2, and K3
K2	Clock, Preset, K1, and K3
K3	Clock, Preset, K1, and K2

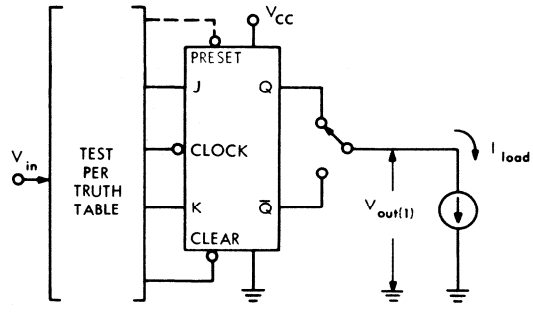
1. Each input is tested separately.

FIGURE 27



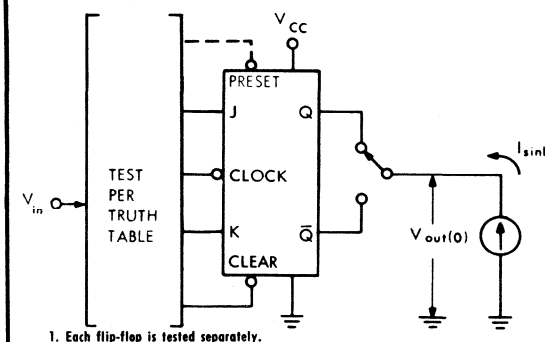
1. Each output is tested separately.

FIGURE 28



1. Each flip-flop is tested separately.
2. Each output is tested separately.
3. Preset is applicable for SN54L78/SN74L78 circuits only.

FIGURE 29



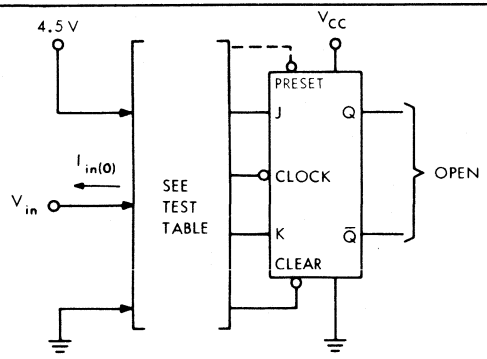
1. Each flip-flop is tested separately.
2. Each output is tested separately.
3. Preset is applicable for SN54L78/SN74L78 circuits only.

FIGURE 30

§Arrows indicate actual direction of current flow.

PARAMETER MEASUREMENT INFORMATION

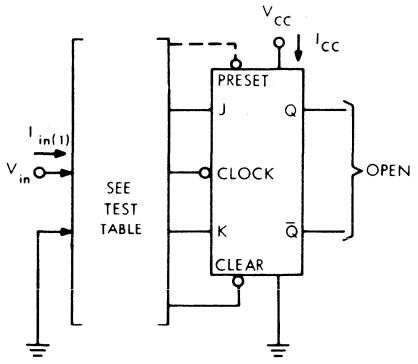
d-c test circuits§ (continued)



TEST TABLE		
Apply V_{in} (Test $I_{in(0)}$)	Apply Momentary GND	Apply 4.5 V
Clock	Clear (See Note 2)	J and K
Clear	None	Clock and J
Preset	None (See Note 5)	Clock and K
J	Q (See Note 3)	Clock and Clear
K	$\overline{Q}$ (See Note 3)	Clock and Clear

1. Each flip-flop is tested separately.
2. Apply momentary ground, then 4.5 V
3. After application of momentary ground, Q and $\overline{Q}$ are left floating.
4. Ground all inputs of the unused flip-flop.
5. Preset is applicable for SN54L78/SN74L78 circuits only.

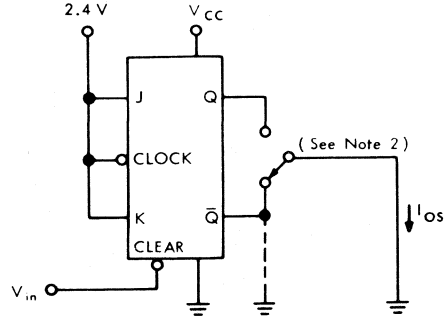
FIGURE 31



TEST TABLE		
Apply V_{in} (Test $I_{in(1)}$)	Ground	Apply Momentary GND, then 4.5 V
Clock	Clear, J, and K	None
Clear	Clock and J	None
Preset (See Note 1)	Clock and K	None
J (See Note 1)	Clock and Clear	Preset
K (See Note 3)	Clock and Preset	Clear

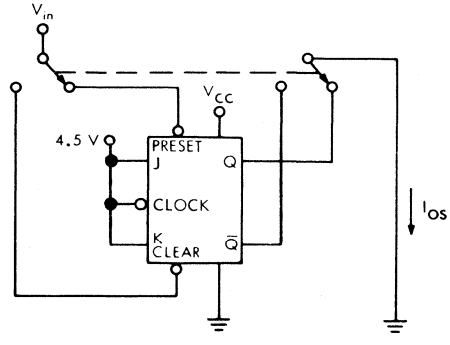
1. Preset is applicable for SN54L78/SN74L78 circuits only.
2. I_{CC} is measured (simultaneously for both flip-flops) for the following conditions:
   a. J = K = Clock = Clear = Gnd. For SN54L78/SN74L78, Preset = 4.5 V.
   b. For SN54L73/SN74L73: J = Clear = 4.5 V, K = Gnd, and apply momentary 4.5 V, then Gnd, to Clock.
   For SN54L78/SN74L78: J = K = Clock = Preset = Gnd and Clear = 4.5 V.
   Average per flip-flop = $\frac{I_{CC\ total}}{2}$.
3. Each flip-flop is tested separately for $I_{in(1)}$

FIGURE 32



1. Each flip-flop is tested separately.
2. Test circuit shows setup for testing $\overline{Q}$. When testing Q, open all inputs and ground $\overline{Q}$.

FIGURE 33

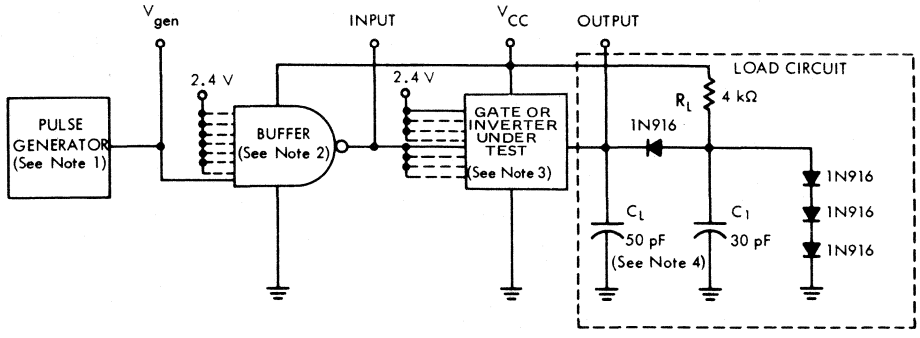


1. Each flip-flop is tested separately.

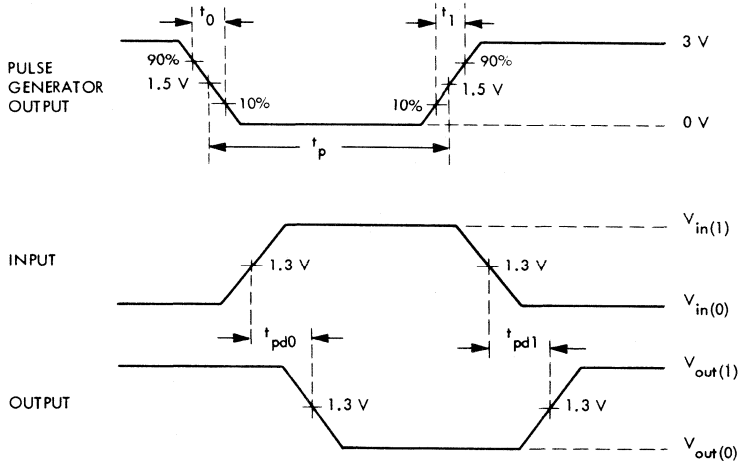
FIGURE 34

PARAMETER MEASUREMENT INFORMATION

switching characteristics



TEST CIRCUIT



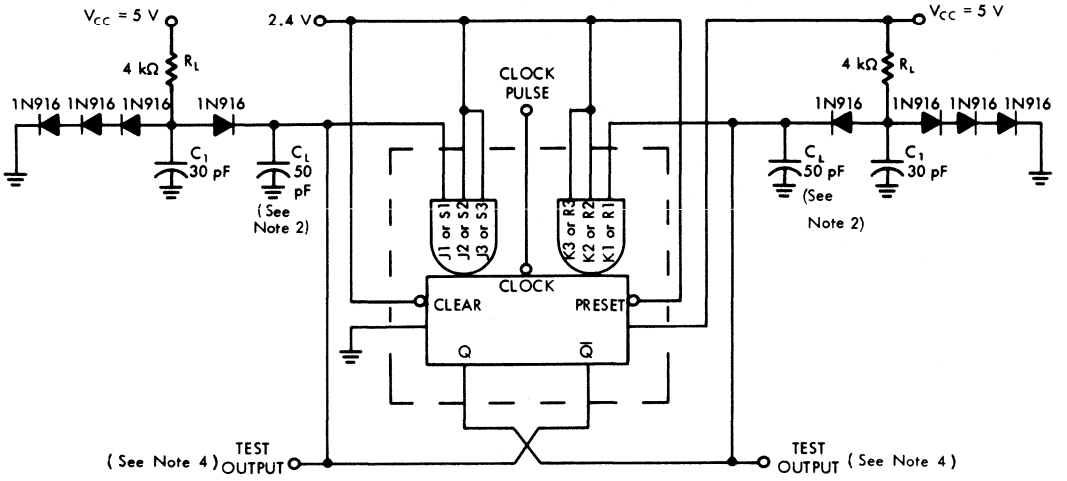
VOLTAGE WAVEFORMS

NOTES: 1. The pulse generator has the following characteristics: $t_1 = t_0 = 15$ ns, PRR = 500 kHz, duty cycle = 50%, $Z_{out} \approx 50\ \Omega$.
2. The buffer gate is a series 54L/74L gate.
3. When testing SN54L00/SN74L00, SN54L10/SN74L10, SN54L20/SN74L20, and SN54L30/SN74L30 circuits, the input signal is applied to one input and all unused inputs are at 2.4 V. When testing SN54L51/SN74L51, SN54L54/SN74L54 and SN54L55/SN74L55 circuits, the input signal is applied to one input of one AND section, 2.4 V is applied to all unused inputs of that AND section, and all inputs of all unused AND sections are grounded.
4. C_L includes probe and jig capacitance.

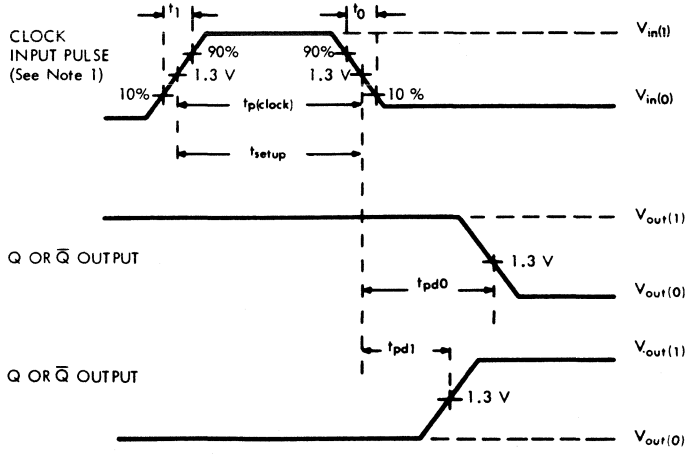
FIGURE 35 – GATE PROPAGATION DELAY TIMES

PARAMETER MEASUREMENT INFORMATION

switching characteristics (continued)



TEST CIRCUIT



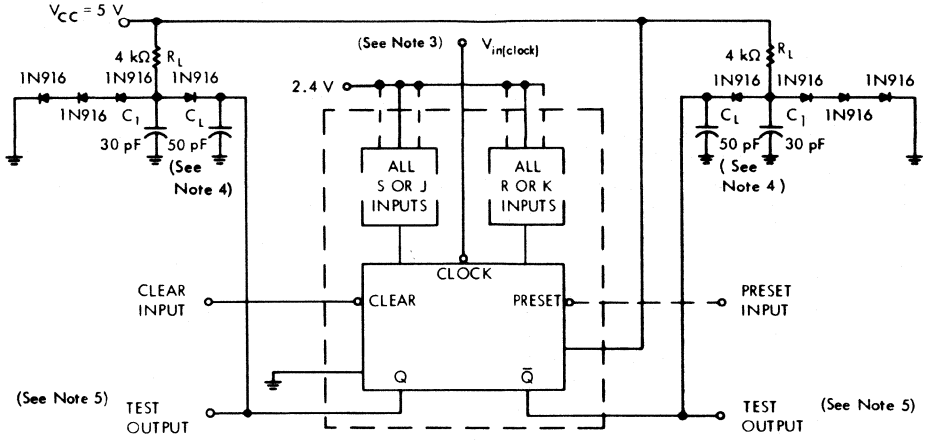
VOLTAGE WAVEFORMS

NOTES: 1. Clock input characteristics: $V_{in(0)} \leq 0.4$ V, $V_{in(1)} \geq 2.4$ V, $t_1 = t_0 = 15$ ns, $t_p \geq 200$ ns, and PRR = 500 kHz. When testing f_{clock}, vary PRR.
2. C_L includes probe and jig capacitance.
3. For SN54L73/SN74L73 and SN54L78/SN74L78, J = K = 2.4 V.
4. Load is applied only to output under test.

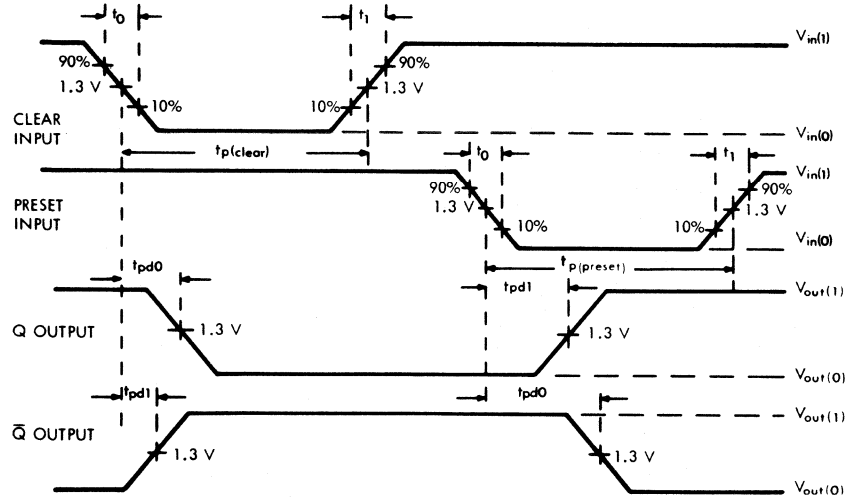
FIGURE 36—FLIP-FLOP CIRCUITS SYNCHRONOUS INPUTS SWITCHING TIMES

PARAMETER MEASUREMENT INFORMATION

switching characteristics (continued)



TEST CIRCUIT



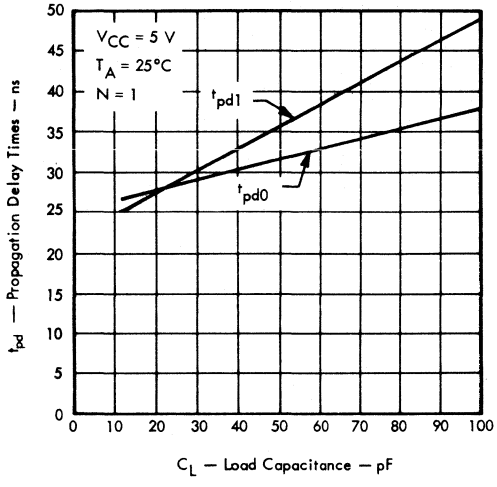
VOLTAGE WAVEFORMS

NOTES: 1. Clear or preset inputs dominate regardless of the state of clock or logic inputs.
2. Clear or preset input pulse characteristics: $V_{in(0)} \leq 0.4$ V, $V_{in(1)} \geq 2.4$ V, $t_1 = t_0 = 15$ ns, $t_{p(clear)} = t_{p(preset)} \geq 100$ ns, and PRR = 500 kHz.
3. See applicable circuit type for actual synchronous and asynchronous input configurations.
4. C_L includes probe and jig capacitance.
5. Load is applied only to output under test.

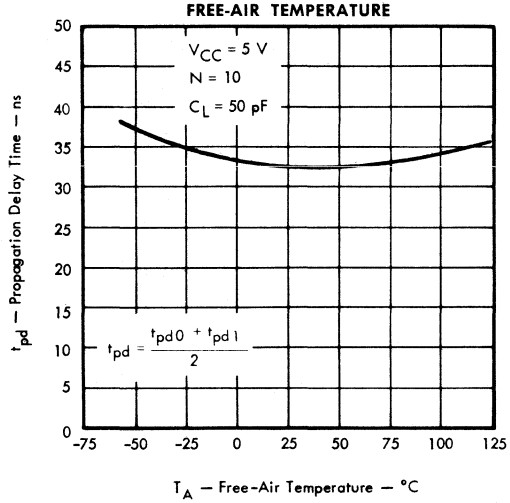
FIGURE 37 — FLIP-FLOP CIRCUITS ASYNCHRONOUS INPUTS SWITCHING TIMES

TYPICAL CHARACTERISTICS†

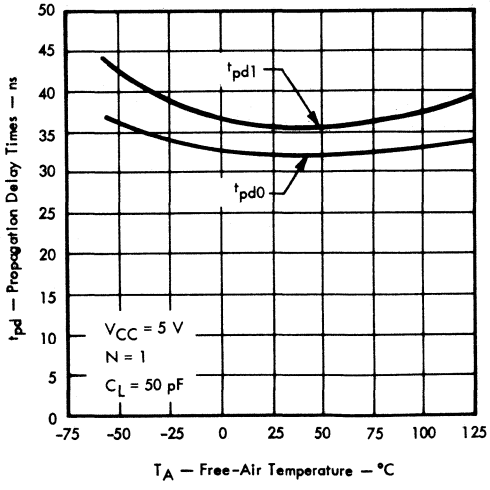
PROPAGATION DELAY TIMES vs LOAD CAPACITANCE



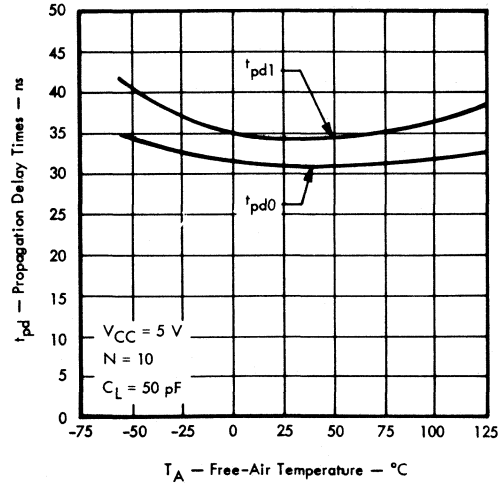
PROPAGATION DELAY TIME vs FREE-AIR TEMPERATURE



PROPAGATION DELAY TIMES vs FREE-AIR TEMPERATURE



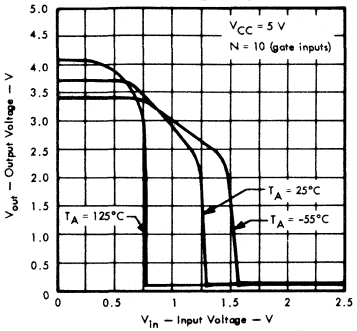
PROPAGATION DELAY TIMES vs FREE-AIR TEMPERATURE



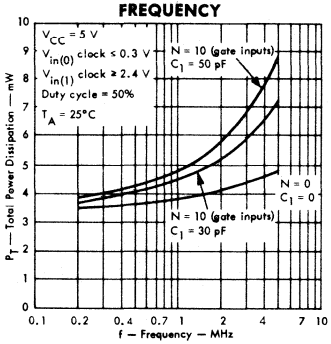
†SN54L00/SN74L00, SN54L10/SN74L10, and SN54L20/SN74L20. Data for temperatures below 0°C and above 70°C is applicable to Series 54L circuits only.

TYPICAL CHARACTERISTICS

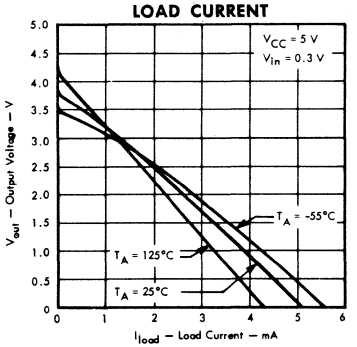
OUTPUT VOLTAGE vs INPUT VOLTAGE



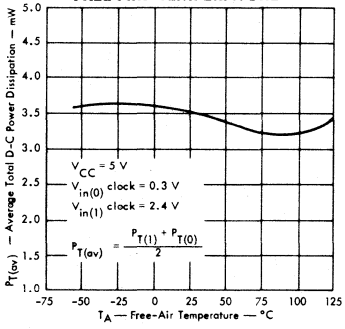
TOTAL POWER DISSIPATION‡ vs FREQUENCY



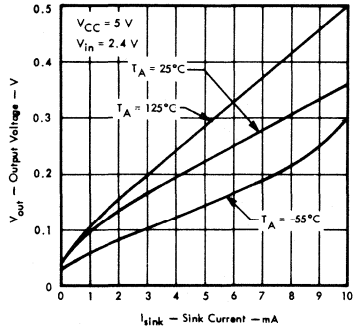
OUTPUT VOLTAGE vs LOAD CURRENT



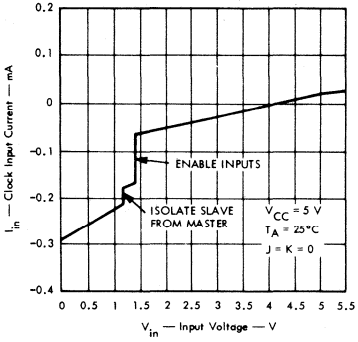
AVERAGE TOTAL D-C POWER DISSIPATION‡ § vs FREE-AIR TEMPERATURE



OUTPUT VOLTAGE vs SINK CURRENT



CLOCK INPUT CURRENT ‡ § vs INPUT VOLTAGE



† Data for temperatures below 0°C and above 70°C is applicable to Series 54L circuits only.

‡Each flip-flop.
§Value of I_{in} for SN54L78 and SN74L78 is twice the amount shown.

Eight New Low-Power MSI Integrated Circuits:

SN54L86/SN74L86
Quadruple 2-Input Exclusive-OR Gates, Page 7-31

SN54L91/SN74L91
8-Bit Shift Registers, Page 9-7

SN54L93/SN74L93
4-Bit Binary Counters, Page 8-19

SN54L95/SN74L95
4-Bit Right-Shift/Left-Shift Registers (Parallel-In, Parallel-Out), Page 9-17

CIRCUIT TYPE SN7441A
BCD-TO-DECIMAL DECODER/DRIVER

A SERIES 74 BCD-TO-DECIMAL DECODER

For Driving
Gas-Filled Cold-Cathode Indicator Tubes

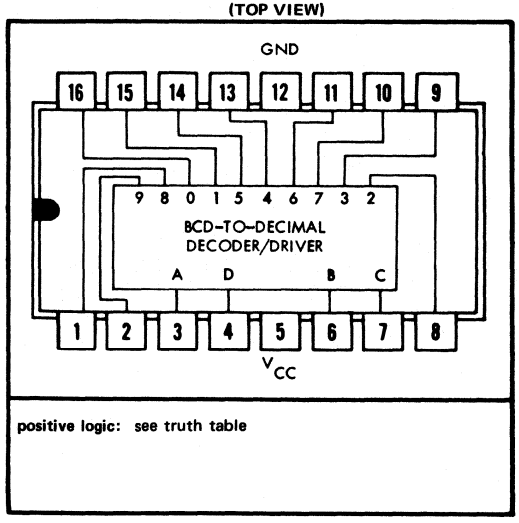
logic

TRUTH TABLE

INPUT				OUTPUT ON‡
D	C	B	A	
0	0	0	0	0
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7
1	0	0	0	8
1	0	0	1	9

‡ All other outputs are off.

J OR N DUAL-IN-LINE PACKAGE
(TOP VIEW)



positive logic: see truth table

description

The SN7441A is a monolithic, BCD-to-decimal decoder incorporating high performance output transistors designed for driving gas-filled, cold-cathode indicator tubes. The BCD-to-decimal decoder consists of familiar transistor-transistor-logic (TTL) gate circuits which select one of the ten decimal output drivers. The BCD inputs are fully compatible with Series 74 logic outputs; and, in addition, physical placement of these inputs is coincidental with the BCD output of the SN7490 decade counter. The ten high-breakdown, n-p-n transistors have a maximum reverse current of 50 μA at 55 V over the operating temperature range.

A typical application shows the SN7441A used as a gas-filled, display-indicator driver.

recommended operating conditions

Supply Voltage V_{CC} (See Note 1) . . . . . 4.75 V to 5.25 V
Maximum Voltage on any Output . . . . . 70 V

absolute maximum ratings (over operating temperature range unless otherwise noted)

Supply Voltage V_{CC} (See Note 1) . . . . . 7 V
Input Voltage, V_{in} (See Notes 1 and 2) . . . . . 5.5 V
Current into any Output (Off-State) . . . . . 2 mA
Operating Free-Air Temperature Range: . . . . . 0°C to 70°C
Storage Temperature Range . . . . . −65°C to 150°C

NOTES: 1. These voltage values are with respect to network ground terminal.
2. Input signals must be zero or positive with respect to network ground terminal.

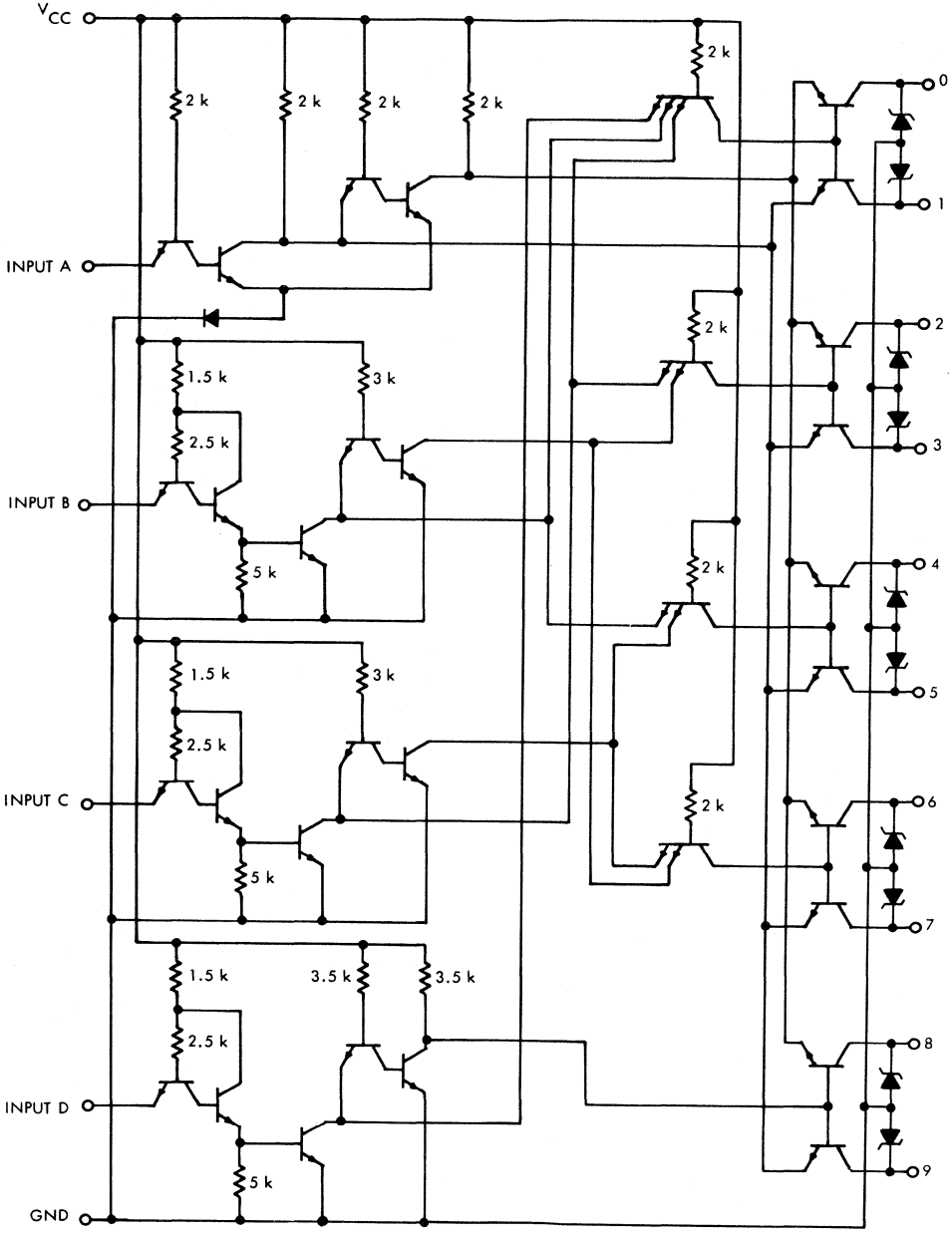
electrical characteristics, T_A = 0°C to 70°C, unless otherwise noted.

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP †	MAX	UNIT
$V_{in(1)}$	Logical 1 input voltage	1	V_{CC} = 4.75 V	2			V
$V_{in(0)}$	Logical 0 input voltage	1	V_{CC} = 4.75 V			0.8	V
V_{on}	On-state output voltage	1	V_{CC} = 4.75 V, I_{on} = 7 mA			2.5	V
I_{off}	Off-state reverse current	2	V_{CC} = 5.25 V, V_{out} = 55 V			50	μA
			V_{CC} 5.25 V, V_{out} = 70 V			2	mA
$I_{in(1)}$	Logical 1 level input current at B, C, or D	3	V_{CC} = 5.25 V, V_{in} = 2.4 V			40	μA
			V_{CC} = 5.25 V, V_{in} = 5.5 V			1	mA
$I_{in(1)}$	Logical 1 level input current at A	3	V_{CC} = 5.25 V, V_{in} = 2.4 V			80	μA
			V_{CC} = 5.25 V, V_{in} = 5.5 V			1	mA
$I_{in(0)}$	Logical 0 level input current at B, C, or D	4	V_{CC} = 5.25 V, V_{in} = 0.4 V			-1.6	mA
$I_{in(0)}$	Logical 0 level input current at A	4	V_{CC} = 5.25 V, V_{in} = 0.4 V			-3.2	mA
I_{CC}	Supply current	3	V_{CC} =5.25 V		21	42	mA

† This typical value is at V_{CC} = 5 V, T_A = 25°C

—SEE ORDERING INSTRUCTIONS PAGE 1-1—

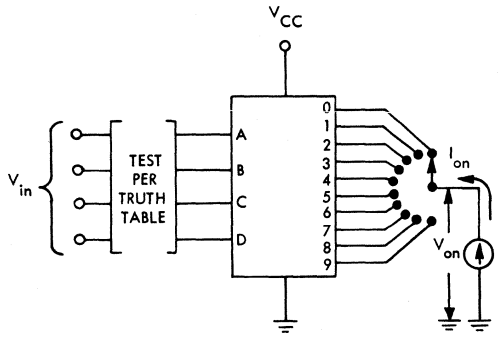
schematic



Component values shown are nominal.
All resistor values are in ohms.

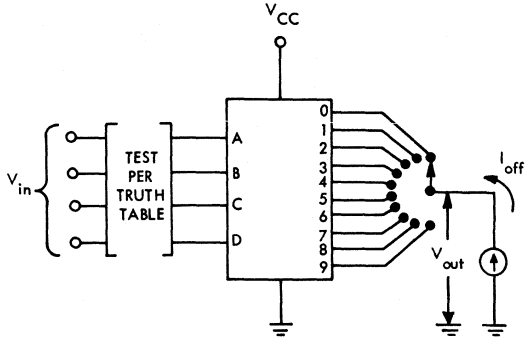
PARAMETER MEASUREMENT INFORMATION

d-c test circuits§



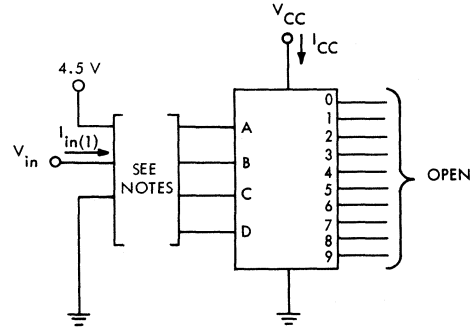
1. Each output is tested separately in the ON state.

FIGURE 1



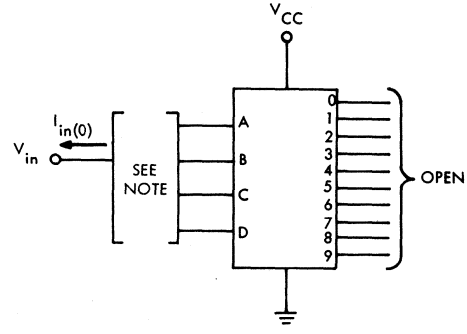
1. Each output is tested separately in the OFF state.

FIGURE 2



1. When testing $I_{in(1)}$, each input is tested separately.
2. When testing I_{CC} all outputs are open, inputs A, B, and C are at 4.5 V, and input D is grounded.

FIGURE 3



1. Each input is tested separately.

FIGURE 4

§ Arrows indicate actual direction of current flow.

typical application data

The SN7441A output transistors are capable of withstanding voltages and sinking current required to operate most types of gas-filled indicator tubes.

Clamping diodes have been incorporated in the outputs of this improved decoder/driver.

When these decoder/drivers are used in close proximity (on the same circuit board) with standard digital integrated circuits, care should be exercised to ensure that the impedance of the ground bus (including interconnections) is sufficiently low to absorb the normal energy levels resulting from switching the tube elements.

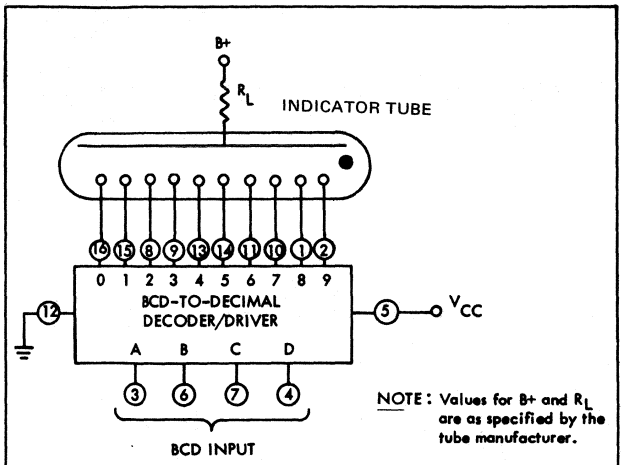
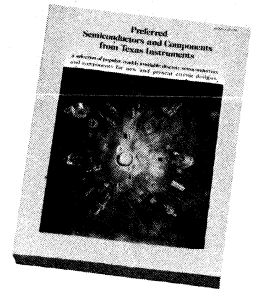


FIGURE 5

The Trend is TTL in Integrated Circuits...

... in Discretes the Trend is Preferred Semiconductors



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TEXAS INSTRUMENTS
INCORPORATED

CIRCUIT TYPES SN5442, SN5443, SN5444, SN7442, SN7443, SN7444
4-LINE-TO-10-LINE DECODERS (1-OF-10)

- BCD-to-Decimal
- Excess 3-to-Decimal
- Excess 3 Gray-to-Decimal

Also for applications as

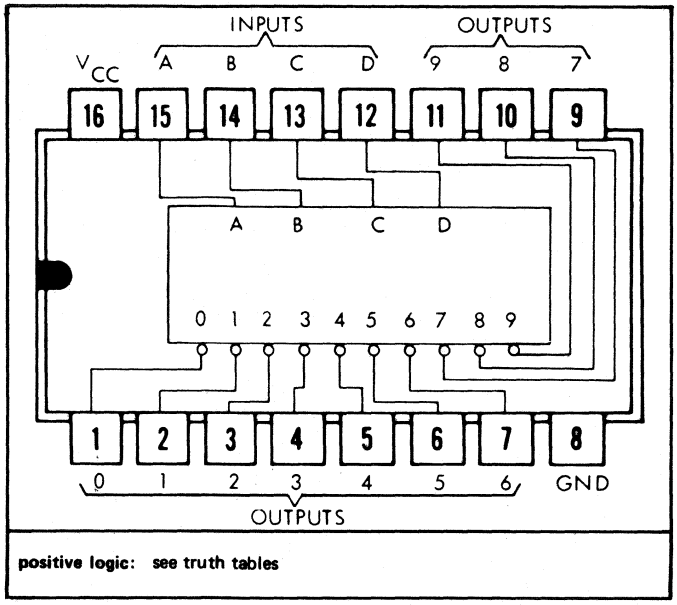
- 4-Line to 16-Line Decoders
- 3-Line to 8-Line Decoders
- featuring diode-clamped inputs

description

These monolithic decimal decoders consist of eight inverters and ten four-input NAND gates. The inverters are connected in pairs to make BCD input data available for decoding by the NAND gates. Full decoding of valid input logic ensures that all outputs remain off for all invalid input conditions.

The SN5442/SN7442 BCD-to-decimal, SN5443/SN7443 excess 3-to-decimal, and SN5444/SN7444 excess 3 gray-to-decimal decoders feature familiar transistor-transistor logic (TTL) circuits with inputs and outputs which are compatible for use with other TTL and DTL circuits. D-c noise margins are typically one volt and power dissipation is typically 140 milliwatts. Full fan-out of 10 is available at all outputs.

J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



positive logic: see truth tables

SN5442/SN7442 BCD INPUT				SN5443/SN7443 EXCESS 3 INPUT				SN5444/SN7444 EXCESS 3 GRAY INPUT				ALL TYPES DECIMAL OUTPUT									
D	C	B	A	D	C	B	A	D	C	B	A	0	1	2	3	4	5	6	7	8	9
0	0	0	0	0	0	1	1	0	0	1	0	0	1	1	1	1	1	1	1	1	1
0	0	0	1	0	1	0	0	0	1	1	0	1	0	1	1	1	1	1	1	1	1
0	0	1	0	0	1	0	1	0	1	1	1	1	1	0	1	1	1	1	1	1	1
0	0	1	1	0	1	1	0	0	1	0	1	1	1	1	0	1	1	1	1	1	1
0	1	0	0	0	1	1	1	0	1	0	0	1	1	1	1	0	1	1	1	1	1
0	1	0	1	1	0	0	0	1	1	0	0	1	1	1	1	1	0	1	1	1	1
0	1	1	0	1	0	0	1	1	1	0	1	1	1	1	1	1	1	0	1	1	1
0	1	1	1	1	0	1	0	1	1	1	1	1	1	1	1	1	1	1	0	1	1
1	0	0	0	1	0	1	1	1	1	1	0	1	1	1	1	1	1	1	1	0	1
1	0	0	1	1	1	0	0	1	0	1	0	1	1	1	1	1	1	1	1	1	0
1	0	1	0	1	1	0	1	1	0	1	1	1	1	1	1	1	1	1	1	1	1
1	0	1	1	1	1	1	0	1	0	0	1	1	1	1	1	1	1	1	1	1	1
1	1	0	0	1	1	1	1	1	0	0	0	1	1	1	1	1	1	1	1	1	1
1	1	0	1	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1
1	1	1	0	0	0	0	1	0	0	0	1	1	1	1	1	1	1	1	1	1	1
1	1	1	1	0	0	1	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1

absolute maximum ratings (over operating temperature range unless otherwise noted)

Supply Voltage V_{CC} (See Note 1) . . . . . 7 V
Input Voltage V_{in} (See Note 1) . . . . . 5.5 V
Operating Free-Air Temperature Range: SN5442, SN5443, SN5444 Circuits . . . . . −55°C to 125°C
SN7442, SN7443, SN7444 Circuits . . . . . 0°C to 70°C
Storage Temperature Range . . . . . −65°C to 150°C

recommended operating conditions (over operating temperature range)

	MIN	NOM	MAX	UNIT
Supply Voltage V_{CC} (See Note 1): SN5442, SN5443, SN5444 Circuits	4.5	5	5.5	V
SN7442, SN7443, SN7444 Circuits	4.75	5	5.25	V
Normalized Fan-Out from each Output (N)			10	

electrical characteristics (over operating temperature range unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
$V_{in(1)}$	Input voltage required to ensure logical 1 at any input terminal	1 and 2	V_{CC} = MIN		2			V
$V_{in(0)}$	Input voltage required to ensure logical 0 at any input terminal	1 and 2	V_{CC} = MIN				0.8	V
$V_{out(1)}$	Logical 1 output voltage	2	V_{CC} = MIN, $V_{in(1)}$ = 2 V, $V_{in(0)}$ = 0.8 V, I_{load} = −400 μA		2.4			V
$V_{out(0)}$	Logical 0 output voltage	1	V_{CC} = MIN, $V_{in(1)}$ = 2 V, $V_{in(0)}$ = 0.8 V, I_{sink} = 16 mA				0.4	V
$I_{in(1)}$	Logical 1 level input current (each input)	3	V_{CC} = MAX, V_{in} = 2.4 V				40	μA
			V_{CC} = MAX, V_{in} = 5.5 V				1	mA
$I_{in(0)}$	Logical 0 level input current (each input)	4	V_{CC} = MAX, V_{in} = 0.4 V				−1.6	mA
I_{OS}	Short-circuit output current§	5	V_{CC} = MAX,	SN5442, SN5443, SN5444	−20		−55	mA
				SN7442, SN7443, SN7444	−18		−55	mA
I_{CC}	Supply current	4	V_{CC} = MAX	SN5442, SN5443, SN5444		28	41	mA
				SN7442, SN7443, SN7444		28	56	mA

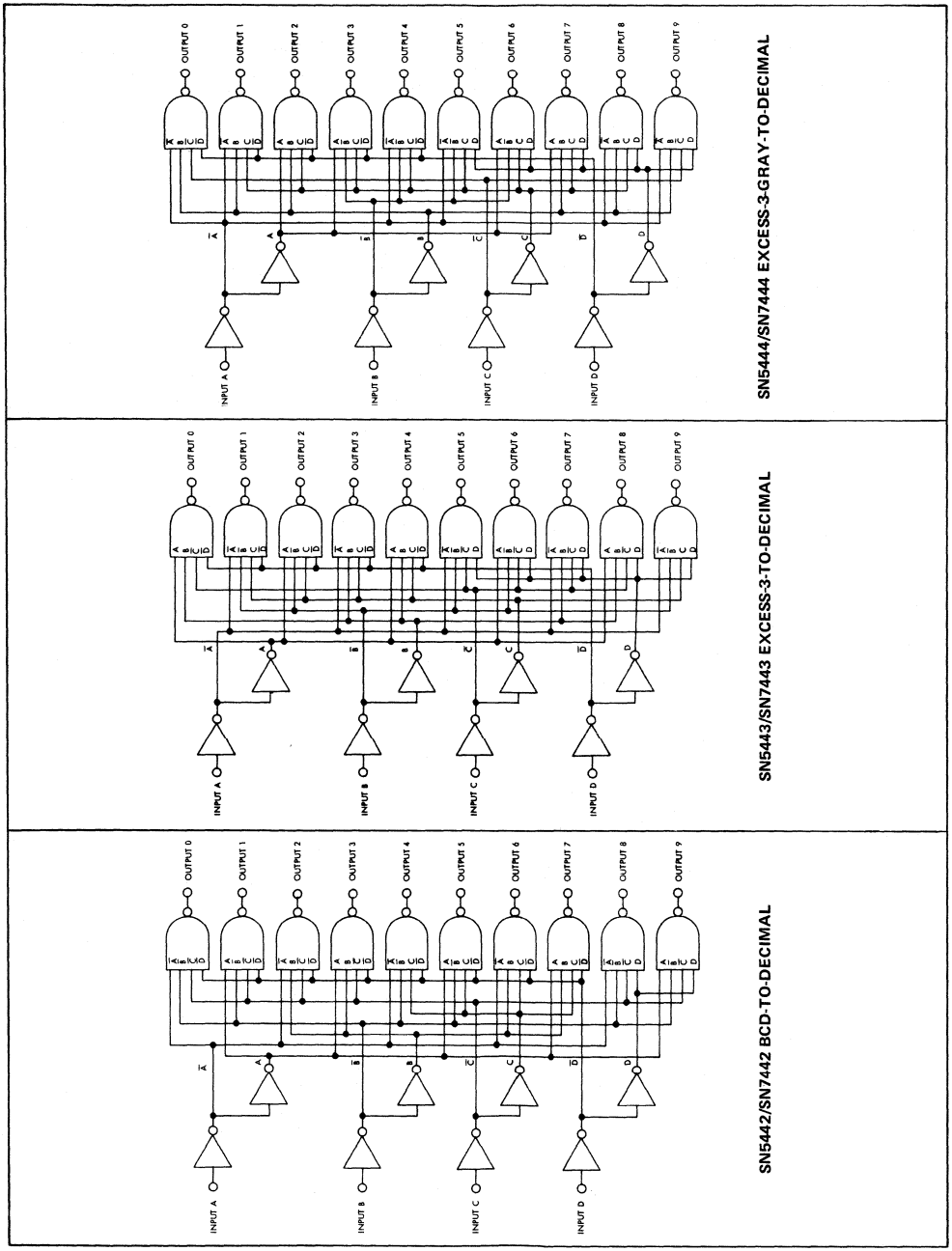
switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{pd0}	Propagation delay time to logical 0 level through two logic levels	6	C_L = 15 pF, R_L = 400 Ω	10	22	30	ns
t_{pd0}	Propagation delay time to logical 0 level through three logic levels	6	C_L = 15 pF, R_L = 400 Ω		23	35	ns
t_{pd1}	Propagation delay time to logical 1 level through two logic levels	6	C_L = 15 pF, R_L = 400 Ω	10	17	25	ns
t_{pd1}	Propagation delay time to logical 1 level through three logic levels	6	C_L = 15 pF, R_L = 400 Ω		26	35	ns

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ Not more than one output should be shorted at a time.

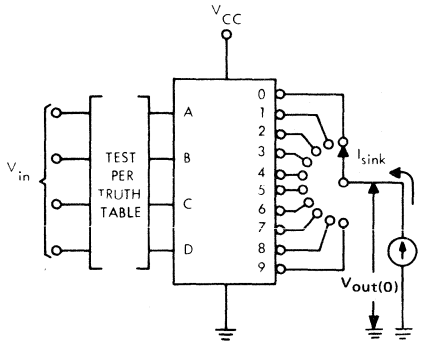
—SEE ORDERING INSTRUCTIONS PAGE 1-1—

functional block diagrams



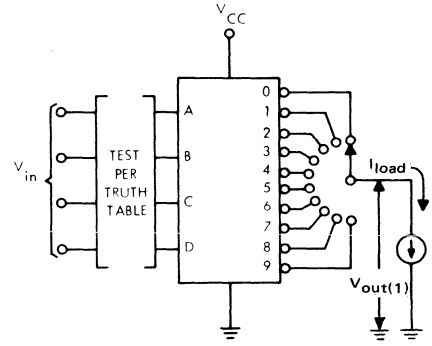
PARAMETER MEASUREMENT INFORMATION

d-c test circuits†



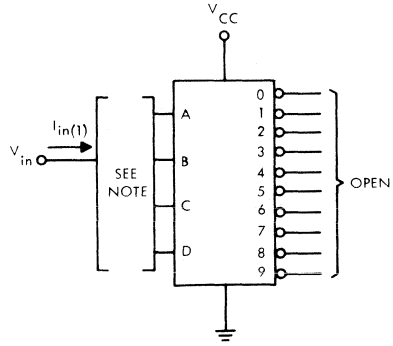
1. Each input is tested separately.

FIGURE 1



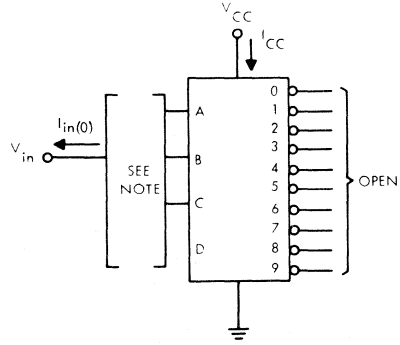
1. Each output is tested separately.

FIGURE 2



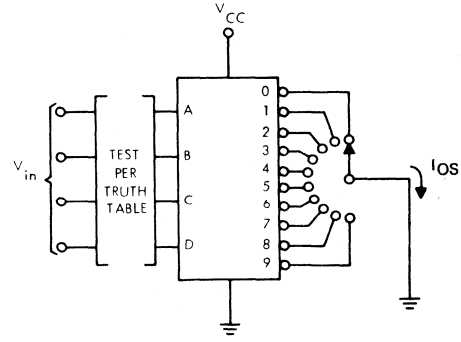
1. Each output is tested separately.

FIGURE 3



1. When testing $I_{in(0)}$ each input is tested separately.
2. When testing I_{CC} all inputs are grounded and outputs are open.

FIGURE 4



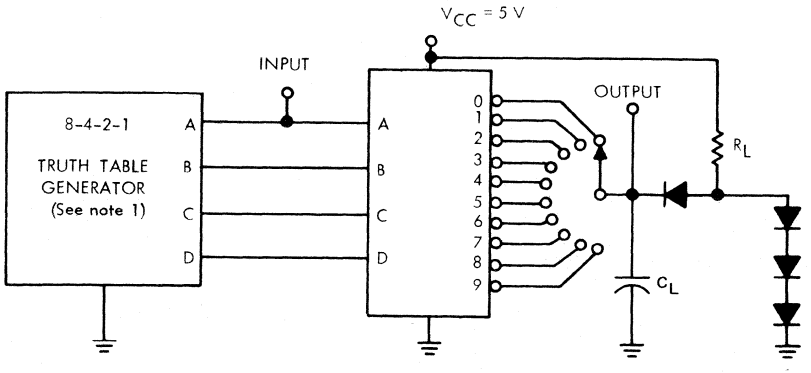
1. Each output is tested separately.

FIGURE 5

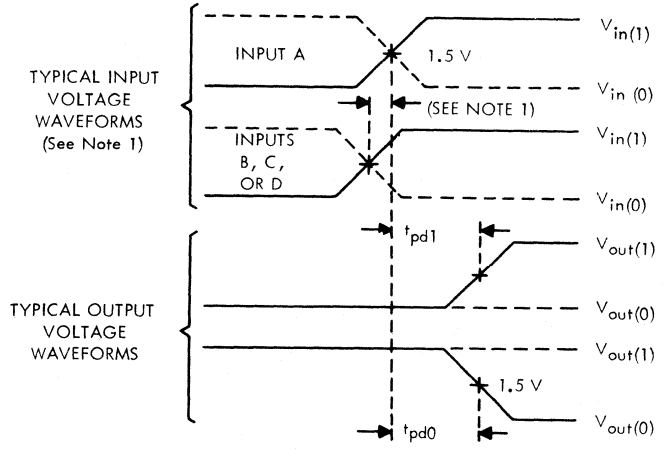
†Arrows indicate actual direction of current flow

PARAMETER MEASUREMENT INFORMATION

switching characteristics



TEST CIRCUIT



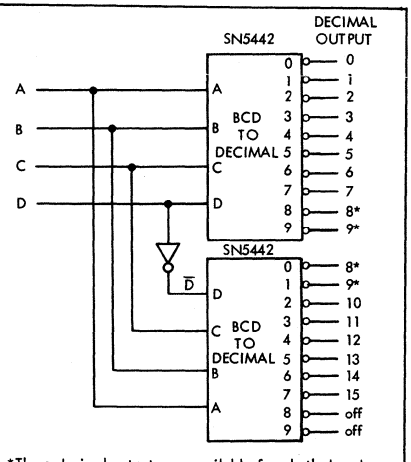
NOTES: 1. The truth table generator has the following characteristics: $V_{out(1)} \geq 2.4$ V, $V_{out(0)} \leq 0.4$ V, t_r and $t_f < 10$ ns, and PRR = 1 MHz. Input B, C, and D transitions occur simultaneously with or prior to input A transitions.
2. C_L includes probe and jig capacitance.
3. All diodes are 1N3064.

FIGURE 6—SWITCHING TIMES

TYPICAL APPLICATIONS

decoding binary-to-decimal with SN5442/SN7442,

Figure A demonstrates a method for utilizing two SN5442/SN7442 decoders to perform 4-wire to 16-wire (1-of-16) decoding. Inputs A, B, and C of the two decoders are paralleled, D is applied to one decoder, and $\overline{D}$ is applied to the other as shown in figure A. Decimal equivalents are available as indicated. Note that decimal 8 and 9 are available from both decoders.



*These decimal outputs are available from both decoders.

FIGURE A

decoding 3-wire binary-to-octal

This application demonstrates a method for decoding 3-wire binary-to-octal using the SN5442/SN7442. See figure B. The binary code ABC is applied to the ABC inputs and the D input is used as a strobe. When the strobe is taken to a logical 0 the octal data may be taken from outputs 0 through 7. Note that decimal outputs 8 and 9 are not used. See BCD truth table.

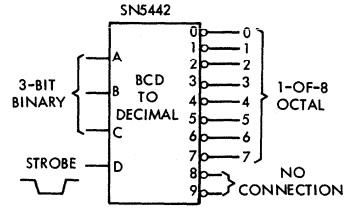


FIGURE B

This application demonstrates a method for decoding 3-wire binary-to-octal using the SN5444/SN7444. See figure C. The binary code ABC is applied to the A, B, and D inputs respectively and the C input is used as a strobe. When the strobe is taken to a logical 1 the octal data (as identified in figure C) may be taken from outputs 1 through 8. Note that outputs 0 and 9 are not used.

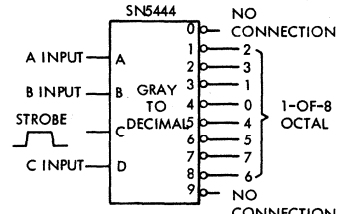


FIGURE C

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

CIRCUIT TYPES SN5445, SN54145, SN7445, SN74145
BCD-TO-DECIMAL DECODER/DRIVERS

TTL MSI LAMP, LOGIC, OR MOS DRIVERS

featuring

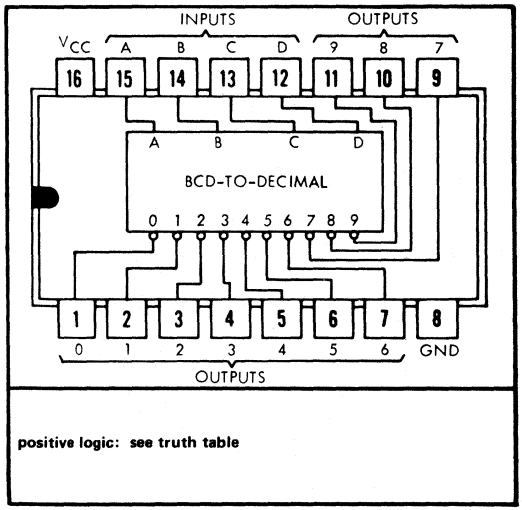
- **Full Decoding of Input Logic**
- **80 mA Sink-Current Capability**

logic

TRUTH TABLE

INPUTS				OUTPUTS								
D	C	B	A	0	1	2	3	4	5	6	7	8	9
0	0	0	0	0	1	1	1	1	1	1	1	1	1
0	0	0	1	1	0	1	1	1	1	1	1	1	1
0	0	1	0	1	1	0	1	1	1	1	1	1	1
0	0	1	1	1	1	1	0	1	1	1	1	1	1
0	1	0	0	1	1	1	1	0	1	1	1	1	1
0	1	0	1	1	1	1	1	1	0	1	1	1	1
0	1	1	0	1	1	1	1	1	1	0	1	1	1
0	1	1	1	1	1	1	1	1	1	1	0	1	1
1	0	0	0	1	1	1	1	1	1	1	1	0	1
1	0	0	1	1	1	1	1	1	1	1	1	1	0
1	0	1	0	1	1	1	1	1	1	1	1	1	1
1	0	1	1	1	1	1	1	1	1	1	1	1	1
1	1	0	0	1	1	1	1	1	1	1	1	1	1
1	1	0	1	1	1	1	1	1	1	1	1	1	1
1	1	1	0	1	1	1	1	1	1	1	1	1	1
1	1	1	1	1	1	1	1	1	1	1	1	1	1

J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



positive logic: see truth table

description

These monolithic BCD-to-decimal decoder/drivers consist of eight inverters and ten four-input NAND gates. The inverters are connected in pairs to make BCD input data available for decoding by the NAND gates. Full decoding of valid BCD input logic ensures that all outputs remain off for all invalid binary input conditions. These decoders feature TTL inputs and high-performance, n-p-n output transistors designed for use as indicator/relay drivers or as open-collector logic-circuit drivers. Each of the high-breakdown output transistors (SN5445, SN7445 = 30 volts and SN54145, SN74145 = 15 volts) will sink up to 80 milliamperes of current. Each input is one normalized Series 54/74 load. Inputs and outputs are entirely compatible for use with TTL or DTL logic circuits, and the outputs are compatible for interfacing with most MOS integrated circuits. Power dissipation is typically 215 milliwatts.

absolute maximum ratings (over operating temperature range unless otherwise noted)

Supply Voltage V_{CC} (See Note 1) . . . . . 7 V
Input Voltage, V_{in} (See Note 1) . . . . . 5.5 V
Maximum Current into each Output (See Note 2) . . . . . 1 mA
Operating Free-Air Temperature Range: SN5445, SN54145 Circuits . . . . . −55°C to 125°C
SN7445, SN74145 Circuits . . . . . 0°C to 70°C
Storage Temperature Range . . . . . −65°C to 150°C

NOTES: 1. These voltage values are with respect to network ground terminal.
2. This rating applies when the output is off.

recommended operating conditions (over operating temperature range)

	MIN	NOM	MAX	UNIT
Supply Voltage V_{CC} (See Note 1): SN5445, SN54145 Circuits	4.5	5	5.5	V
SN7445, SN74145 Circuits	4.75	5	5.25	V
Voltage on any Output (See Note 2): SN5445, SN7445 Circuits			30	V
SN54145, SN74145 Circuits			15	V

electrical characteristics (over operating temperature range unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
$V_{in(1)}$	Input voltage required to ensure logical 1 at any input terminal	1 and 2	V_{CC} = MIN		2			V
$V_{in(0)}$	Input voltage required to ensure logical 0 at any input terminal	1 and 2	V_{CC} = MIN				0.8	V
V_{on}	On-state output voltage	1	V_{CC} = MIN, I_{sink} = 80 mA			0.5	0.9	V
			V_{CC} = MIN, I_{sink} = 20 mA				0.4	V
V_{off}	Off-state output voltage (SN5445 or SN7445)	2	V_{CC} = MAX, I_{off} = 250 μA		30			V
V_{off}	Off-state output voltage (SN54145 or SN74145)	2	V_{CC} = MAX, I_{off} = 250 μA		15			V
$I_{in(1)}$	Logical 1 level input current (each input)	3	V_{CC} = MAX, V_{in} = 2.4 V				40	μA
			V_{CC} = MAX, V_{in} = 5.5 V				1	mA
$I_{in(0)}$	Logical 0 level input current (each input)	4	V_{CC} = MAX, V_{in} = 0.4 V				−1.6	mA
I_{CC}	Supply current	4	V_{CC} = MAX	SN5445, SN54145		43	62	mA
				SN7445, SN74145		43	70	mA

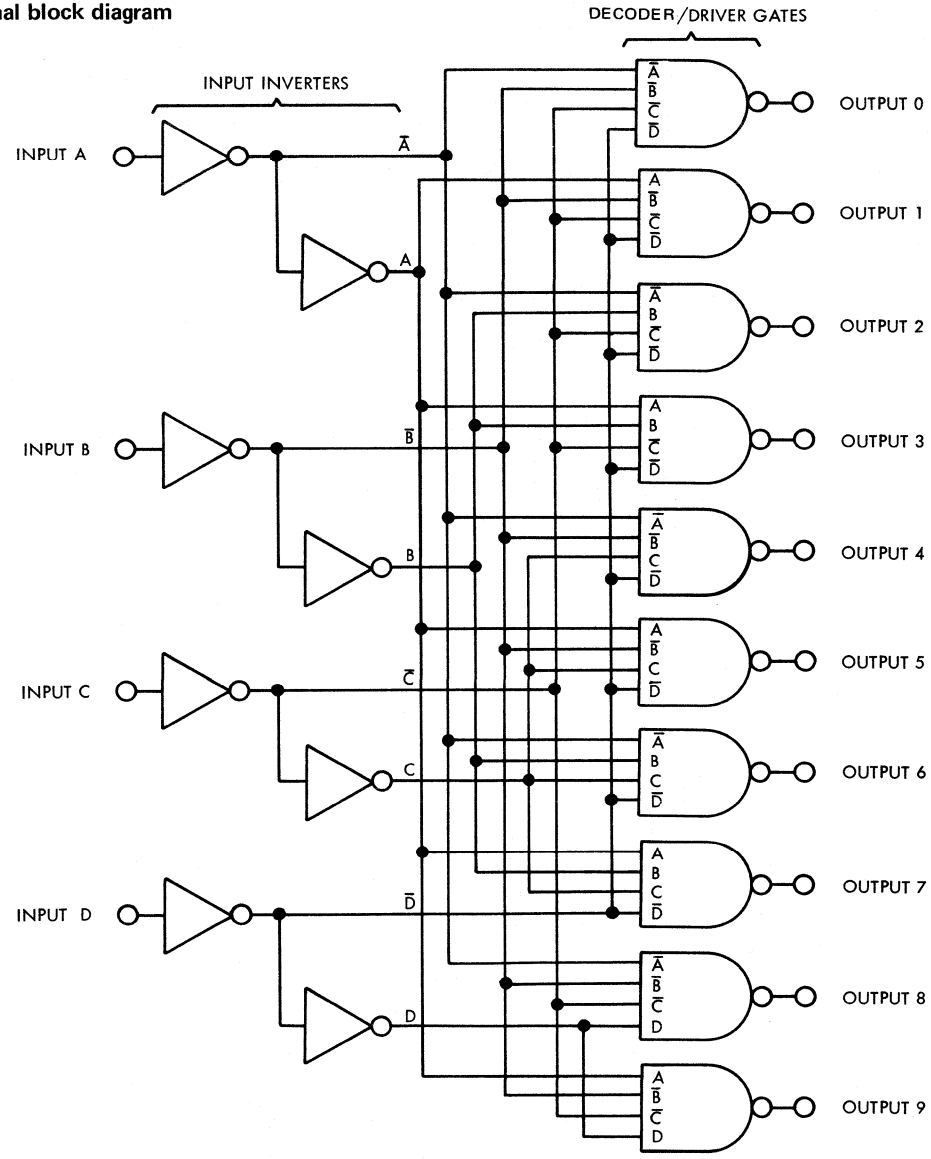
switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{pd1}	Propagation delay time to logical 1 level	5	C_L = 15 pF, R_L = 100 Ω			50	ns
t_{pd0}	Propagation delay time to logical 0 level	5	C_L = 15 pF, R_L = 100 Ω			50	ns

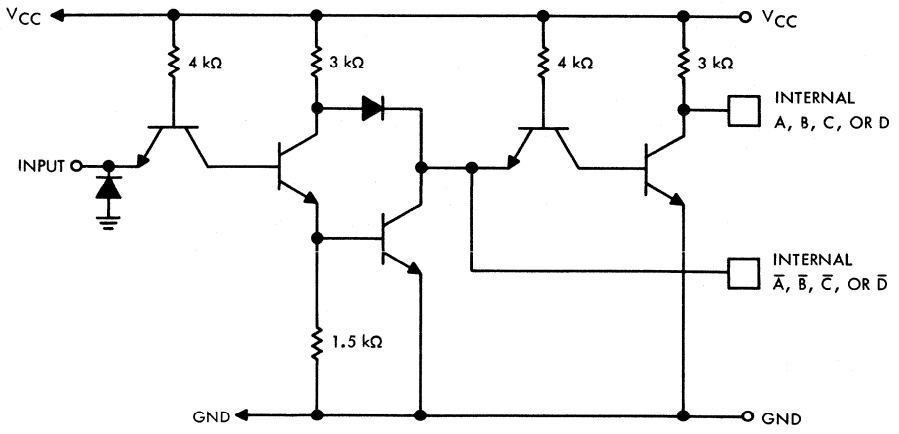
†For condition shown as MIN or MAX, use the appropriate value specified under operating conditions for the applicable circuit type.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

–SEE ORDERING INSTRUCTIONS PAGE 1-1–

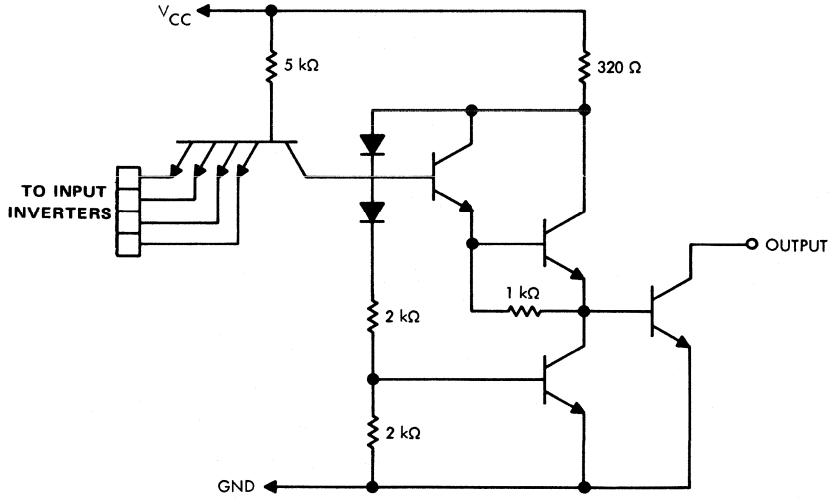
functional block diagram



schematic



EACH PAIR OF INPUT INVERTERS

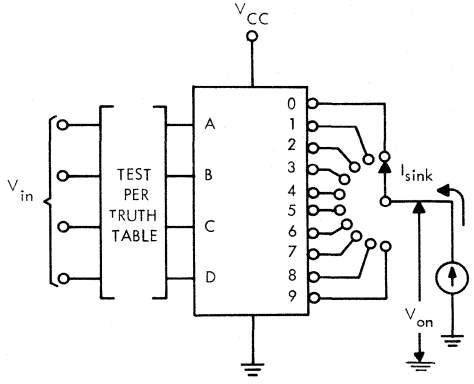


EACH DECODER/DRIVER GATE

NOTE: 1. Component values shown are nominal.

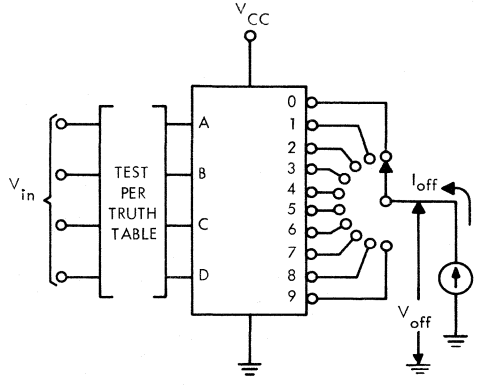
PARAMETER MEASUREMENT INFORMATION

d-c test circuits†



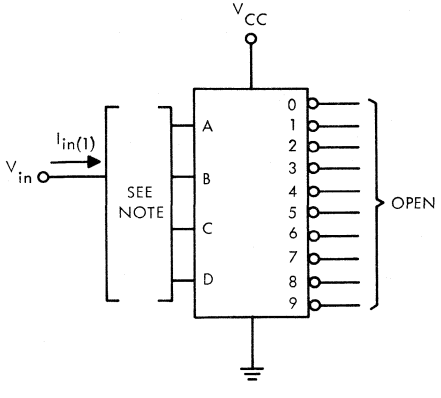
1. Each output is tested separately in the ON state.

FIGURE 1



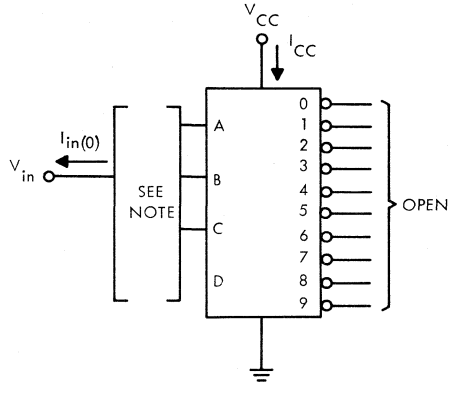
1. Each output is tested separately in the OFF state.

FIGURE 2



1. Each input is tested separately.

FIGURE 3



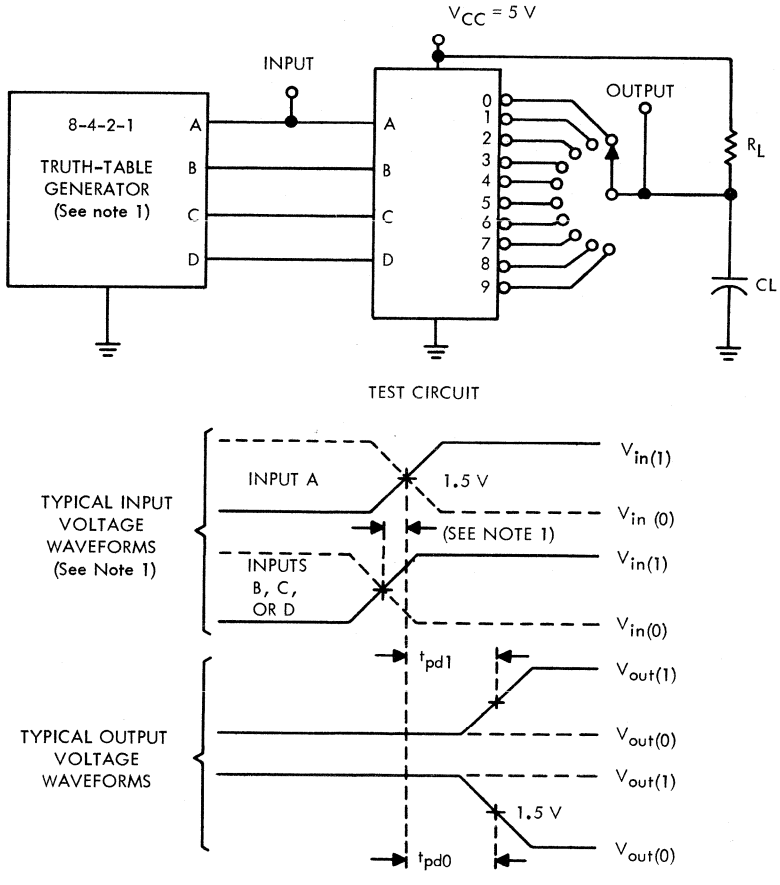
1. When testing $I_{in(0)}$ each input is tested separately.
2. When testing I_{CC} all inputs are grounded and outputs are open.

FIGURE 4

† Arrows indicate actual direction of current flow

PARAMETER MEASUREMENT INFORMATION

switching characteristics



NOTES: 1. The truth-table generator has the following characteristics: $V_{out(1)} \geq 2.4$ V, $V_{out(0)} \leq 0.4$ V, t_r and $t_f < 10$ ns, and PRR = 1 MHz. Inputs B, C, and D transitions occur simultaneously with or prior to input A transitions.
2. C_L includes probe and jig capacitance.

FIGURE 5-SWITCHING TIMES

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

CIRCUIT TYPES SN5446, SN5447, SN5448, SN5449
SN7446, SN7447, SN7448, SN7449
BCD-TO-SEVEN-SEGMENT DECODER/DRIVERS

SN5446, SN5447, SN7446 SN7447
featuring

- DIRECT DRIVE FOR INDICATORS
- OPEN-COLLECTOR OUTPUTS
- LAMP-TEST PROVISION
- LEADING/TRAILING ZERO SUPPRESSION
- CERAMIC OR PLASTIC DUAL-IN-LINE PACKAGES

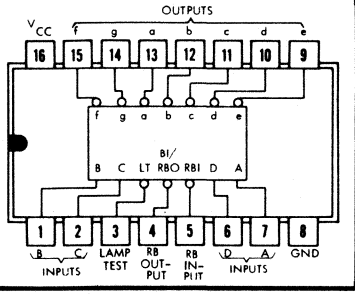
SN5448, SN7448
featuring

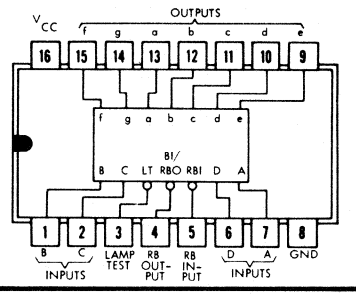
- PASSIVE PULL-UP OUTPUTS
- LAMP-TEST PROVISION
- LEADING/TRAILING ZERO SUPPRESSION
- CERAMIC OR PLASTIC DUAL-IN-LINE PACKAGES

SN5449, SN7449
featuring

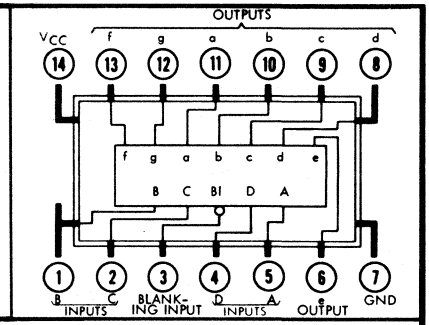
- OPEN-COLLECTOR OUTPUTS
- BLANKING INPUT
- WELDED FLAT PACKAGE

J OR N DUAL-IN-LINE PACKAGE (TOP VIEW)





S FLAT PACKAGE (TOP VIEW)



positive logic: see truth tables

ALL CIRCUIT TYPES FEATURE:

- TTL-DTL COMPATIBILITY
- FULL DECODING OF ALL 16 INPUT COMBINATIONS
- LAMP INTENSITY MODULATION CAPABILITY

description

These monolithic, TTL, BCD-to-seven-segment decoder/drivers consist of NAND gates, input buffers, and seven AND-OR-INVERT gates. Three configurations offer active-low, high-sink-current outputs (SN5446 and SN5447) for driving indicators directly; active-high, passive-pull-up outputs, (SN5448) and active-high, open-collector outputs (SN5449) for current-sourcing applications to drive logic circuits or discrete, active components. Seven NAND gates and one driver are connected in pairs to make BCD data and its complement available to the seven decoding AND-OR gates, and the remaining NAND gate and three input buffers provide lamp test, blanking input/ripple-blanking output, and ripple-blanking input for the SN5446, SN5447 and SN5448. Four NAND gates and four input buffers provide BCD data and its complement and a buffer provides blanking input for the SN5449. See functional block diagrams.

The circuits accept 4-bit binary-coded-decimal (BCD) and, depending on the state of the auxiliary inputs, decodes this data to drive a seven-segment display indicator (SN5446 and SN5447) or other components (SN5448, SN5449). The relative positive-logic output levels, as well as conditions required at the auxiliary inputs, are shown in the truth tables. Output configurations of the SN5446 and SN5447 are designed to withstand the relatively high voltages required for seven segment indicators. The SN5446 outputs will withstand 30 volts, and the SN5447 will withstand 15 volts, with a maximum reverse current of 250 microamperes. Indicator segments requiring up to 20 milli-amperes of current may be driven directly from the SN5446 or SN5447 high-performance output transistors. Segment identification with resultant displays are shown in Figure A. Display patterns for BCD input counts above 9 are unique symbols to authenticate input conditions.

PRELIMINARY DATA SHEET:
Supplementary data will be published at a later date.

description (continued)

The SN5446, SN5447, and SN5448 circuits incorporate automatic leading and/or trailing-edge zero-blanking control (RBI and RBO). Lamp test (LT) of these types may be performed at any time when the BI/RBO node is a logical 1. All types contain an overriding blanking input (BI) which can be used to control the lamp intensity or to inhibit the outputs. All inputs except the BI/RBO nodes are one normalized series 54/74 load. Inputs and outputs are entirely compatible for use with TTL or DTL logic outputs. Power dissipation is typically 265 milliwatts (SN5446, SN5447, and SN5448) or 165 milliwatts (SN5449).

The SN5446, SN5447, SN5448 and SN5449 are characterized for operation over the full military temperature range of -55°C to 125°C. The SN7446, SN7447, SN7448, and SN7449 (electrically identical to the corresponding Series 54 types) are for operation over the temperature range of 0°C to 70°C.

TRUTH TABLE SN5446, SN5447, SN7446, SN7447

	INPUTS							OUTPUTS							
DECIMAL OR FUNCTION	LT	RBI	D	C	B	A	BI/RBO	a	b	c	d	e	f	g	NOTE
0	1	1	0	0	0	0	1	0	0	0	0	0	0	1	1
1	1	X	0	0	0	1	1	1	0	0	1	1	1	1	1
2	1	X	0	0	1	0	1	0	0	1	0	0	1	0	
3	1	X	0	0	1	1	1	0	0	0	0	1	1	0	
4	1	X	0	1	0	0	1	1	0	0	1	1	0	0	
5	1	X	0	1	0	1	1	0	1	0	0	1	0	0	
6	1	X	0	1	1	0	1	1	1	0	0	0	0	0	
7	1	X	0	1	1	1	1	0	0	0	1	1	1	1	
8	1	X	1	0	0	0	1	0	0	0	0	0	0	0	
9	1	X	1	0	0	1	1	0	0	0	1	1	0	0	
10	1	X	1	0	1	0	1	1	1	1	0	0	1	0	
11	1	X	1	0	1	1	1	1	1	0	0	1	1	0	
12	1	X	1	1	0	0	1	1	0	1	1	1	0	0	
13	1	X	1	1	0	1	1	0	1	1	0	1	0	0	
14	1	X	1	1	1	0	1	1	1	1	0	0	0	0	
15	1	X	1	1	1	1	1	1	1	1	1	1	1	1	
BI	X	X	X	X	X	X	0	1	1	1	1	1	1	1	2
RBI	1	0	0	0	0	0	0	1	1	1	1	1	1	1	3
LT	0	X	X	X	X	X	1	0	0	0	0	0	0	0	4

NOTES: 1. BI/RBO is wire-OR logic serving as blanking input (BI) and/or ripple-blanking output (RBO). The blanking input must be open or held at a logical 1 when output functions 0 through 15 are desired and ripple-blanking input (RBI) must be open or at a logical 1 during the decimal 0 input. X = input may be high or low.

2. When a logical 0 is applied to the blanking input (forced condition) all segment outputs go to a logical 1 regardless of the state of any other input condition.

3. When ripple-blanking input (RBI) is at a logical 0 and A=B=C=D=logical 0, all segment outputs go to a logical 1 and the ripple-blanking output goes to a logical 0 (response condition).

4. When blanking input/ripple-blanking output is open or held at a logical 1, and a logical 0 is applied to lamp-test input, all segment outputs go to a logical 0.

TRUTH TABLE SN5448, SN7448

	INPUTS							OUTPUTS							
DECIMAL OR FUNCTION	LT	RBI	D	C	B	A	BI/RBO	a	b	c	d	e	f	g	NOTE
0	1	1	0	0	0	0	1	1	1	1	1	1	1	0	1
1	1	X	0	0	0	1	1	0	1	1	0	0	0	0	1
2	1	X	0	0	1	0	1	1	1	0	1	1	0	1	
3	1	X	0	0	1	1	1	1	1	1	1	0	0	1	
4	1	X	0	1	0	0	1	0	1	1	0	0	1	1	
5	1	X	0	1	0	1	1	1	0	1	1	0	1	1	
6	1	X	0	1	1	0	1	0	0	1	1	1	1	1	
7	1	X	0	1	1	1	1	1	1	1	0	0	0	0	
8	1	X	1	0	0	0	1	1	1	1	1	1	1	1	
9	1	X	1	0	0	1	1	1	1	1	0	0	1	1	
10	1	X	1	0	1	0	1	0	0	0	1	1	0	1	
11	1	X	1	0	1	1	1	0	0	1	1	0	0	1	
12	1	X	1	1	0	0	1	0	1	0	0	0	1	1	
13	1	X	1	1	0	1	1	1	0	0	1	0	1	1	
14	1	X	1	1	1	0	1	0	0	0	1	1	1	1	
15	1	X	1	1	1	1	1	0	0	0	0	0	0	0	
BI	X	X	X	X	X	X	0	0	0	0	0	0	0	0	2
RBI	1	0	0	0	0	0	0	0	0	0	0	0	0	0	3
LT	0	X	X	X	X	X	1	1	1	1	1	1	1	1	4

NOTES: 1. BI/RBO is wire-OR logic serving as blanking input (BI) and/or ripple-blanking output (RBO). The blanking input must be open or held at a logical 1 when output functions 0 through 15 are desired, and ripple-blanking input (RBI) must be open or at a logical 1 during the decimal 0 output. X=input may be high or low.

2. When a logical 0 is applied to the blanking input (forced condition) all segment outputs go to a logical 0 regardless of the state of any other input condition.

3. When ripple-blanking input (RBI) is at a logical 0, and A=B=C=D=logical 0, all segment outputs go to a logical 0 and the ripple-blanking output goes to a logical 0 (response condition).

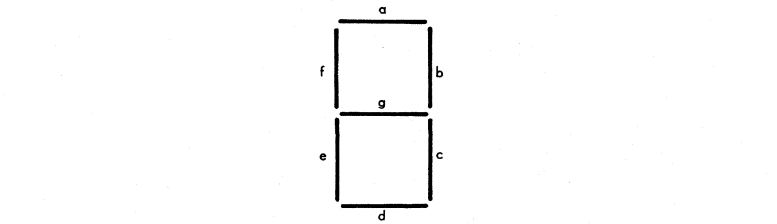
4. When blanking input/ripple-blanking output is open or held at a logical 1, and a logical 0 is applied to lamp-test input, all segment outputs go to a logical 1.

TRUTH TABLE SN5449, SN7449

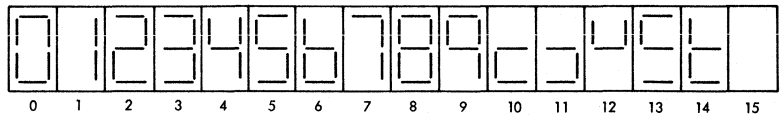
	INPUTS					OUTPUTS							
DECIMAL OR FUNCTION	D	C	B	A	BI	a	b	c	d	e	f	g	NOTE
0	0	0	0	0	1	1	1	1	1	1	1	0	1
1	0	0	0	1	1	0	1	1	0	0	0	0	
2	0	0	1	0	1	1	1	0	1	1	0	1	
3	0	0	1	1	1	1	1	1	1	0	0	1	
4	0	1	0	0	1	0	1	1	0	0	1	1	
5	0	1	0	1	1	1	0	1	1	0	1	1	
6	0	1	1	0	1	0	0	1	1	1	1	1	
7	0	1	1	1	1	1	1	1	0	0	0	0	
8	1	0	0	0	1	1	1	1	1	1	1	1	
9	1	0	0	1	1	1	1	1	0	0	1	1	
10	1	0	1	0	1	0	0	0	1	1	0	1	
11	1	0	1	1	1	0	0	1	1	0	0	1	
12	1	1	0	0	1	0	1	0	0	0	1	1	
13	1	1	0	1	1	1	0	0	1	0	1	1	
14	1	1	1	0	1	0	0	0	1	1	1	1	
15	1	1	1	1	1	0	0	0	0	0	0	0	
BI	X	X	X	X	0	0	0	0	0	0	0	0	2

NOTES: 1. The blanking input must be open or held at a logical 1 when output functions 0 through 15 are desired.

2. When a logical 0 is applied to the blanking input all segment outputs go to a logical 0 regardless of the state of any other input condition. X=input may be high or low.



SEGMENT IDENTIFICATION



NUMERICAL DESIGNATIONS — RESULTANT DISPLAYS

FIGURE A

absolute maximum ratings (over operating temperature range unless otherwise noted)

Supply Voltage V_{CC} (See Note 1) . . . . . 7 V
Input Voltage, V_{in} (See Notes 1 and 2) . . . . . 5.5 V
Current Into any Output of SN5446, SN7446, SN5447, SN7447, SN5449, SN7449 (See Note 3) . . . . . 1 mA
Operating Case Temperature Range: SN5449 Circuits . . . . . −55°C to 125°C
Operating Free-Air Temperature Range:
SN5446, SN5447, SN5448 Circuits . . . . . −55°C to 125°C
SN7446, SN7447, SN7448, SN7449 Circuits. . . . . 0°C to 70°C
Storage Temperature Range . . . . . −65°C to 150°C

NOTES: 1. These voltage values are with respect to network ground terminal.
2. Input voltage must be zero or positive with respect to network ground terminal.
3. This rating applies when the output is off.

recommended operating conditions (over operating temperature range)

	MIN	NOM	MAX	UNIT
Supply Voltage V_{CC} (See Note 1):				
SN5446, SN5447, SN5448, SN5449 Circuits	4.5	5	5.5	V
SN7446, SN7447, SN7448, SN7449 Circuits	4.75	5	5.25	V
Continuous Voltage at Outputs a through g:				
SN5446, SN7446 Circuits			30	V
SN5447, SN7447 Circuits			15	V
SN5449, SN7449 Circuits			5.5	V
Normalized Fan-Out From Outputs a through g to Series 54/74 Loads:				
SN5446, SN7446, SN5447, SN7447 Circuits			12	
SN5448, SN7448 Circuits			4	
SN5449, SN7449 Circuits			6	
Normalized Fan-Out From BI/RBO Node to Series 54/74 Loads:				
SN5446, SN7446, SN5447, SN7447, SN5448, SN7448 Circuits			5	
Output Sink Current, I_{sink}:				
SN5446, SN7446, SN5447, SN7447 Outputs a through g			20	mA
SN5448, SN7448 Outputs a through g			6.4	mA
SN5449, SN7449 Outputs a through g			10	mA
SN5446, SN7446, SN5447, SN7447, SN5448, SN7448 BI/RBO Node			8	mA

electrical characteristics (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
$V_{in(1)}$	Input voltage required to ensure logical 1 at any input	1 and 2	V_{CC}=MIN		2			V
$V_{in(0)}$	Input voltage required to ensure logical 0 at any input	1 and 2	V_{CC}=MIN				0.8	V
V_{on}	On-state output voltage at outputs a through g	1	V_{CC}=MIN, I_{sink}=20 mA			0.27	0.4	V
$V_{out(0)}$	Logical 0 output voltage at BI/RBO node	1	V_{CC}=MIN, I_{sink}=8 mA			0.3	0.4	V
V_{off}	Off-state output voltage at outputs a through g (SN5446 and SN7446 only)	2	V_{CC}=MAX, I_{off}=250 µA		30			V
V_{off}	Off-state output voltage at outputs a through g (SN5447 and SN7447 only)	2	V_{CC}=MAX, I_{off}=250 µA		15			V
$V_{out(1)}$	Logical 1 output voltage at BI/RBO node	2	V_{CC}=MIN, I_{load}=-200 µA		2.4	3.7		V
$I_{in(0)}$	Logical 0 level input current at any input except BI/RBO node	3	V_{CC}=MAX, V_{in}=0.4 V				-1.6	mA
$I_{in(0)}$	Logical 0 level input current at BI/RBO node	3	V_{CC}=MAX, V_{in}=0.4 V				-4.2	mA
$I_{in(1)}$	Logical 1 level input current at any input except BI/RBO node	4	V_{CC}=MAX, V_{in}=2.4 V				40	µA
			V_{CC}=MAX, V_{in}=5.5 V				1	mA
I_{OS}	Short-circuit output current at BI/RBO node	5	V_{CC}=MAX				-4	mA
I_{CC}	Supply current	4	V_{CC}=MAX	SN5446, SN5447		53	76	mA
				SN7446, SN7447		53	90	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{pd1}	Propagation delay time to logical 1 level from A input to any output	6	C_L = 15 pF, R_L = 280 Ω			100	ns
t_{pd0}	Propagation delay time to logical 0 level from A input to any output	6	C_L = 15 pF, R_L = 280 Ω			100	ns
t_{pd1}	Propagation delay time to logical 1 level from RBI input to any output	6	C_L = 15 pF, R_L = 280 Ω			100	ns
t_{pd0}	Propagation delay time to logical 0 level from RBI input to any output	6	C_L = 15 pF, R_L = 280 Ω			100	ns

—SEE ORDERING INSTRUCTIONS PAGE 1-1—

electrical characteristics (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS †	MIN	TYP ‡	MAX	UNIT
$V_{in(1)}$	Input voltage required to ensure logical 1 at any input	1 and 2	V_{CC} = MIN	2			V
$V_{in(0)}$	Input voltage required to ensure logical 0 at any input	1 and 2	V_{CC} = MIN			0.8	V
$V_{out(0)}$	Logical 0 output voltage at any output (SN5448, SN7448 only)	1	V_{CC} = MIN, I_{sink} = MAX		0.27	0.4	V
V_{on}	On-state output voltage at any output (SN5449, SN7449 only)	1	V_{CC} = MIN, I_{sink} = MAX		0.27	0.4	V
$V_{out(1)}$	Logical 1 level output voltage at outputs a through g (SN5448, SN7448)	2	V_{CC} = MIN, I_{load} = -400 μA	2.4	4.2		V
$V_{out(1)}$	Logical 1 level output at BI/RBO node (SN5448, SN7448 only)	2	V_{CC} = MIN, I_{load} = -200 μA	2.4	3.7		V
I_{load}	Load current available at outputs a through g (SN5448, SN7448 only)	2	V_{CC} = MIN, V_{out} = 0.85 V	-1.3	-2		mA
V_{off}	Off-state output voltage at any output (SN5449, SN7449 only)	2	V_{CC} = MAX, I_{off} = 250 μA	5.5			V
$I_{in(0)}$	Logical 0 level input current at any input (except BI/RBO node of SN5448, SN7448)	3	V_{CC} = MAX, V_{in} = 0.4 V			-1.6	mA
$I_{in(0)}$	Logical 0 level input current at BI/RBO node (SN5448, SN7448 only)	3	V_{CC} = MAX, V_{in} =0.4 V			-4.2	mA
$I_{in(1)}$	Logical 1 level input current at any input (except BI/RBO node of SN5448, SN7448)	4	V_{CC} = MAX, V_{in} = 2.4 V			40	μA
			V_{CC} = MAX, V_{in} = 5.5 V			1	mA
I_{OS}	Short-circuit output current at any output (except outputs a through g of SN5449, SN7449)	5	V_{CC} = MAX			-4	mA
I_{CC}	Supply current	4	SN5448		53	76	mA
			SN7448		53	90	mA
			SN5449		33	47	mA
			SN7449		33	56	mA

† For conditions shown as MIN or MAX use the appropriate value specified under recommended operating conditions for the applicable device type.
‡ These typical values are at V_{CC} = 5 V, T_A = 25°C

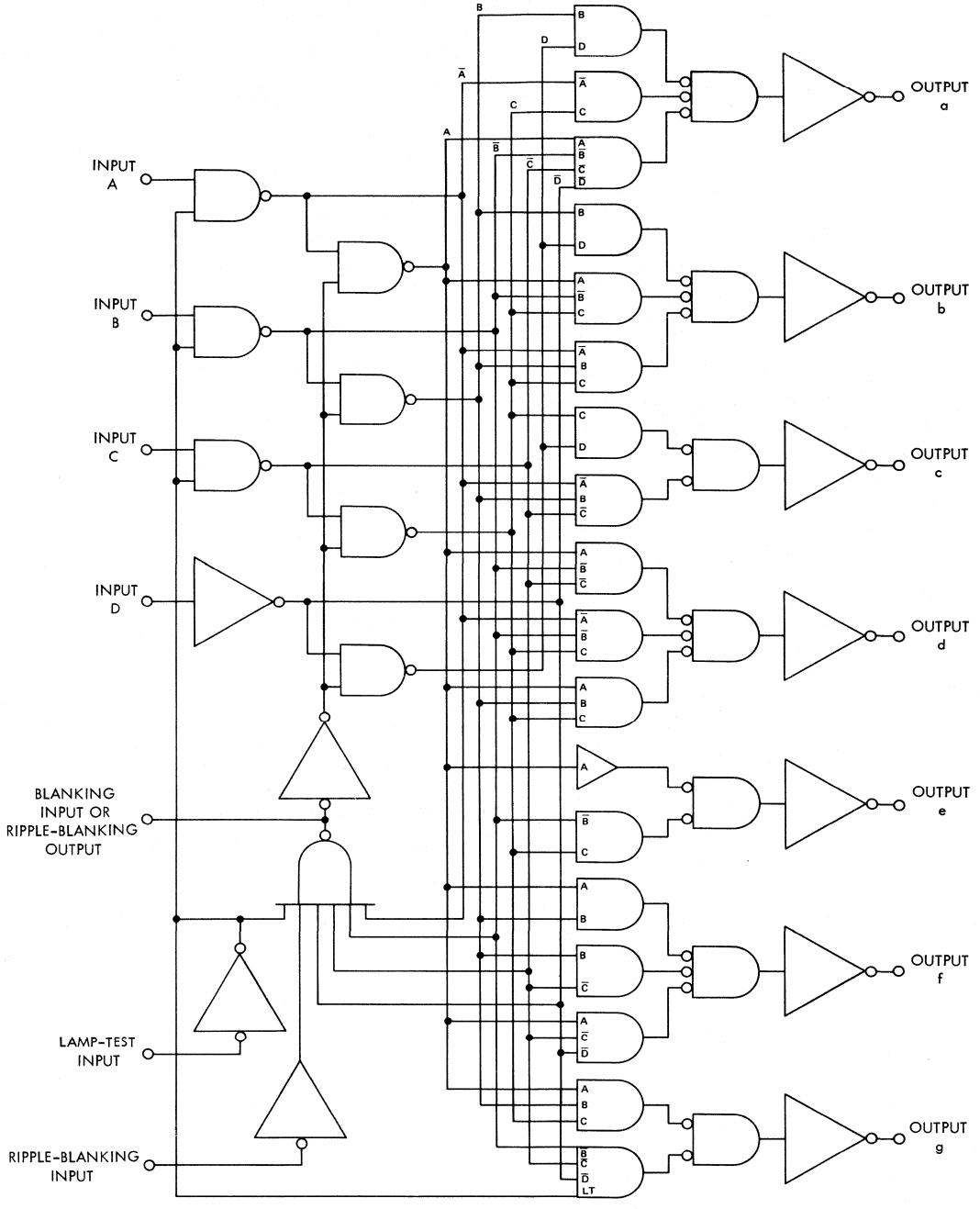
switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST FIGURE	TEST CONDITIONS §	MIN	TYP	MAX	UNIT
t_{pd1}	Propagation delay time to logical 1 level from A input to any output	6	C_L =15 pF			100	ns
t_{pd0}	Propagation delay time to logical 0 level from A input to any output	6	C_L = 15 pF			100	ns
t_{pd1}	Propagation delay time to logical 1 level from RBI input to any output	6	C_L = 15 pF			100	ns
t_{pd0}	Propagation delay time to logical 0 level from RBI input to any output	6	C_L =15 pF			100	ns

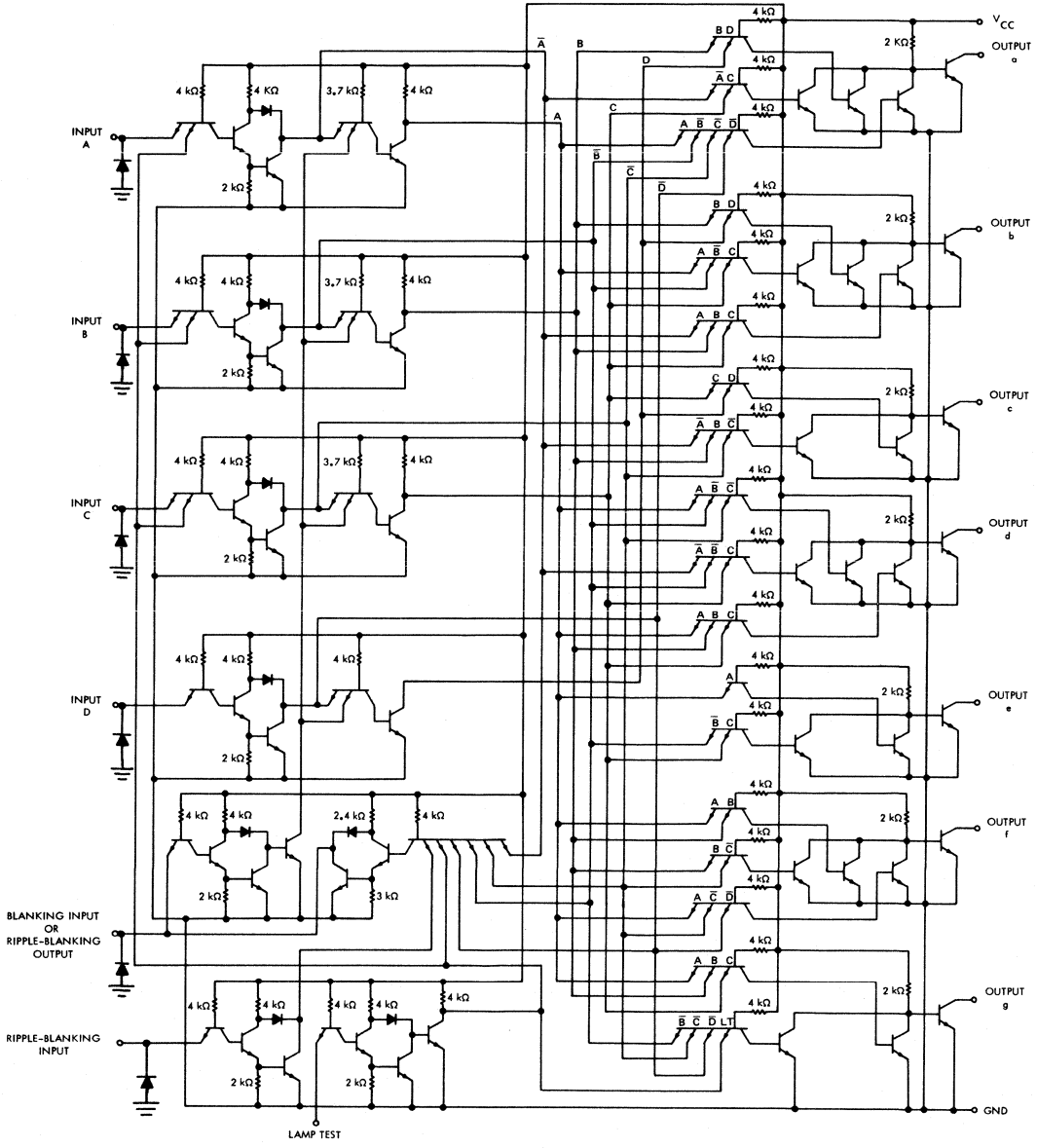
§ R_L = 1 kΩ for SN5448 and SN5449; R_L = 667 Ω for SN7448 and SN7449.

—SEE ORDERING INSTRUCTIONS PAGE 1-1—

functional block diagram

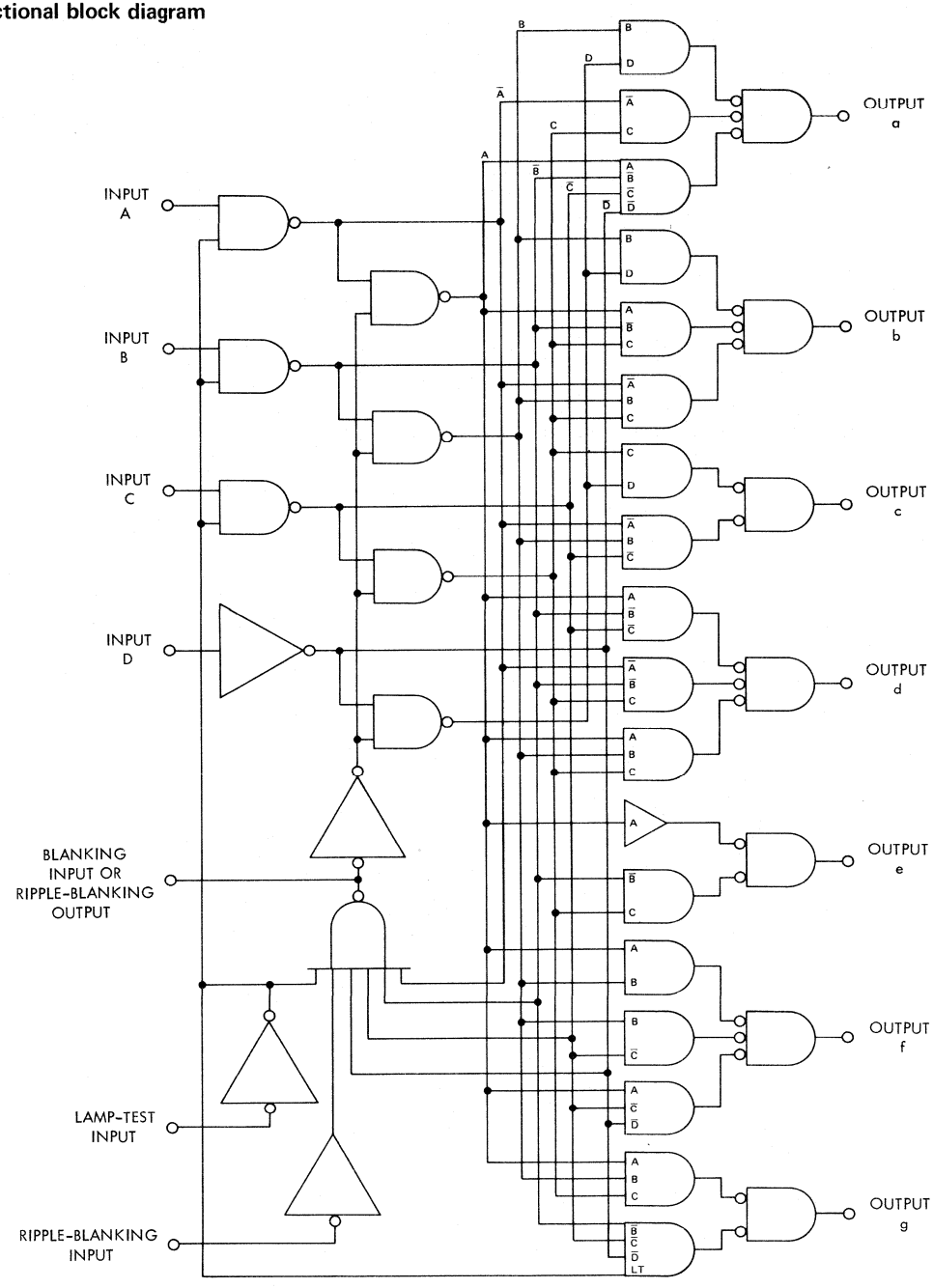


schematic diagram

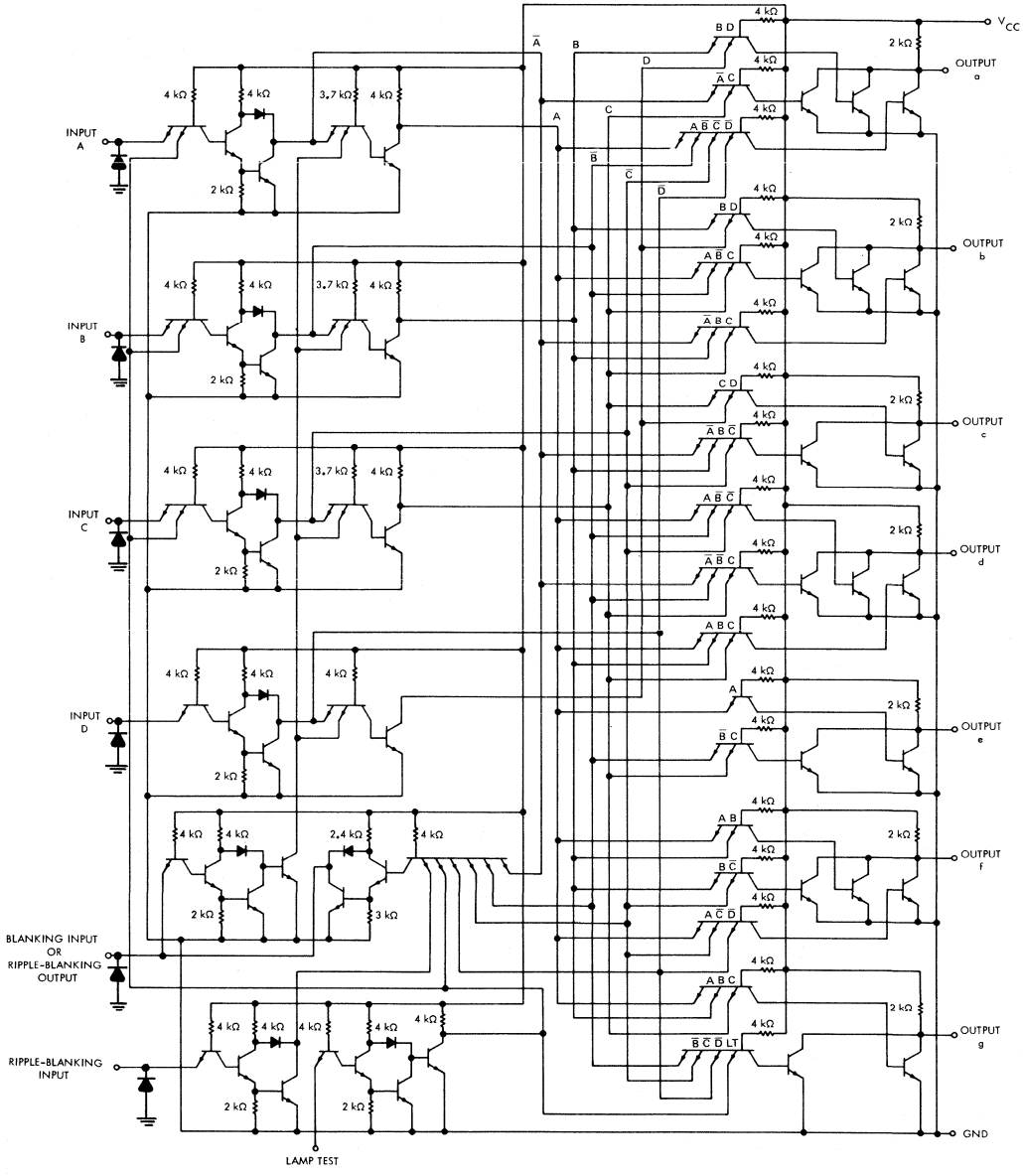


Component values shown are nominal

functional block diagram

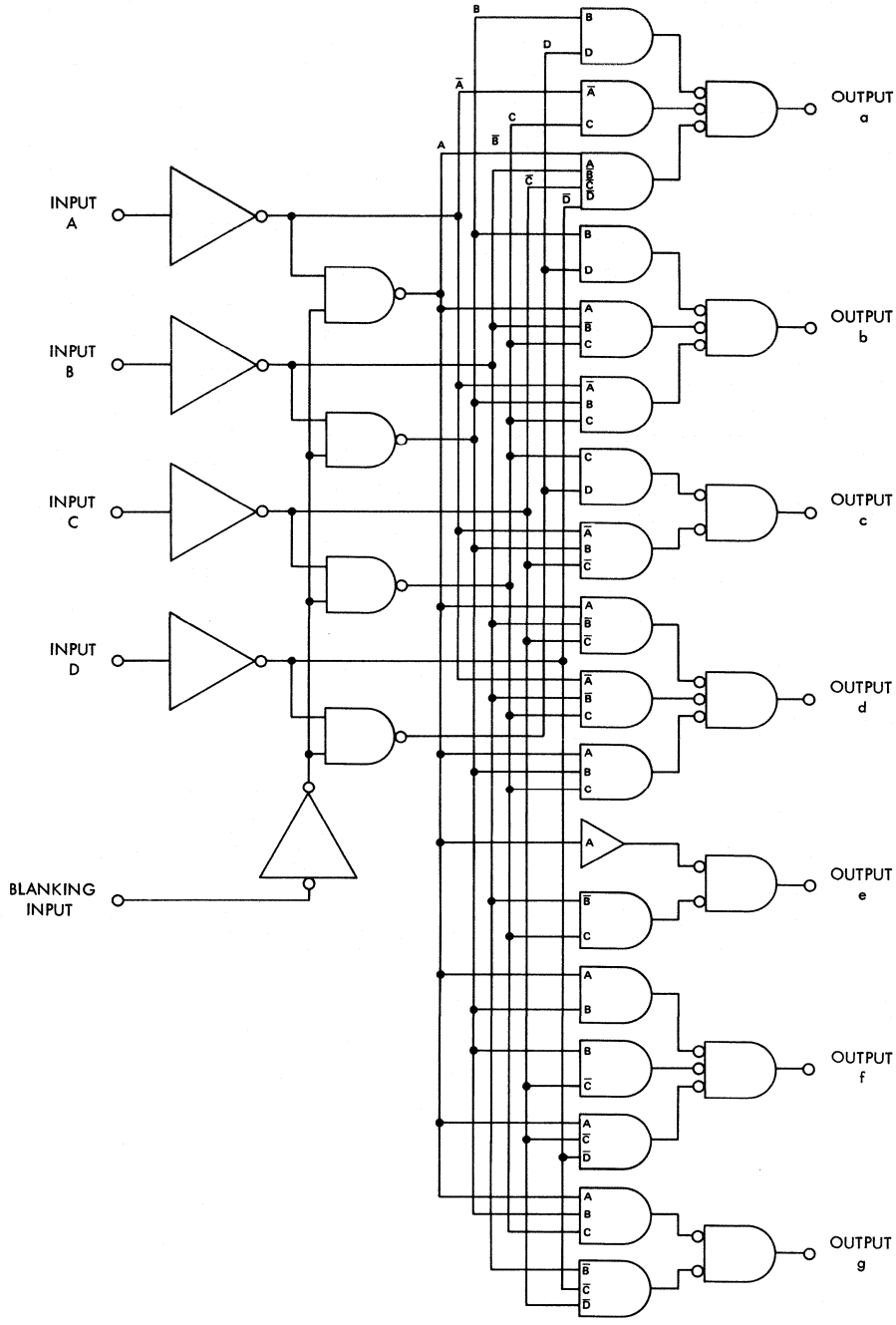


schematic diagram

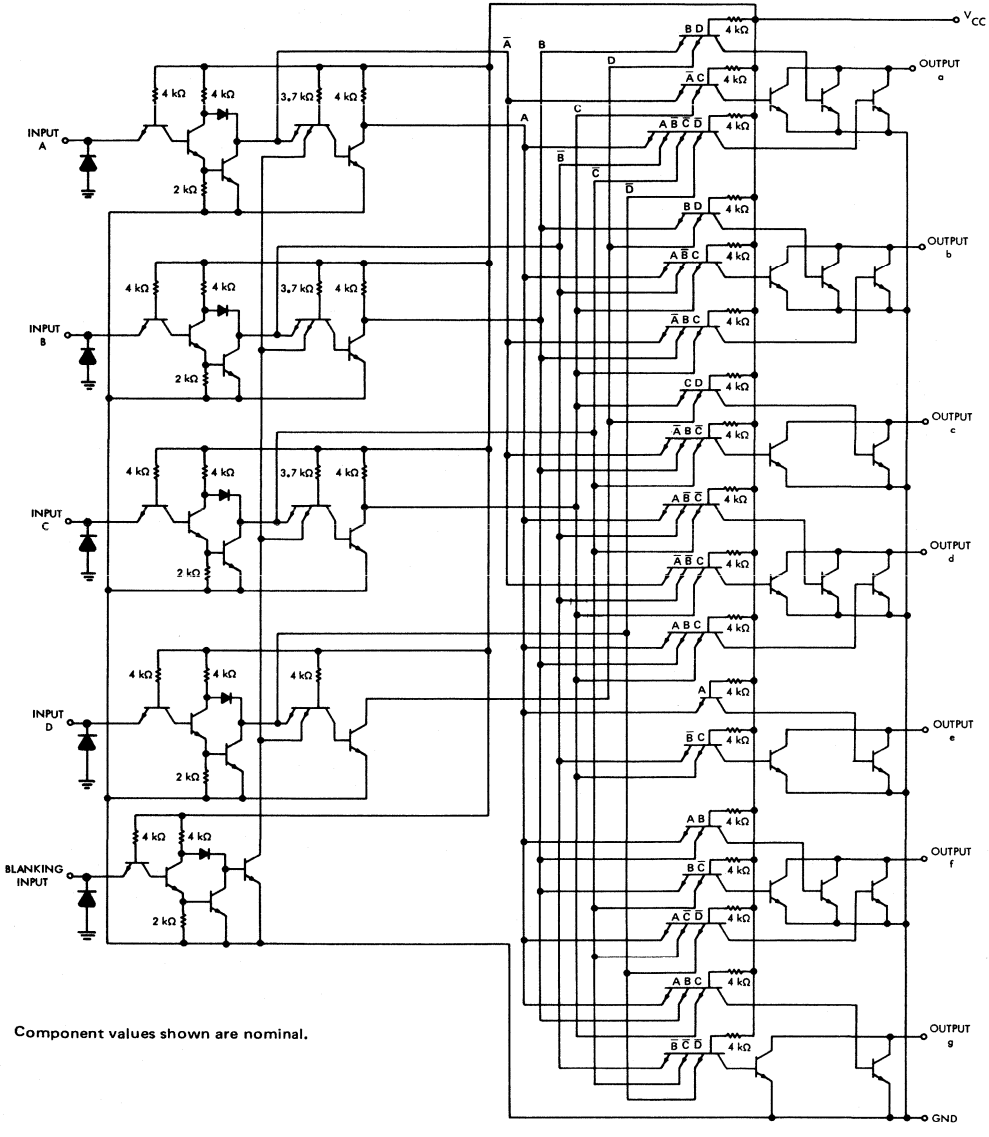


Compenent values shown are nominal

functional block diagram



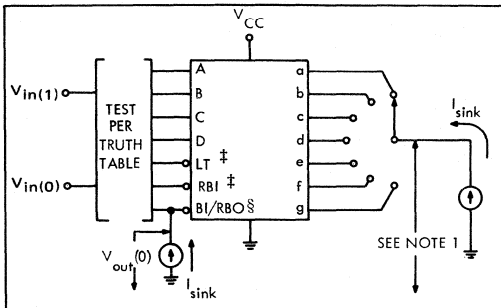
schematic diagram



Component values shown are nominal.

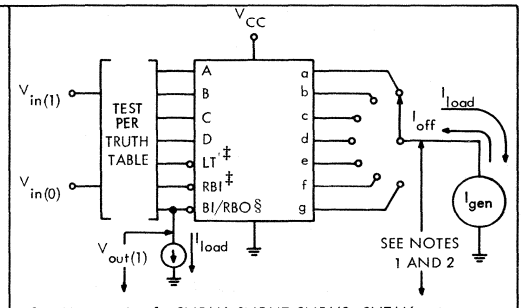
PARAMETER MEASUREMENT INFORMATION

d-c test circuits†



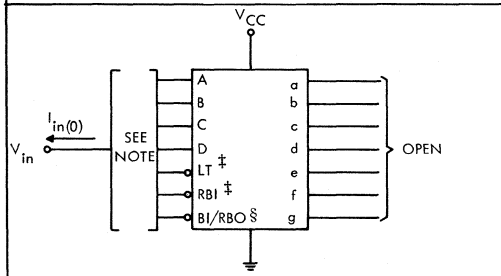
1. Measure V_{on} for SN5446, SN5447, SN5449, SN7446, SN7447, and SN7449. Measure $V_{out(0)}$ for SN5448 and SN7448.

FIGURE 1



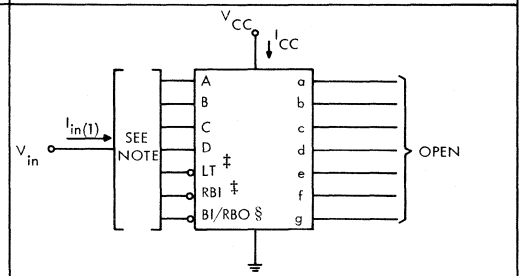
1. Measure V_{off} for SN5446, SN5447, SN5449, SN7446, SN7447, and SN7449.
2. Measure $V_{out(1)}$ for SN5448 and SN7448.

FIGURE 2



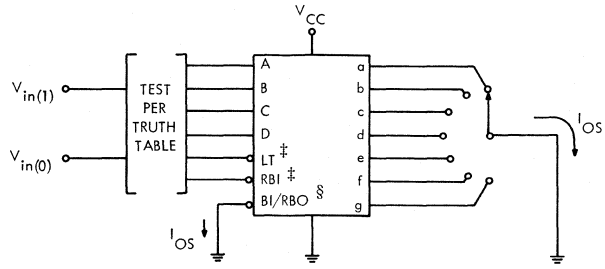
1. Each input is tested separately.

FIGURE 3



1. Each input is tested separately for $I_{in(1)}$.

FIGURE 4



1. Each output is tested separately.

FIGURE 5

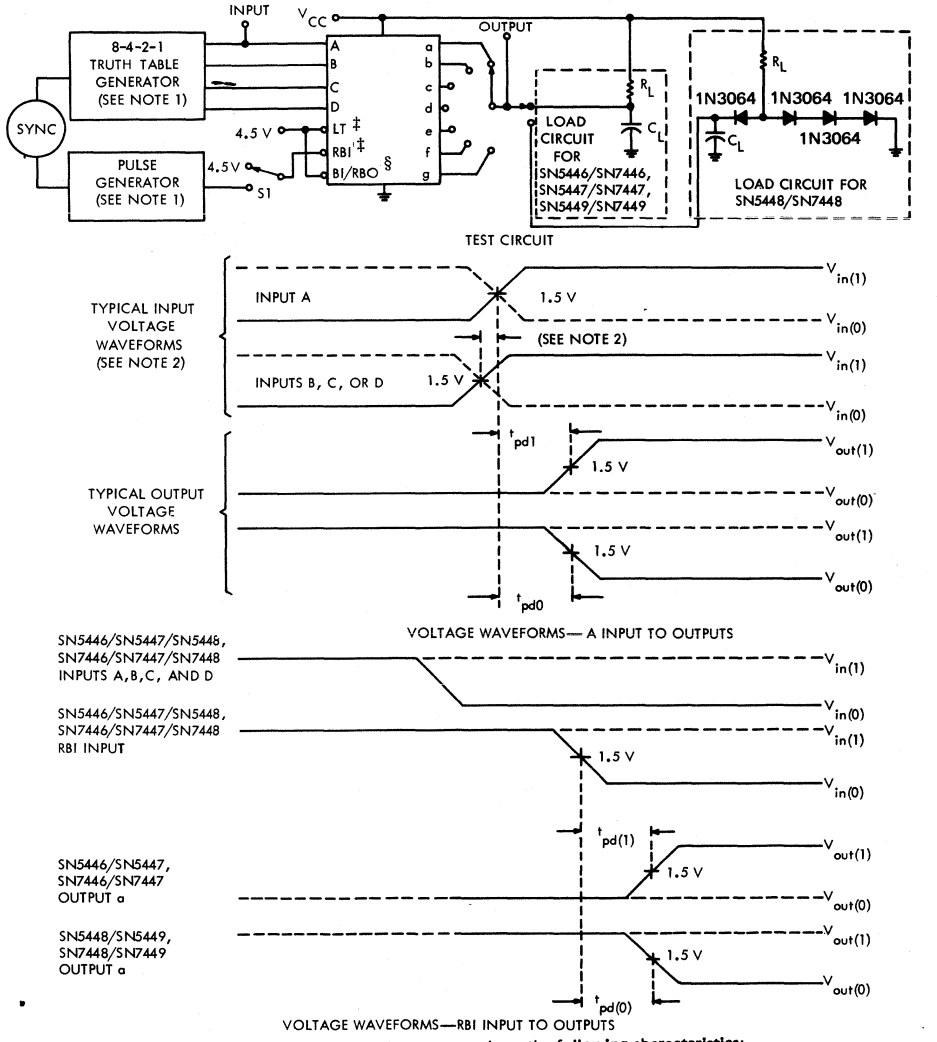
† Arrows indicate actual direction of current flow. Logic symbol used is representative for all types.

‡ Available on SN5446, SN5447, SN5448, SN7446, SN7447, and SN7448 only.

§ BI is available on all types. RBO node is available on SN5446, SN5447, SN5448, SN7446, SN7447, and SN7448 only.

PARAMETER MEASUREMENT INFORMATION

switching characteristics



NOTES: 1. The truth table generator and pulse generator have the following characteristics:
$V_{out(1)} \geqslant 2.4$ V, $V_{out(0)} \leqslant 0.4$ V, t_r and $t_f \leqslant 10$ ns, and PRR = 1 MHz.

2. Inputs B, C, and D transitions occur simultaneously with or prior to input A transitions. RBI=4.5 V.

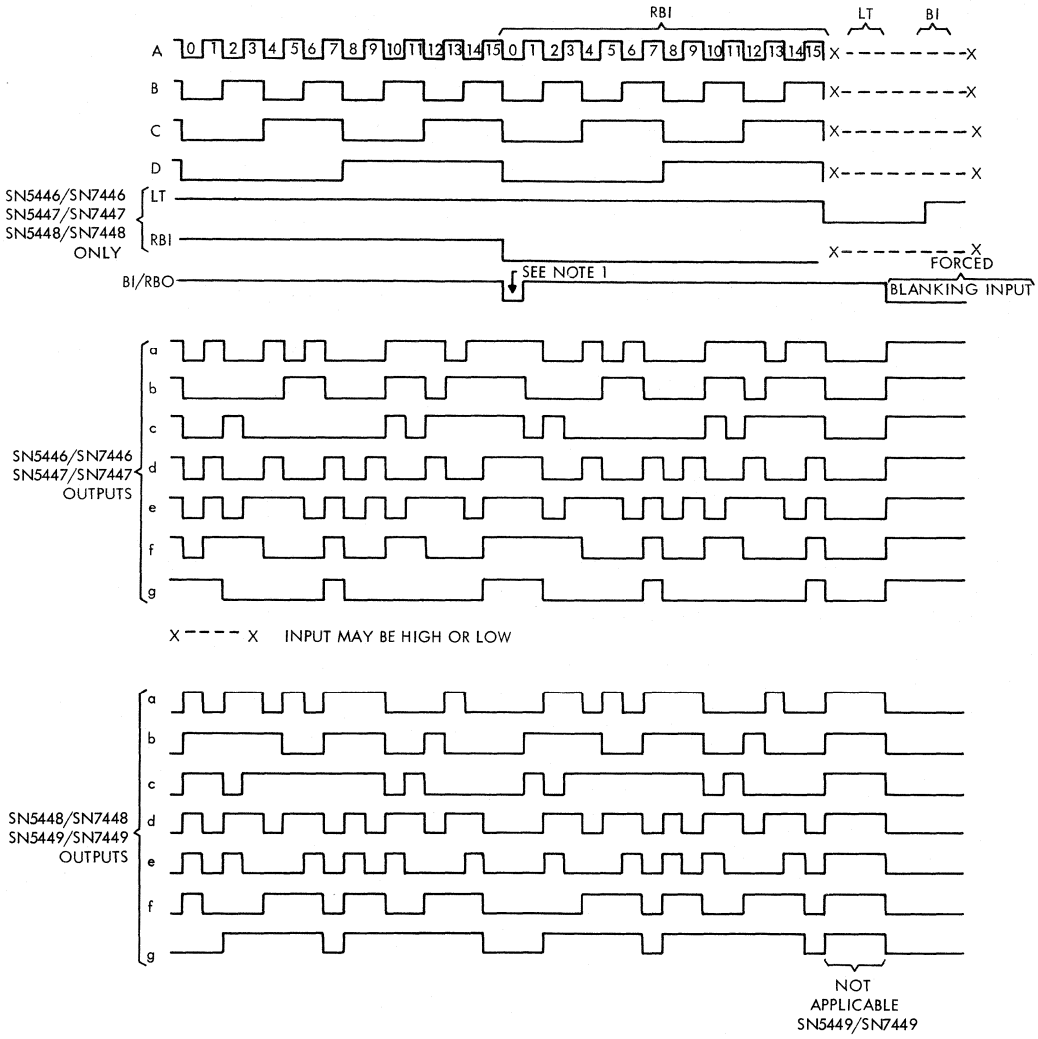
3. C_L includes probe and jig capacitance.

‡ Available on SN5446,SN5447,SN5448,SN7446,SN7447, and SN7448 only.

§ BI is available on all types. RBO node is available on SN5446,SN5447,SN5448, SN7446,SN7447, and SN7448 only.

FIGURE 6—SWITCHING TIMES

TYPICAL INPUT/OUTPUT VOLTAGE WAVEFORMS



NOTE 1: For the SN5446, SN5447, SN5448, SN7446, SN7447, and SN7448 this logical 0 represents the RBO response. For the SN5449 and SN7449 a logical 0 pulse is applied to the blanking input.

APPLICATIONS DATA

driving indicators directly (see Figure B)

This application demonstrates how the SN5446 or SN5447 may be used to drive seven-segment indicators directly. The output transistors of these two circuit types will sink up to 20 milliamperes of current; therefore, external components are not required.

Also illustrated is how the quadruple latch (SN5475) and decade counter (SN5490) may be utilized to acquire and store the numeral to be displayed. The method shown is typical of a single stage and a number of methods are possible for distributing the BCD data from the decade counter to the quadruple latch.

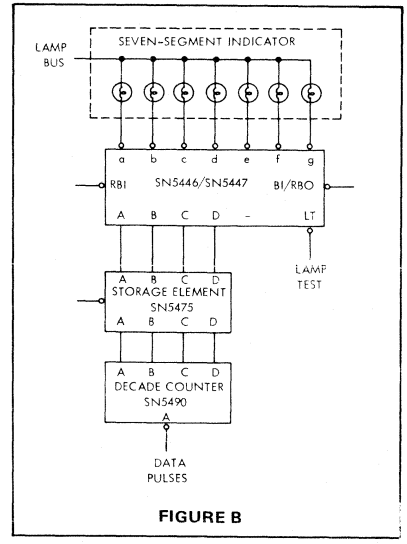


FIGURE B

n-digit display with leading-and trailing-edge blanking (see Figure C)

This application demonstrates a method for driving incandescent, seven-segment, display indicators directly from the output of the SN5446, or SN5447 decoder with provisions for leading-edge and trailing-edge zero-blanking, intensity control, and lamp test.

Leading-edge and trailing-edge zero blanking is illustrated for a six-digit mixed integer with zero indications suppressed for the two most-significant decades (MSD) of the whole number and the two least-significant decades (LSD). This scheme causes the number to be displayed in its easily identified, common form. Blanking is accomplished by grounding RBI inputs of most-significant and least-significant decades and interconnecting the BI/BRO nodes of these two decades to the ripple-blanking inputs of the adjacent decades. This improves readability by inhibiting suppression of zeros occurring on either side of the decimal point. The ripple-blanking inputs of the decades on either side of the fixed decimal point are inhibited by connecting to a 5-volt d-c source.

Intensity control is accomplished at all six of the decoder/drivers by modulating the blanking input with a nultivibrator. Best results are obtained with a modulation source in which the duty cycle can be varied. Individual drivers are required as they are wire-OR connected with the ripple-blanking functions.

As the lamp-test input is only one load, a number (up to ten) of these may be driven from a single Series 54/74 circuit.

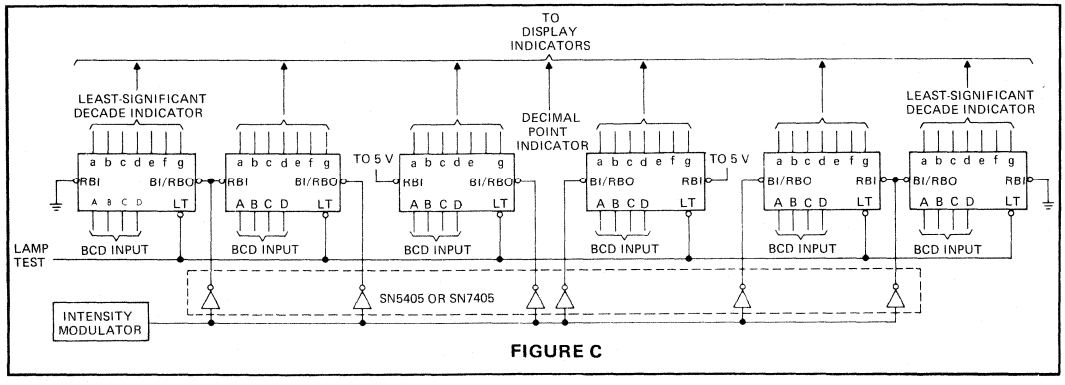


FIGURE C

APPLICATIONS DATA

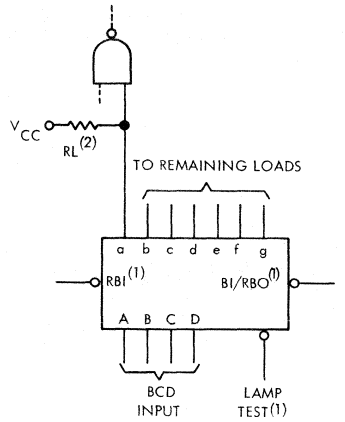
driving logic circuits (see Figure D)

These decoder/drivers may be used to drive other logic circuits. (See Figure D.) Value of the pull-up resistor (required on the open-collector outputs) may be calculated using the methods given for the SN5401 open-collector NAND gate.

driving buffer transistors (see Figures E and F)

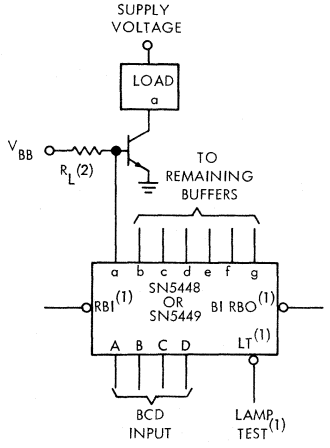
For applications requiring increased drive currents these decoder/drivers may be used with discrete drivers. A universal method of supplying base drive for a buffer transistor is illustrated in Figure E. Value of the base resistor (required on the open-collector outputs) may be calculated using the methods similar to those given for the SN5401 open-collector NAND gate. Increased base drive from the SN5448 is possible with the employment of external base resistor.

Circuitry for employing SCR's to drive electro-luminescent displays is illustrated in Figure F.



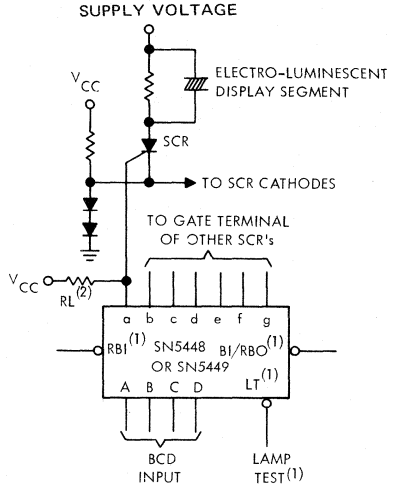
1. Available on SN5446, SN5447, SN5448, SN7446, SN7447, and SN7448 only.
2. Pull-up resistor is required with SN5446, SN5447, SN5449, SN7446, SN7447 or SN7449, and is optional with SN5448 or SN7448.

FIGURE D



1. Available on SN5448 and SN7448 only.
2. Pull-up resistor is required with SN5449 or SN7449, and is optional with SN5448 or SN7448.

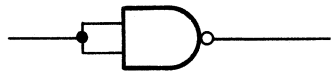
FIGURE E



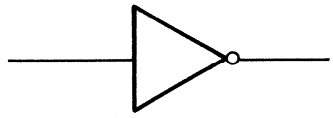
1. Available on SN5448 and SN7448 only.
2. Pull-up resistor is required with SN5449 or SN7449, and is optional with SN5448 or SN7448.

FIGURE F

Logic Diagrams Look Like This?



Replace With This!



Order:

SN5404/SN7404 Hex Inverters, Page 2-11

SN5405/SN7405 Hex Inverters, Page 2-12

SN54H04/SN74H04 High-Speed Hex Inverters, Page 3-9

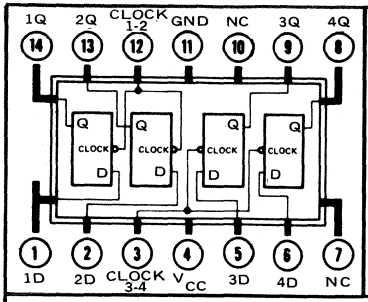
SN54H05/SN74H05 High-Speed Hex Inverters, Page 3-10

SN54L04/SN74L04 Low-Power Hex Inverters, Page 4-5

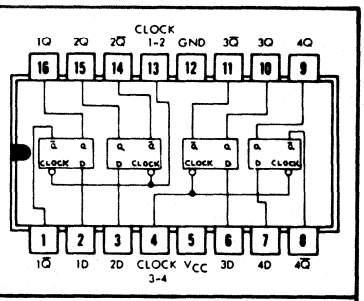
And Reduce Package Count by 50%!

CIRCUIT TYPES SN5475, SN5477, SN54100, SN7475, SN7477, SN74100
8-BIT AND 4-BIT BISTABLE LATCHES

SN5477/SN7477
S FLAT PACKAGE
(TOP VIEW)



SN5475/SN7475
J OR N DUAL-IN-LINE PACKAGE
(TOP VIEW)



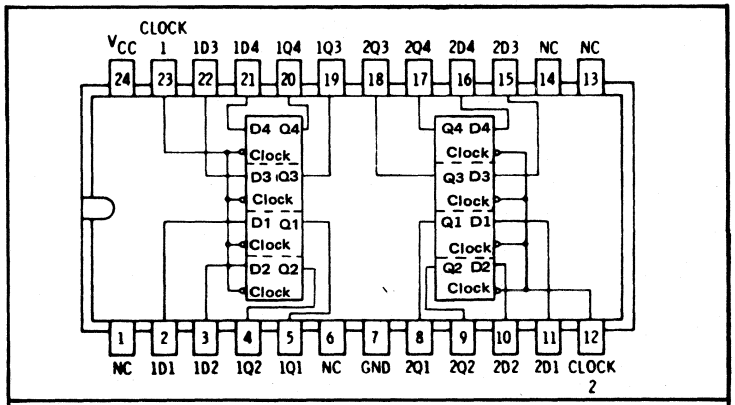
positive logic: see truth table

logic

TRUTH TABLE (Each Latch)	
t_n	t_{n+1}
D	Q
1	1
0	0

NOTES: 1. t_n = bit time before clock pulse transition.
2. t_{n+1} = bit time after clock pulse transition.
NC—No Internal Connection

SN54100/SN74100
N DUAL-IN-LINE PACKAGE (TOP VIEW)



positive logic: see truth table

description

These latches are ideally suited for use as temporary storage for binary information between processing units and input/output or indicator units. Information present at a data (D) input is transferred to the Q output when the clock is high, and the Q output will follow the data input as long as the clock remains high. When the clock goes low, the information (that was present at the data input at the time the transition occurred) is retained at the Q output until the clock is permitted to go high.

The SN5475/SN7475 features complementary Q and $\overline{Q}$ outputs from a 4-bit latch, and is available in the 16-pin packages. For higher component density applications the SN5477/SN7477 4-bit latch is available in the 14-pin flat package. The SN54100/SN74100 features two independent quadruple latches in a single 24-pin dual-in-line package.

These circuits are completely compatible with all popular TTL or DTL families. Typical power dissipation is 40 milliwatts per latch. The Series 54 circuits are characterized for operation over the full military temperature range of −55°C to 125°C and Series 74 circuits are characterized for operation from 0°C to 70°C.

absolute maximum ratings (over operating temperature range unless otherwise noted)

Supply Voltage, V_{CC} (See Note 3) . . . . . 7 V
Input Voltage, V_{in} (See Notes 3 and 4) . . . . . 5.5 V
Operating Case Temperature Range: SN5477S . . . . . −55°C to 125°C
Operating Free-Air Temperature Range: SN5475J/N, SN54100N . . . . . −55°C to 125°C
SN7475J/N, SN7477S, SN74100N . . . . . 0°C to 70°C
Storage Temperature Range . . . . . −65°C to 150°C

NOTES: 3. These voltage values are with respect to network ground terminal.
4. Input signals must be zero or positive with respect to network ground terminal.

recommended operating conditions (over operating temperature range)

	MIN	NOM	MAX	UNIT
Supply Voltage V_{CC} (See Note 3): SN5475, SN5477, SN54100	4.5	5	5.5	V
SN7475, SN7477, SN74100	4.75	5	5.25	V
Normalized Fan-Out From Outputs			10	

NOTE: 3. These voltages are with respect to network ground terminal.

electrical characteristics (over operating temperature range unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
$V_{in(1)}$	Input voltage required to ensure logical 1 level at any input terminal	1	V_{CC} = MIN		2			V
$V_{in(0)}$	Input voltage required to ensure logical 0 level at any input terminal	2	V_{CC} = MIN				0.8	V
$V_{out(1)}$	Logical 1 output voltage	1 and 2	V_{CC} = MIN, I_{load} = −400 μA		2.4			V
$V_{out(0)}$	Logical 0 output voltage	1 and 2	V_{CC} = MIN, I_{sink} = 16 mA				0.4	V
$I_{in(0)}$	Logical 0 level input current at D	3	V_{CC} = MAX, V_{in} = 0.4 V				−3.2	mA
$I_{in(0)}$	Logical 0 level input current at clock	3	V_{CC} = MAX,	SN5475, SN5477, SN7475, SN7477			−6.4	mA
				SN54100, SN74100			−12.8	mA
$I_{in(1)}$	Logical 1 level input current at D	3	V_{CC} = MAX, V_{in} = 2.4 V				80	μA
			V_{CC} = MAX, V_{in} = 5.5 V				1	mA
$I_{in(1)}$	Logical 1 level input current at clock	3	V_{CC} = MAX, V_{in} = 2.4 V,	SN5475, SN5477, SN7475, SN7477			160	μA
				SN54100, SN74100			320	μA
			V_{CC} = MAX, V_{in} = 5.5 V				1	mA
I_{OS}	Short-circuit output current§	4	V_{CC} = MAX, V_{out} = 0	SN5475, SN5477, SN54100	−20		−57	mA
				SN7475, SN7477, SN74100	−18		−57	mA
I_{CC}	Supply current	5	V_{CC} = MAX,	SN5475, SN5477		32	46	mA
				SN54100		64	92	mA
				SN7475, SN7477		32	53	mA
				SN74100		64	106	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

§ Not more than one output should be shorted at a time.

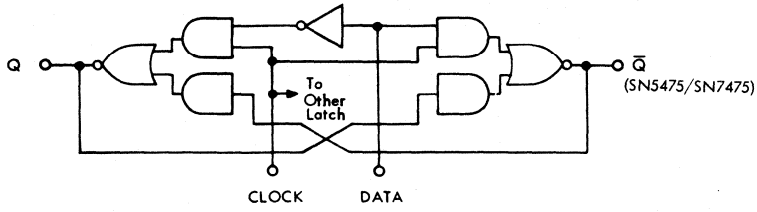
— SEE ORDERING INSTRUCTIONS PAGE 1-1 —

switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10

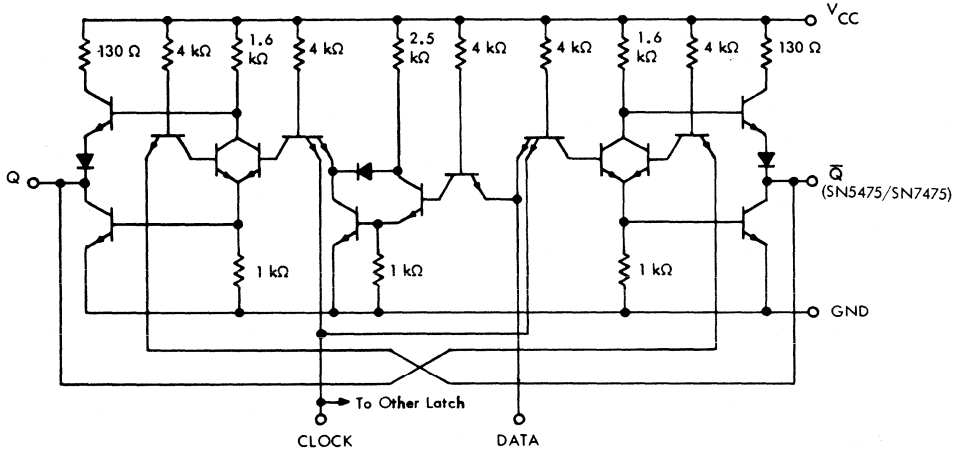
PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{setup1}	Minimum logical 1 level input setup time at D input	6	C_L = 15 pF, R_L = 400 Ω		7	20	ns
t_{setup0}	Minimum logical 0 level input setup time at D input	6	C_L = 15 pF, R_L = 400 Ω		14	20	ns
t_{hold1}	Maximum logical 1 level input hold time required at D input	6	C_L = 15 pF, R_L = 400 Ω	0	15¶		ns
t_{hold0}	Maximum logical 0 level input hold time required at D input	6	C_L = 15 pF, R_L = 400 Ω	0	6¶		ns
$t_{pd1(D-Q)}$	Propagation delay time to logical 1 level from D input to Q output	6	C_L = 15 pF, R_L = 400 Ω		16	30	ns
$t_{pd0(D-Q)}$	Propagation delay time to logical 0 level from D input to Q output	6	C_L = 15 pF, R_L = 400 Ω		14	25	ns
$t_{pd1(D-\bar{Q})}$	Propagation delay time to logical 1 level from D input to $\bar{Q}$ output (SN5475, SN7475)	6	C_L = 15 pF, R_L = 400 Ω		24	40	ns
$t_{pd0(D-\bar{Q})}$	Propagation delay time to logical 0 level from D input to $\bar{Q}$ output (SN5475, SN7475)	6	C_L = 15 pF, R_L = 400 Ω		7	15	ns
$t_{pd1(C-Q)}$	Propagation delay time to logical 1 level from clock input to Q output	6	C_L = 15 pF, R_L = 400 Ω		16	30	ns
$t_{pd0(C-Q)}$	Propagation delay time to logical 0 level from clock input to Q output	6	C_L = 15 pF, R_L = 400 Ω		7	15	ns
$t_{pd1(C-\bar{Q})}$	Propagation delay time to logical 1 level from clock input to $\bar{Q}$ output (SN5475, SN7475)	6	C_L = 15 pF, R_L = 400 Ω		16	30	ns
$t_{pd0(C-\bar{Q})}$	Propagation delay time to logical 0 level from clock input to $\bar{Q}$ output (SN5475, SN7475)	6	C_L = 15 pF, R_L = 400 Ω		7	15	ns

¶ These typical times indicate that period occurring prior to the fall of clock pulse (t_0) below 1.5 V when data at the D input will still be recognized and stored.

functional block diagram (each latch)



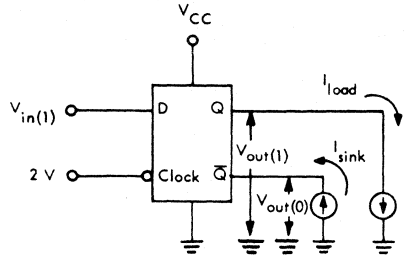
schematic (each latch)



Component values shown are nominal.

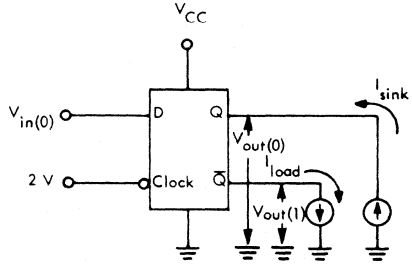
PARAMETER MEASUREMENT INFORMATION

d-c test circuits †



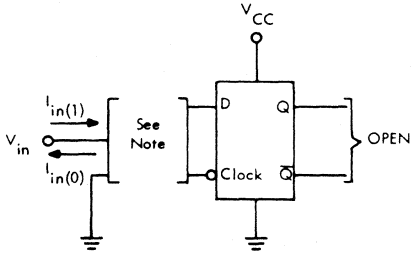
1. Each latch is tested separately.

FIGURE 1



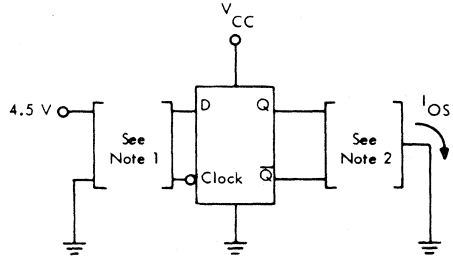
1. Each latch is tested separately.

FIGURE 2



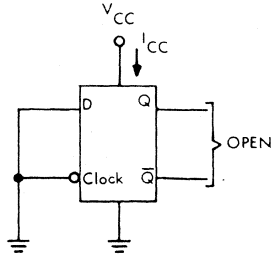
1. Each input is tested separately.
2. When testing $I_{in(1)}$ at D ground clock.
3. When testing $I_{in(1)}$ at clock ground all D inputs.

FIGURE 3



1. Input conditions are in accordance with truth table.
2. Each latch and each output is tested separately.

FIGURE 4



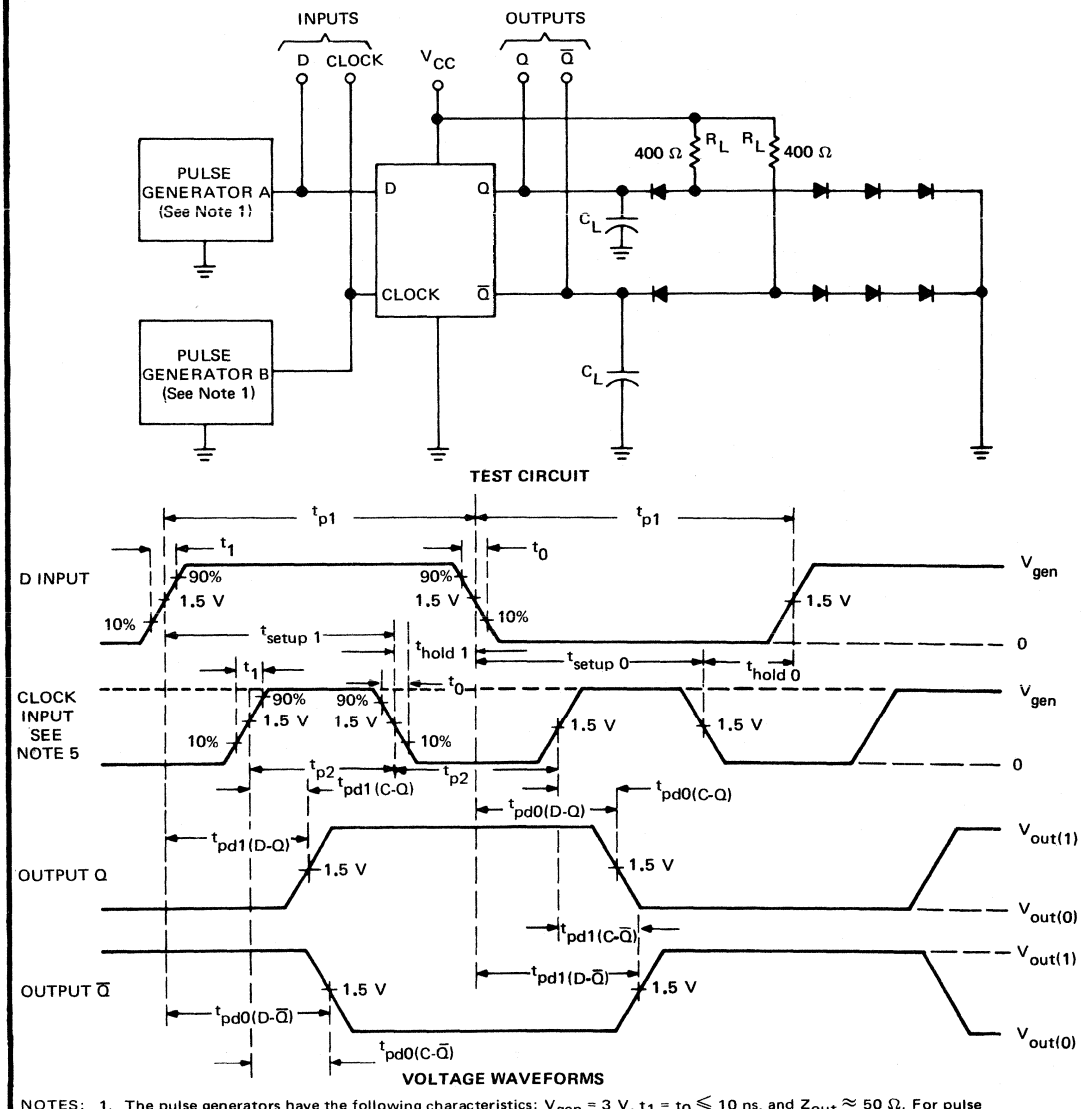
1. All latches are tested simultaneously.

FIGURE 5

† Arrows indicate actual direction of current flow. Complementary $\overline{Q}$ outputs are available on the SN5475/SN7475.

PARAMETER MEASUREMENT INFORMATION

switching characteristics†



NOTES: 1. The pulse generators have the following characteristics: V_{gen} = 3 V, $t_1 = t_0 \leqslant 10$ ns, and $Z_{out} \approx 50\ \Omega$. For pulse generator A t_{p1} = 1 μs and PRR = 500 kHz. For pulse generator B, t_{p2} = 500 ns and PRR = 1 MHz. Positions of D-input and clock-input pulses are varied with respect to each other to verify setup and hold times.

2. Each latch is tested separately.
3. C_L includes probe and jig capacitance.
4. All diodes are 1N3064.
5. When measuring $t_{pd1(D-Q)}$ and $t_{pd0(D-Q)}$ (or $t_{pd0(D-\overline{Q})}$ and $t_{pd1(D-\overline{Q})}$ for the SN5475/SN7475), clock input must be held at logical 1.

FIGURE 6 – SWITCHING TIMES

†Complementary Q outputs are on the SN5475/SN7475 only.

TYPICAL APPLICATION

temporary storage of binary data

This application demonstrates the use of the SN7475 bistable latch as a temporary storage of binary-coded decimal data, from the SN7490 decade counter, which is to be decoded by the SN7441 decoder/driver. Temporary storage is desirable at this point for two reasons:

a. At counting frequencies above several cycles per second, it is sometimes desirable to eliminate the flicker on the display tube caused by reading an input count which is too fast to be recognized.

b. During the time that the latch is storing information the decade counter may start acquiring data for the next display.

A typical sequence of operation is illustrated (see Figure 7):

1. During t_1, reset decade counter to 0. At end of t_1, indicator will display "0".
2. During t_2, count BCD 3 at output of SN7490. Indicator still displays "0".
3. At start of t_3, indicator will display "3". At end of t_3, BCD 3 is committed to memory by SN7475 and the SN7490 may begin counting again.
4. During t_4, reset decade counter to 0 and count BCD 5 at output of SN7490. Indicator still displays "3".
5. At start of t_5, indicator will display "5". At end of t_5, BCD 5 is committed to memory by SN7475 and the SN7490 is released.

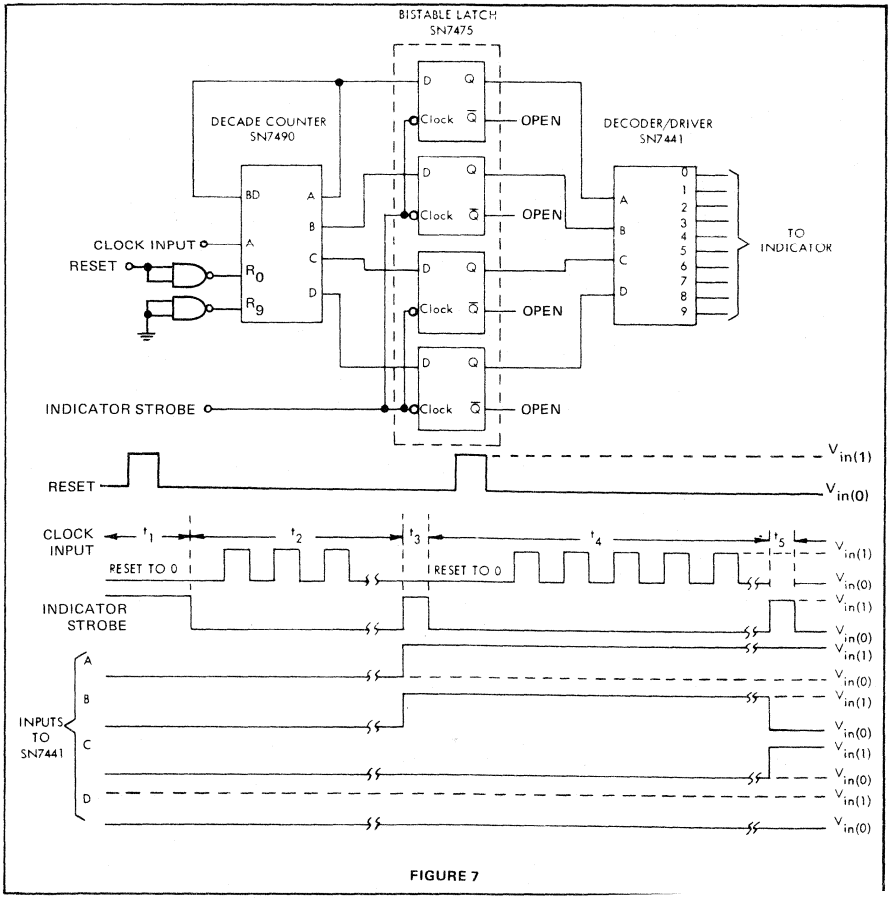


FIGURE 7

TYPICAL APPLICATION

dual D-type master-slave flip-flop

This application demonstrates the use of the SN7475 as a dual D-type master-slave flip-flop, provided that two-phase clocking is permissible. Each of the D-type flip-flops are formed by merely interconnecting the Q output of one of the latches (which serves as the master) to the data input of another latch (which serves as the slave). Each of these interconnected latches must have a separate clock line; therefore if a dual D-type master-slave flip-flop is constructed from a single package (see Figure 8) they must be operated synchronously.

A typical transfer of data is illustrated. Note that after the start of t_1 the data input is released to acquire new information as the master section has "locked up" the original data after clock pulse A_1. At the start of t_2 the data "locked up" in the master is transferred to the output, and at the end of t_2 (and for the duration of t_3) the slave retains the original data.

This type of flip-flop is desirable in applications where speed is not a primary requirement and where the additional clock skew, resulting from this delay between the two clock pulses, affords greater system reliability.

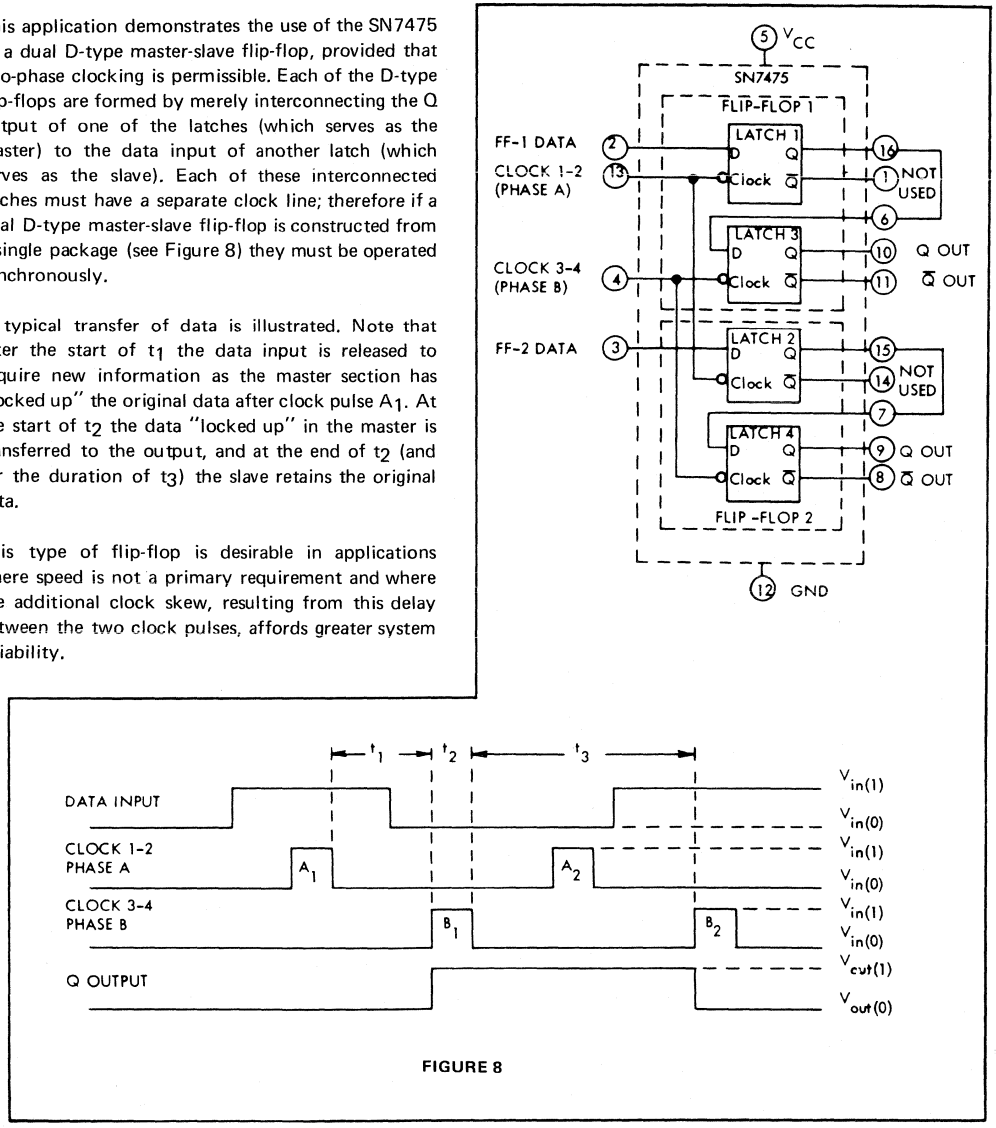


FIGURE 8

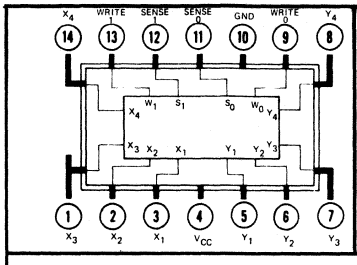
CIRCUIT TYPES SN5481, SN5484, SN7481, SN7484
16-BIT ACTIVE-ELEMENT MEMORIES

description

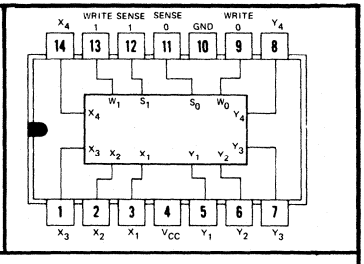
The 16-bit active-element memory is a monolithic, high-speed, transistor-transistor-logic (TTL) array of 16 flip-flops, and two write amplifiers interconnected to form a "scratch-pad" memory with direct-address and non-destructive read-out.

The flop-flops are arranged in a 4-by-4 matrix with each flip-flop representing one bit of 16 words. Four X-address lines and four Y-address lines permit the address of one bit at a time. Each flip-flop, composed of two cross-coupled 3-emitter transistors, is used to store one bit. To determine if a logical 1 or 0 has been stored, it is necessary to know which one of the two flip-flop transistors is conducting. One emitter of each of these transistors serves as the sensing output. All 16 of the logical 1 sensing outputs are connected to the sense logic 1 (S_1) amplifier input and all 16 of the logical0 sensing outputs are connected to the sense logical 0 (S_0) amplifier input. The two remaining emitters on each transistor are used to complete the matrix connections necessary for the X- and Y-address lines. Address line inputs are normally held low (logical 0) and currents from all conducting flip-flop transistors flow out these address lines.

SN5481/SN7481 CIRCUITS
S FLAT PACKAGE (TOP VIEW)

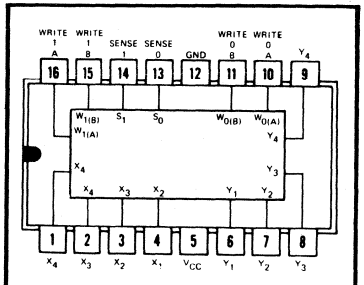


SN5481/SN7481 CIRCUITS
J OR N DUAL-IN-LINE PACKAGE (TOP VIEW)



positive logic: see logic diagram

SN5484/SN7484 CIRCUITS
J OR N DUAL-IN-LINE PACKAGE (TOP VIEW)



positive logic: see logic diagram

To address a flip-flop both the X- and Y-address lines associated with that flip-flop are taken to a logical 1 voltage. Due to the matrix nature of the circuit, at least one address line of all flip-flops except the one being addressed will continue to remain at a logical 0 level and no change will occur on those flip-flops. But, in the addressed flip-flop, the current in the conducting transistor diverts from the address lines to the appropriate sense line and then to one of the sense amplifiers. Thus, either the sense amplifier associated with a logical 1 or the sense amplifier associated with a logical 0 is activated. When this occurs, the output of the activated sense amplifier drops from a logical 1 to a logical 0 level. The memory is non-destructive as the states of the flip-flops are not disturbed during sensing. The memory is volatile and information will be lost if the supply voltage is removed.

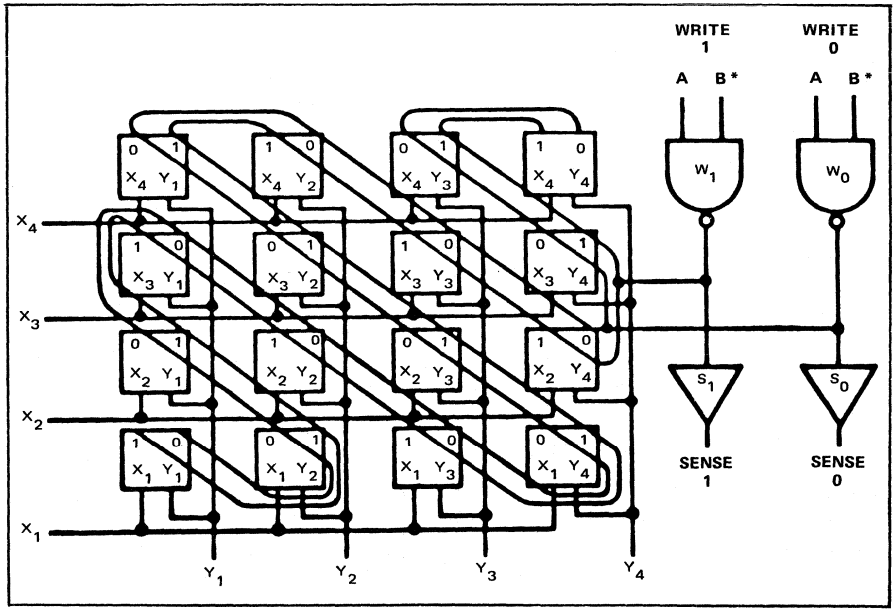
description (continued)

To store new information in a flip-flop, it is necessary to address it and apply logical 1 voltage to the appropriate write amplifier input. (The SN5484/SN7484 circuit has gated write-amplifier inputs). The output of the write amplifier responds by dropping to a logical 0 level. Since all logical 0 sense lines are connected to the output of the logical 0 write amplifier and all logical 1 sense lines are connected to the output of the logical 1 write amplifier, a logical 0 voltage on the output of a write amplifier will apply the same voltage to emitters of all flip-flop transistors connected to that amplifier. In all flip-flops except the one being addressed, this low voltage has no effect since at least one other emitter on each of the flip-flop transistors is held low by the address lines. But two possibilities exist with the flip-flop that is addressed. The flip-flop may already be in the desired state, in which case no change occurs. But if the flip-flop must be changed from one state to the other, the low voltage applied to the emitter of the transistor which is not conducting turns that transistor on causing the other transistor to turn off.

Since the connection between the output of the write amplifier and the sense line is common to the input of the sense amplifier, the memory cannot be used to provide information on the state of a bit while the write amplifiers are activated.

A number of active element memories may be paralleled to form the desired matrix size (number of words) and to form the desired word length (number of bits). Standard TTL circuitry, employed for the address line inputs, write amplifier inputs, and the saturating output transistors, provides complete TTL and DTL compatibility and maintains typical noise margins of one volt. Average power dissipation is 275 milliwatts (typical), and the open-collector outputs may be wire-OR connected to similar outputs. Internal circuitry of the write and sense amplifiers are operated within their linear range to improve speed. Sensing propagation delay times are typically 20 nanoseconds when operated at full fan-out and 30 picofarads of circuit capacitance.

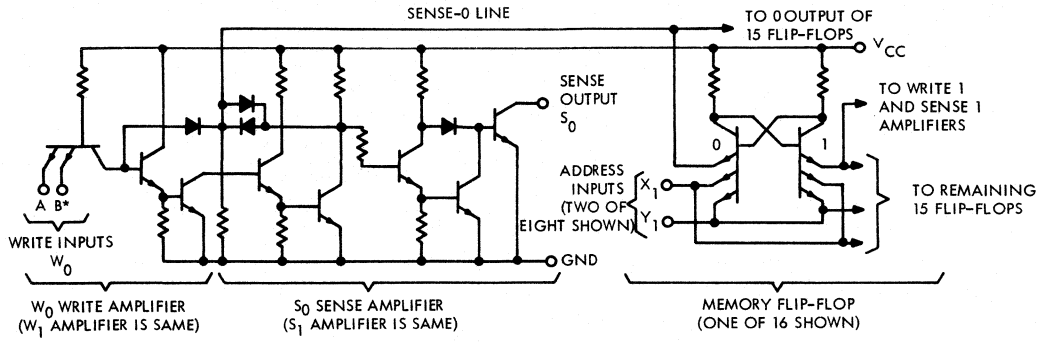
logic diagram



*Gated inputs (as shown) are available on SN5484/SN7484 only.

The SN5481/SN7481 has one W_0 and one W_1 input.

schematic diagram



* Gated inputs (as shown) are available on SN5484/SN7484 only. The SN5481/SN7481 has one W_0 and one W_1 input.

absolute maximum ratings (over operating temperature range unless otherwise noted)

Supply Voltage V_{CC} (See Note 1)	7 V
Input Voltage, V_{in} (See Notes 1 and 2)	5.5 V
Operating Case Temperature Range: SN5481S	−55°C to 125°C
Operating Free-Air Temperature Range: SN5481J/N, SN5484J/N	−55°C to 125°C
SN7481, SN7484 Circuits	0°C to 70°C
Storage Temperature Range	−65°C to 150°C

recommended operating conditions (over operating temperature range)

	MIN	NOM	MAX	UNIT
Supply Voltage V_{CC} (See Note 1): SN5481, SN5484 Circuits	4.5	5	5.5	V
SN7481, SN7484 Circuits	4.75	5	5.25	V
Width of Write Pulse, $t_{p(write)}$ (See Figure 11)	25			ns
Address Lines Input Setup Time, t_{setup} (See Figure 11)	0			ns

NOTES: 1. These voltage values are with respect to ground terminal.
2. Input signals must be zero or positive with respect to network ground terminal.

electrical characteristics (over operating temperature range unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
$V_{in(1)AW}$ or $V_{in(1)AS}$	Input voltage required at X or Y address lines to ensure writing or sensing	1	V_{CC} = MIN, I_{sink} = 20 mA, $V_{out(0)} \leq 0.4$ V	SN5481, SN5484	2.1			V
			V_{CC} = MIN, I_{sink} = 40 mA, $V_{out(0)} \leq 0.4$ V	SN7481, SN7484	2.1			V
$V_{in(1)W}$	Input voltage required at W_0 or W_1 inputs to ensure writing	1	V_{CC} = MIN, I_{sink} = 20 mA, $V_{out(0)} \leq 0.4$ V	SN5481, SN5484	2			V
			V_{CC} = MIN, I_{sink} = 40 mA, $V_{out(0)} \leq 0.4$ V	SN7481, SN7484	2			V
$V_{in(0)A\overline{W}}$	Input voltage required at X or Y address lines to prevent writing	2	V_{CC} = MIN, I_{sink} = 20 mA, $V_{out(0)} \leq 0.4$ V	SN5481, SN5484			0.8	V
			V_{CC} = MIN, I_{sink} = 40 mA, $V_{out(0)} \leq 0.4$ V	SN7481, SN7484			0.8	V
$V_{in(0)A\overline{S}}$	Input voltage required at X or Y address lines to prevent sensing	3	V_{CC} = MIN, $I_{out(1)}$ = 250 μA, V_{out} = 5.5 V				1	V
$V_{in(0)\overline{W}}$	Input voltage required at W_0 or W_1 to prevent writing	1	V_{CC} = MIN, I_{sink} = 20 mA, $V_{out(0)} \leq 0.4$ V	SN5481, SN5484			1	V
			V_{CC} = MIN, I_{sink} = 40 mA, $V_{out(0)} \leq 0.4$ V	SN7481, SN7484			1	V
$V_{out(1)}$	Logical 1 output voltage	3	V_{CC} = MIN, $I_{out(1)}$ = 250 μA		5.5			V
$V_{out(0)}$	Logical 0 output voltage (on level)	1 and 2	V_{CC} = MIN, I_{sink} = 20 mA	SN5481, SN5484			0.4	V
			V_{CC} = MIN, I_{sink} = 40 mA	SN7481, SN7484			0.4	V
$I_{in(0)}$	Logical 0 level input current at write 1 and write 0 (each input)	4	V_{CC} = MAX, V_{in} = 0.4 V				−1.6	mA
$I_{in(0)}$	Logical 0 level input current at all X or all Y address lines	5	V_{CC} = MAX, V_{in} = 0.4 V				−11	mA
$I_{in(1)}$	Logical 1 level input current at write 1 and write 0 (each input)	6	V_{CC} = MAX, V_{in} = 2.4 V				40	μA
			V_{CC} = MAX, V_{in} = 5.5 V				1	mA
$I_{in(1)}$	Logical 1 level input current at each X and each Y address line	6	V_{CC} = MAX, V_{in} = 4.5 V				400	μA
			V_{CC} = MAX, V_{in} = 5.5 V				3	mA
I_{CC}	Supply current	6	V_{CC} = MAX	SN5481, SN5484		55	78	mA
				SN7481, SN7484		55	91	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

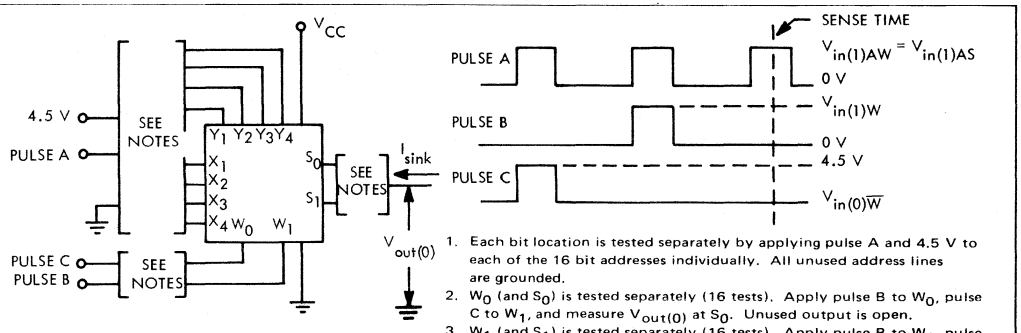
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

—SEE ORDERING INSTRUCTIONS PAGE 1-1—

switching characteristics V_{CC} = 5 V, T_A = 25°C

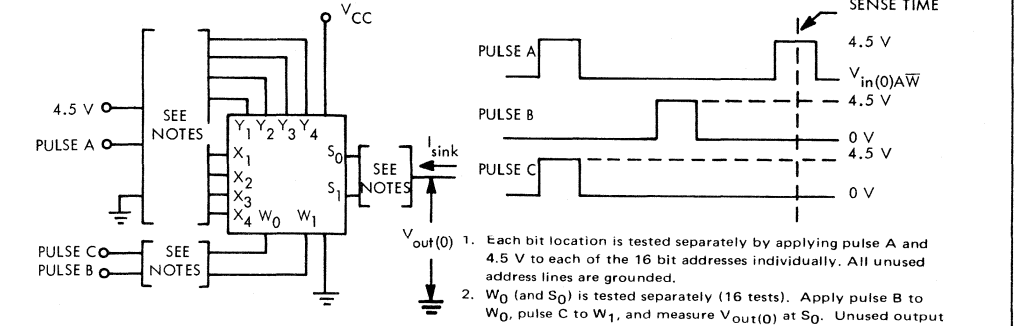
PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{WR}	Write recovery time	7	C_L = 15 pF, X_1 - Y_1 location addressed		30	60	ns
t_{pd0}	Propagation delay time to logical 0 level from address-line inputs to S_0 or S_1 outputs	7	C_L = 15 pF, X_1 - Y_1 location addressed		22	45	ns
			C_L = 15 pF, X_1 =Y_1 location addressed		27	55	ns
t_{pd1}	Propagation delay time to logical 1 level from address-line inputs to S_0 or S_1 outputs	7	C_L = 15 pF, X_1 - Y_1 location addressed		15	25	ns
			C_L = 200 pF, X_1 - Y_1 location addressed		20	35	ns
t_{pd0}	Propagation delay time to logical 0 level from address-line inputs to S_0 or S_1 outputs	7	C_L = 15 pF, X_1 through X_4 and Y_1 locations addressed		20	30	ns

d-c test circuits† PARAMETER MEASUREMENT INFORMATION



1. Each bit location is tested separately by applying pulse A and 4.5 V to each of the 16 bit addresses individually. All unused address lines are grounded.
2. W_0 (and S_0) is tested separately (16 tests). Apply pulse B to W_0, pulse C to W_1, and measure $V_{out(0)}$ at S_0. Unused output is open.
3. W_1 (and S_1) is tested separately (16 tests). Apply pulse B to W_1, pulse C to W_0, and measure $V_{out(0)}$ at S_1. Unused output is open.
4. For the SN5484/SN7484, each of the two W_0 or two W_1 inputs are tested separately. Apply 4.5 V to unused W_0 or W_1 inputs.

FIGURE 1



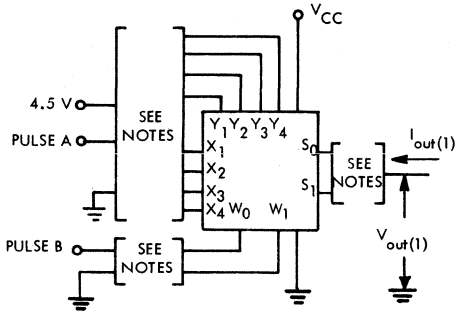
1. Each bit location is tested separately by applying pulse A and 4.5 V to each of the 16 bit addresses individually. All unused address lines are grounded.
2. W_0 (and S_0) is tested separately (16 tests). Apply pulse B to W_0, pulse C to W_1, and measure $V_{out(0)}$ at S_0. Unused output is open.
3. W_1 (and S_1) are tested separately (16 tests). Apply pulse B to W_1, pulse C to W_0, and measure $V_{out(0)}$ at S_1. Unused output is open.
4. For the SN5484/SN7484, each of the two W_0 or two W_1 inputs are tested separately. Apply 4.5 V to unused W_0 or W_1 inputs.

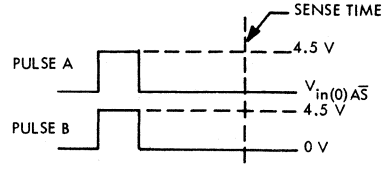
FIGURE 2

†Arrows indicate actual direction of current flow.

PARAMETER MEASUREMENT INFORMATION

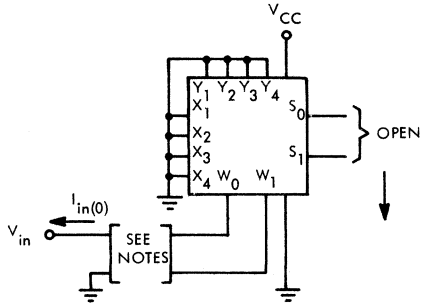
d-c test circuits† (continued)





1. Each bit location is tested separately by applying pulse A and 4.5 V to each of the 16 bit addresses individually. All unused address lines are grounded.
2. W_0 (and S_0) is tested separately (16 tests). Apply pulse B to W_0, ground W_1, and measure $V_{out(1)}$ at S_0. Unused output is open.
3. W_1 (and S_1) is tested separately (16 tests). Apply pulse B to W_1, ground W_0, and measure $V_{out(1)}$ at S_1. Unused output is open.
4. For the SN5484/SN7484, each of the two W_0 or two W_1 inputs are tested separately. Apply 4.5 V to the unused input of the gate under test and ground both inputs of the unused gate.

FIGURE 3



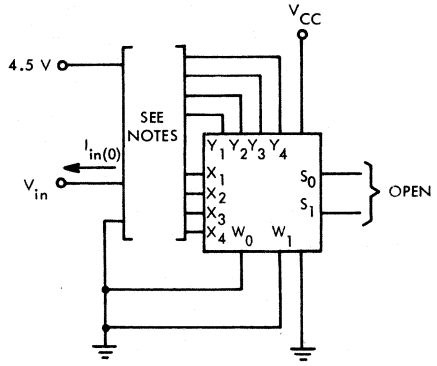
1. Each input is tested separately.
2. All unused inputs are grounded.

FIGURE 4

† Arrows indicate actual direction of current flow.

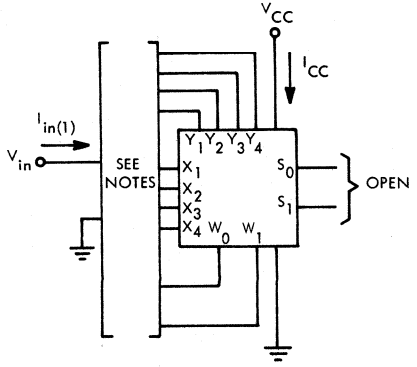
PARAMETER MEASUREMENT INFORMATION

d-c test circuits† (continued)



1. Each X input is tested separately with the other three X inputs grounded and 4.5 V applied to all Y inputs.
2. Each Y input is tested separately with the other three Y inputs grounded and 4.5 V applied to all Y inputs.
3. For the SN5484/SN7484, both W_0 and both W_1 inputs are grounded.

FIGURE 5



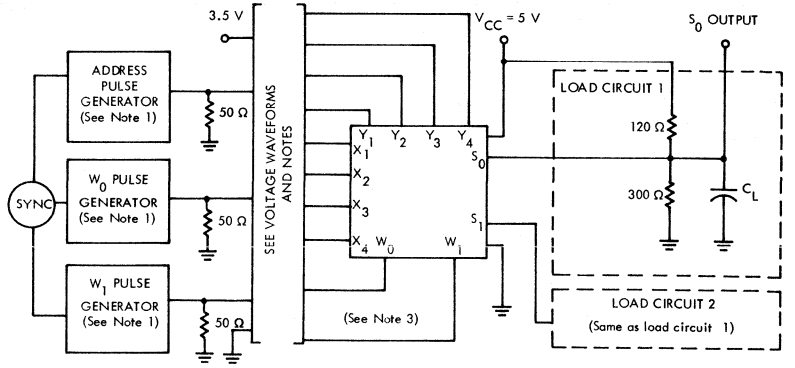
1. Each input is tested separately for $I_{in(1)}$ with all unused inputs grounded.
2. When measuring I_{CC} all inputs are grounded.

FIGURE 6

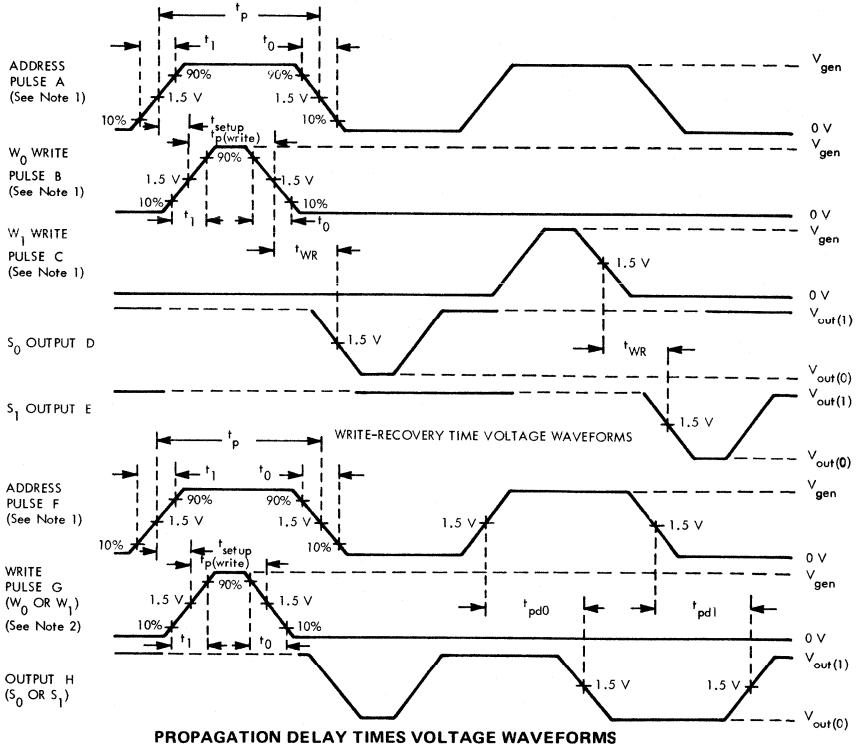
† Arrows indicate actual direction of current flow.

PARAMETER MEASUREMENT INFORMATION

switching characteristics



TEST CIRCUIT



PROPAGATION DELAY TIMES VOLTAGE WAVEFORMS

NOTES: 1. The pulse generators have the following characteristics: V_{gen} = 3 V, $t_1 = t_0$ = 10 ns, t_{setup} = 0 to 10 ns. For the address pulse generator, t_p = 100 ns and PRR = 2 MHz. For the W_0 and W_1 pulse generators, t_p = 25 ns and PRR = 1 MHz.

2. C_L includes probe and jig capacitance.

3. For the SN5484/SN7484, unused W_0 and W_1 inputs are 3.5 V.

FIGURE 7 – SWITCHING CHARACTERISTICS

TYPICAL APPLICATIONS

This application demonstrates use of the 16-bit active element memory to form a high-speed, direct-address, scratch-pad memory having a storage capability of m-words (in multiples of 16) of n-bit length. For purposes of this discussion, a memory is illustrated which will store 64 words each having a length of 8-bits. See Figure A. This storage capability may be increased or decreased using the patterns shown.

In this example, each of the planes consist of four 16-bit memory circuits connected in an 8-by-8 matrix. This organization provides 64 addresses (words) of 8-bits (word length) or a total bit capability of 512 bits (64 X 8).

Each bit plane (B_0 through B_7) is formed by paralleling the W_0, W_1 inputs, S_0, S_1 outputs, and completing the X-Y matrix connections. The matrix is completed by paralleling the X lines of Circuits A-B and C-D and the Y lines of A-C then B-D, to form the 64 addresses of plane B_0. Two pull-up resistors, one for S_0 and one for S_1, should be provided for wired-OR outputs. The other seven planes are identical to B_0.

The X and Y lines of the eight planes are paralleled so that all bits of each word are addressed simultaneously. Addressing of a particular word is accomplished by the X-Y decoder/drivers. For this particular example, the decoder could be a 1-of-8 decoder (see SN7442 and SN7444 applications) and the drivers may consist of discrete transistors, each capable of supplying current for 16 address inputs. A number of decoding/driving schemes are possible.

The SN5484/SN7484 has gated W_0 and W_1 inputs which may be used to perform the write enable function. External gating may be employed if enabling functions are required with the SN5481/SN7481.

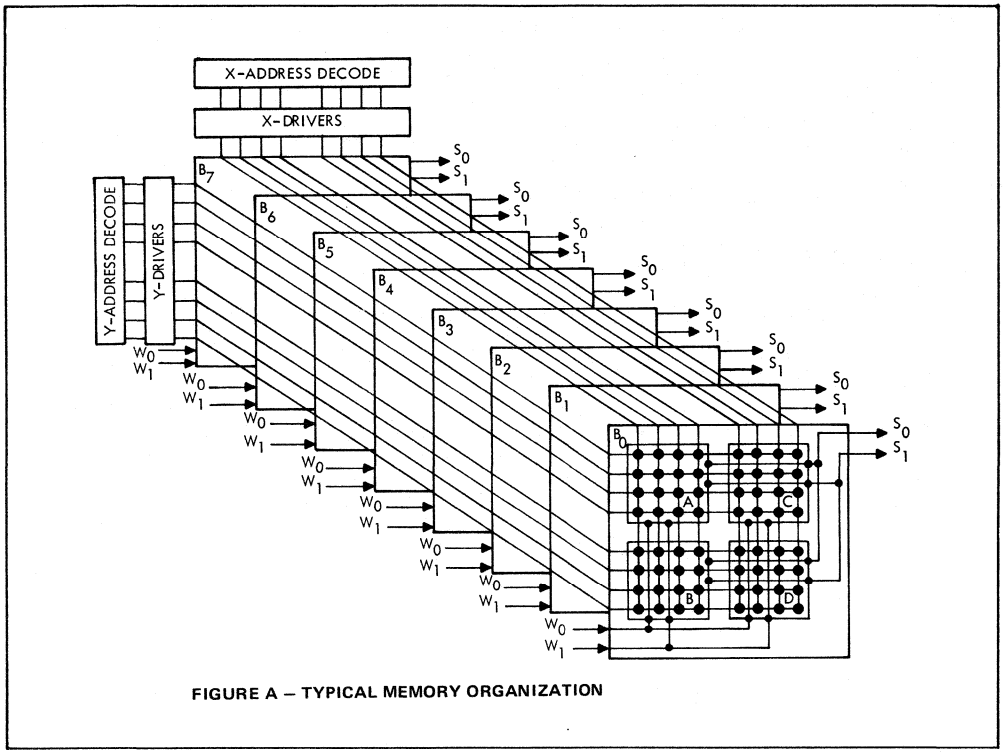


FIGURE A – TYPICAL MEMORY ORGANIZATION

Series 54/74 TTL

The most complete IC logic family in the industry... and the first choice for new designs. Here's why:

- **Over 90 distinct functions to select from...including 35 MSI circuits**
- **Three compatible performance ranges**
  - **Series 54/74 standard**
  - **Series 54H/74H high speed**
  - **Series 54L/74L low power**
- **Three package configurations**
  - **Plastic dual-in-line**
  - **Ceramic dual-in-line**
  - **Metal flatpack**
- **Two temperature ranges**
  - **Series 54...−55° to +125°C**
  - **Series 74...0° to 70°C**

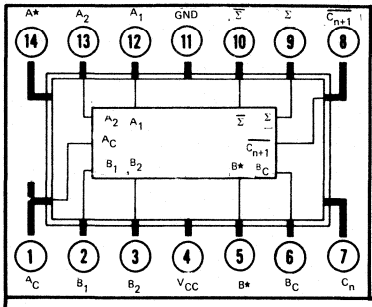
CIRCUIT TYPES SN5480, SN7480
GATED FULL ADDERS

logic

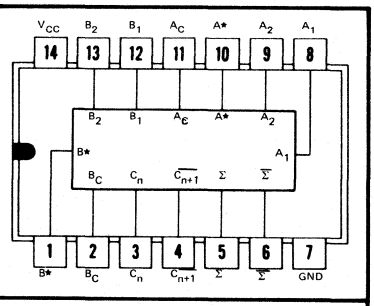
TRUTH TABLE
(See Notes 1, 2, and 3)

C_n	B	A	$\overline{C_{n+1}}$	$\overline{\Sigma}$	Σ
0	0	0	1	1	0
0	0	1	1	0	1
0	1	0	1	0	1
0	1	1	0	1	0
1	0	0	1	0	1
1	0	1	0	1	0
1	1	0	0	1	0
1	1	1	0	0	1

S
FLAT PACKAGE (TOP VIEW)



J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



positive logic: See truth table

NOTES: 1. $A = \overline{A^* \cdot A_C}$, $B = \overline{B^* \cdot B_C}$ where $A^* = \overline{A_1 \cdot A_2}$, $B^* = \overline{B_1 \cdot B_2}$
2. When A* or B* are used as inputs, A_1 and A_2 or B_1 and B_2 respectively must be connected to GND.
3. When A_1 and A_2 or B_1 and B_2 are used as inputs, A*or B* respectively must be open or used to perform Dot-OR logic.

description

This single-bit, high-speed, binary full adder with gated complementary inputs, complementary sum (Σ and $\overline{\Sigma}$) outputs and inverted carry output is designed for medium- and high-speed, multiple-bit, parallel-add/serial-carry applications. The circuit (see schematic diagram) utilizes diode-transistor logic (DTL) for the gated inputs, and high-speed, high-fan-out transistor-transistor logic (TTL) for the sum and carry outputs. The circuit is entirely compatible with both DTL and TTL logic families. The implementation of a single-inversion, high-speed, Darlington-connected serial-carry circuit minimizes the necessity for extensive "look-ahead" and carry-cascading circuits.

absolute maximum ratings (over operating temperature range unless otherwise noted)

Supply Voltage V_{CC} (See Note 4) . . . . . 7 V
Input Voltage, V_{in} (See Notes 4 and 5) . . . . . 5.5 V
Operating Case Temperature Range: SN5480S Circuits . . . . . −55°C to 125°C
Operating Free-Air Temperature Range: SN5480J, SN5480N Circuits . . . . . −55°C to 125°C
SN7480 Circuits . . . . . 0°C to 70°C
Storage Temperature Range . . . . . −65°C to 150°C

recommended operating conditions (over operating temperature range)

	MIN	NOM	MAX	UNIT
Supply Voltage V_{CC}: SN5480 Circuits	4.5	5	5.5	V
SN7480 Circuits	4.75	5	5.25	V
Normalized Fan-Out From Outputs:				
$\overline{C_{n+1}}$, N			5	
Σ or $\overline{\Sigma}$, N			10	
A* or B*, N			3	

NOTES: 4. The voltages are with respect to ground terminal.
5. Input signals must be zero or positive with respect to network ground terminal.

electrical characteristics (over operating temperature range unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
$V_{in(1)}$	Logical 1 input voltage	1 and 2	V_{CC} = MIN		2			V
$V_{in(0)}$	Logical 0 input voltage	1 and 2	V_{CC} = MIN				0.8	V
$V_{out(1)}$	Logical 1 output voltage	2	V_{CC} = MIN		2.4	3.5		V
$V_{out(0)}$	Logical 0 output voltage	1	V_{CC} = MIN			0.22	0.4	V
$I_{in(0)}$	Logical 0 level input current at A_1, A_2, B_1, B_2, A_c or B_c	3	V_{CC} = MAX,	V_{in} = 0.4 V			−1.6	mA
$I_{in(0)}$	Logical 0 level input current at A★ or B★	4	V_{CC} = MAX,	V_{in} = 0.4 V			−2.6	mA
$I_{in(0)}$	Logical 0 level input current at C_n	4	V_{CC} = MAX,	V_{in} = 0.4 V			−8	mA
$I_{in(1)}$	Logical 1 level input current at A_1, A_2, B_1, B_2, A_c or B_c	5	V_{CC} = MAX,	V_{in} = 2.4 V			15	μA
			V_{CC} = MAX,	V_{in} = 5.5 V			1	mA
$I_{in(1)}$	Logical 1 level input current at C_n	6	V_{CC} = MAX,	V_{in} = 2.4 V			200	μA
			V_{CC} = MAX,	V_{in} = 5.5 V			1	mA
I_{OS}	Short-circuit output current at Σ or $\overline{\Sigma}$§	7	V_{CC} = MAX	SN5480	−20		−57	mA
				SN7480	−18		−57	mA
I_{OS}	Short-circuit output current at $\overline{C_{n+1}}$§	7	V_{CC} = MAX	SN5480	−20		−70	mA
				SN7480	−18		−70	mA
I_{CC}	Supply current	8	V_{CC} = MAX	SN5480		21	31	mA
				SN7480		21	35	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ Not more than one output should be shorted at a time.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER¶	FROM INPUT	TO OUTPUT	FIGURE 9 TEST NO.	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{pd1}	C_n	$\overline{C_{n+1}}$	1	C_L = 15 pF, R_L = 780 Ω		13	17	ns
t_{pd0}			2	C_L = 15 pF, R_L = 780 Ω		8	12	ns
t_{pd1}	B_C	$\overline{C_{n+1}}$	3	C_L = 15 pF, R_L = 780 Ω		18	25	ns
t_{pd0}			4	C_L = 15 pF, R_L = 780 Ω		38	55	ns
t_{pd1}	A_C	Σ	5	C_L = 15 pF, R_L = 400 Ω		52	70	ns
t_{pd0}			6	C_L = 15 pF, R_L = 400 Ω		62	80	ns
t_{pd1}	B_C	$\overline{\Sigma}$	7	C_L = 15 pF, R_L = 400 Ω		38	55	ns
t_{pd0}			8	C_L = 15 pF, R_L = 400 Ω		56	75	ns
t_{pd1}	A_1	A★	9	C_L = 15 pF		48	65	ns
t_{pd0}			10	C_L = 15 pF		17	25	ns
t_{pd1}	B_1	B★	11	C_L = 15 pF		48	65	ns
t_{pd0}			12	C_L = 15 pF		17	25	ns

¶ t_{pd1} is propagation delay time to logical 1 level. t_{pd0} is propagation delay time to logical 0 level.

— SEE ORDERING INSTRUCTIONS PAGE 1-1 —

TYPICAL APPLICATIONS

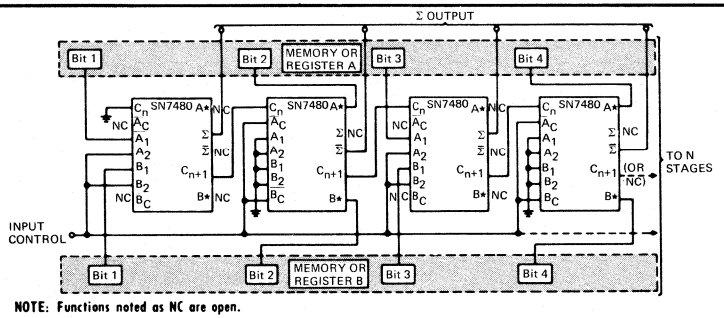
n-bit binary adder or subtractor (see figures A and B)

The SN7480 is designed specifically for N-bit adder or subtractor operations without external gates or inverters. In both applications, the sum or difference functions are generated in parallel while the carry functions are obtained serially. When the number of stages is small, the add or subtract time determines the maximum system clock rate. However, as the number of bits increases, the time required for the carry function to ripple through each bit becomes the limiting factor. Normally the ripple time of adders built with standard integrated circuits is excessive, and the resulting system speed is so slow that other more complex methods are required to perform these functions.

In the SN7480, two methods are used to reduce the carry delay. The carry circuit employs a high-speed Darlington output, and the logic gating has only one inversion between the C_n input and the C_{n+1} output. This logic configuration results in an inverted carry output, and consequently an inverted carry input to the succeeding stage. To counteract this inverted input without sacrificing propagation time through the carry, gates are provided within the circuit to invert the A and B inputs and the resulting sum or difference output. This interconnection method is illustrated by bit 2 and bit 4 of the adder (Figure A). The inverted carry output is a true carry from bit 2 and bit 4, enabling the use of noninverted A and B inputs for the odd-numbered bits.

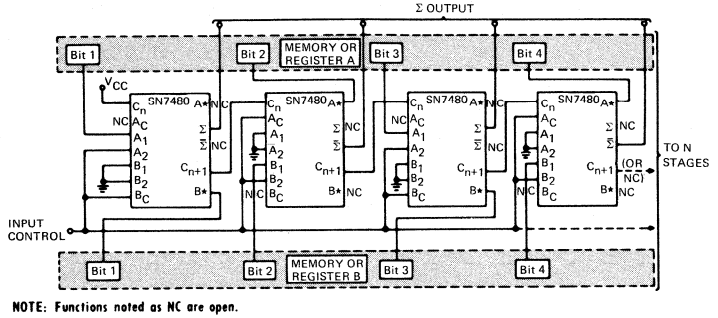
When performing subtraction (Figure B) the C_n input to bit 1 is connected to a logical 1 and input bits and input control functions for the subtrahend (memory or register B) are effectively inverted.

The input control is used to disable the A and B inputs when memory or register information is being shifted. A logical 0 applied to this line will bring each sum or difference output to a logical 0 condition and maintain this level regardless of the state of the input information into each bit. For the adder (Figure A), input control is applied to A_2 and B_2 of odd-numbered bits and to A_C and B_C of even numbered bits. For the subtractor (Figure B), input control is applied to A_2 and B_C of the odd-numbered bits and to A_C and B_2 of the even-numbered bits. These alternating patterns are necessary to complement the varying input sequence which they control.



NOTE: Functions noted as NC are open.

FIGURE A – N-BIT BINARY ADDER



NOTE: Functions noted as NC are open.

FIGURE B – N-BIT BINARY SUBTRACTOR

TYPICAL APPLICATIONS

n-bit binary adder with register selection (see figure C)

This application fully utilizes the flexibility of the input gating available within the SN7480. Two "A" registers and two "B" registers drive a single adder for each bit required. Register selection is performed internally for registers A_1 and B_1, and externally by a type SN7405 TTL gate for registers A_2 and B_2. Dot-OR logic is performed at the A★ and B★ nodes within the the adder when the register selection is made.

Operation is as follows: To add the contents of Register A_1 to Register B_1, A_2 and B_2 control lines are brought to the logical 0 state. In similar fashion, the contents of register A_1 are added to register B_2 by holding A_2 and B_1 control lines at a logical 0. Four register combinations may be used. Even-numbered input bits from each register must be inverted since the A★ and B★ inputs are being used to perform Dot-OR logic. This is not a configuration restriction for flip-flop type registers and memories, but may require additional logic elements if other storage configurations are used as inputs.

The input control function is available as in the previous application and is implemented by bringing all four register control lines and the input control line to a logical 0 level. This condition ensures a logical 0 at each Σ output regardless of "A" and "B" register logic levels.

Up to four "A" registers and four "B" registers may be implemented in a fashion analogous to that shown in Figure C. Inputs from the register-control gates (SN7405) of the additional registers would be Dot-OR connected with A_2 and B_2 registers at the A★ and B★ inputs.

To perform N-bit subtraction, the C_n input at bit 1 is connected to a logical 1 and bit inputs from each register or memory used as a subtrahend must consist of the complement of bit inputs shown for the adder addend. Input control remains the same.

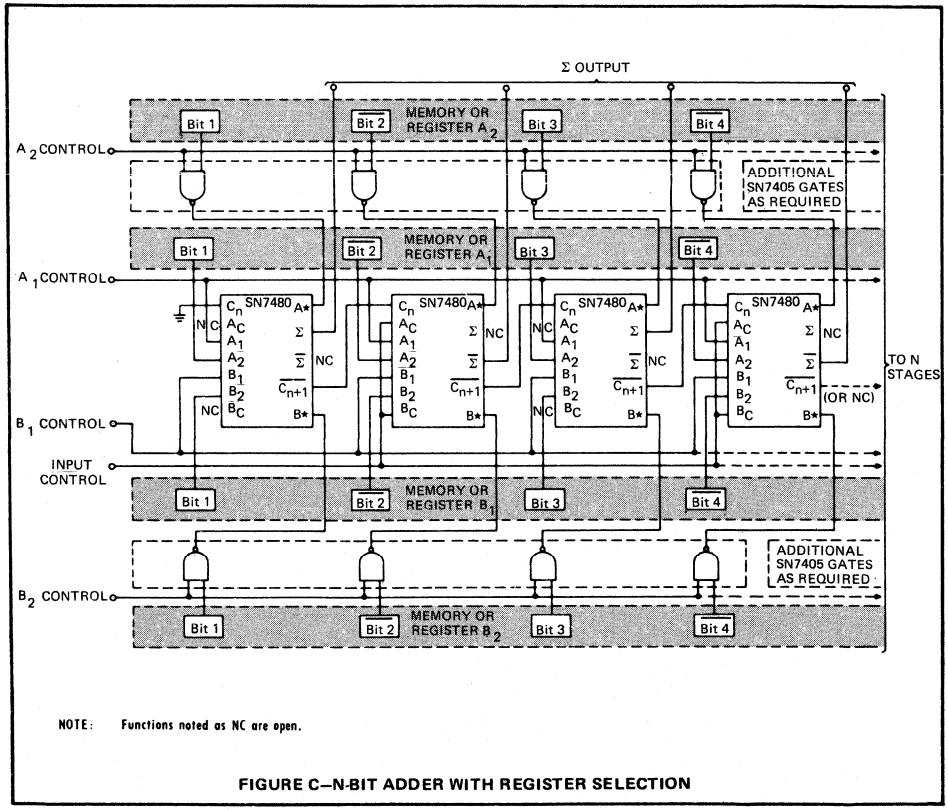
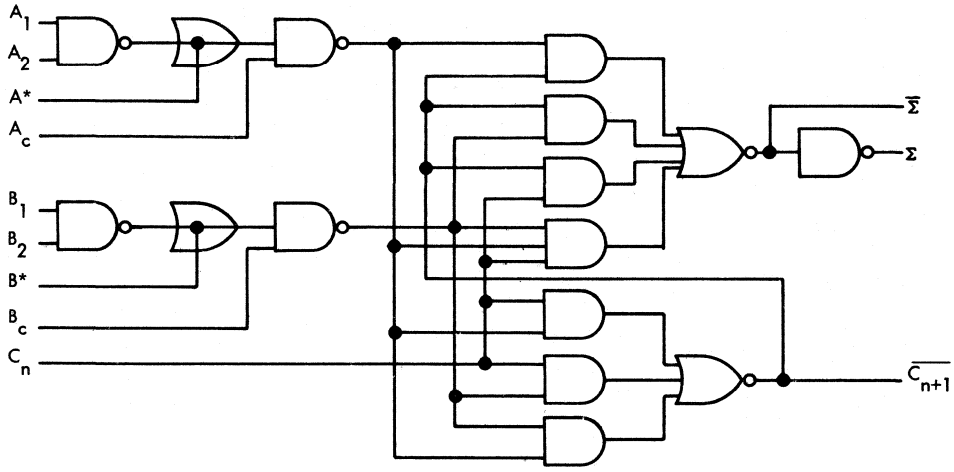
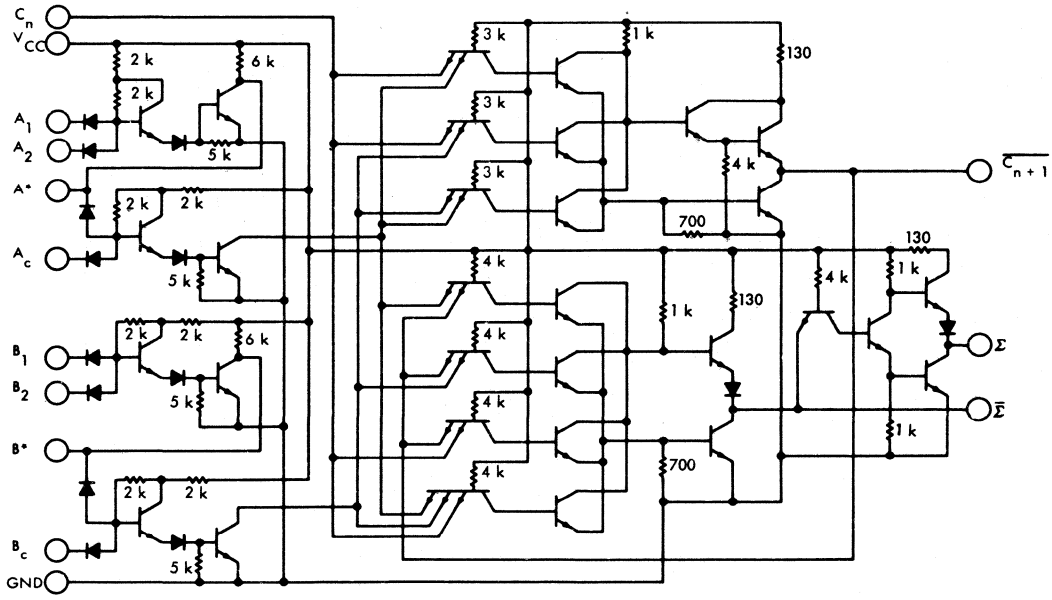


FIGURE C–N-BIT ADDER WITH REGISTER SELECTION

functional block diagram



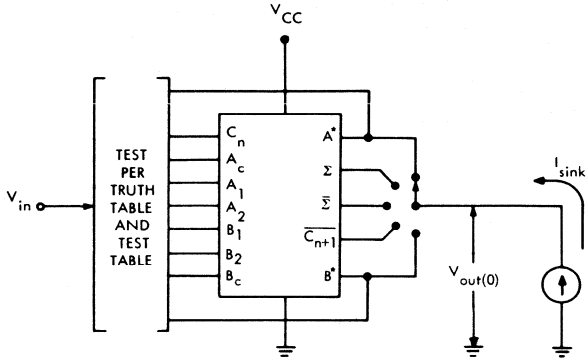
schematic



Component values shown are nominal.
Resistor values are in ohms.

PARAMETER MEASUREMENT INFORMATION

d-c test circuits§

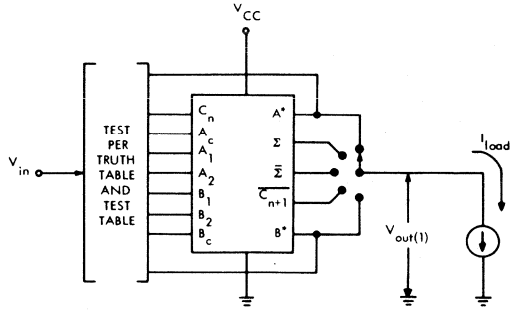


TEST TABLE

Output Under Test	I_{sink} (Min)
Σ or $\overline{\Sigma}$	16 mA
$\overline{C_{n+1}}$	8 mA
A★ or B★	4.8 mA

1. Each input or output is tested separately.
2. When A★ is tested A_1 and A_2 are at GND. When B★ is tested B_1 and B_2 are at GND.
3. When A_1 and A_2 or B_1 and B_2 is tested, A★ or B★ respectively, is open.

FIGURE 1



TEST TABLE

Output Under Test	I_{load} (Min)
Σ or $\overline{\Sigma}$	−400 μA
$\overline{C_{n+1}}$	−200 μA
A★ or B★	−120 μA

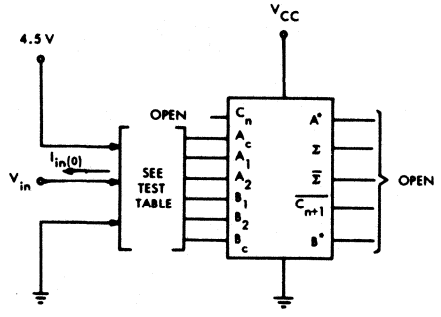
1. Each input or output is tested separately.
2. When A★ is tested A_1 and A_2 are at GND. When B★ is tested B_1 and B_2 are at GND.
3. When A_1 and A_2 or B_1 and B_2 are tested A★ or B★, respectively, is open.

FIGURE 2

§Arrows indicate actual direction of current flow.

PARAMETER MEASUREMENT INFORMATION

d-c test circuits§ (continued)

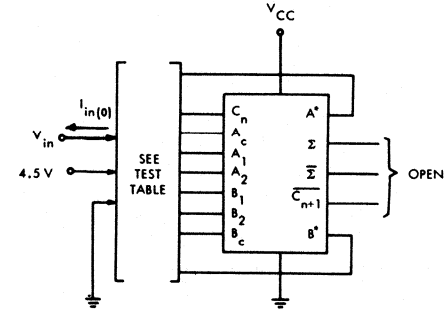


TEST TABLE

Apply V_{in} (Test $I_{in(0)}$)	Apply 4.5 V	GND
A_1	A_2	None
A_2	A_1	None
B_1	B_2	None
B_2	B_1	None
A_C	None	A_1 and A_2
B_C	None	B_1 and B_2

1. Each input is tested separately.

FIGURE 3



TEST TABLE

Apply V_{in} (Test $I_{in(0)}$)	Apply 4.5 V	GND
A★	A_C	A_1 and A_2
B★	B_C	B_1 and B_2
C_n	None	None

Unused inputs are open.

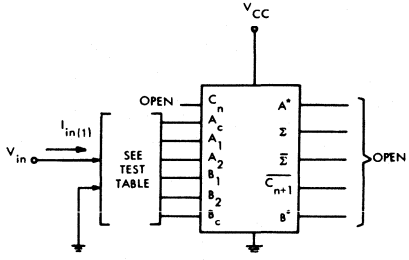
1. Each input is tested separately.

FIGURE 4

§Arrows indicate actual direction of current flow.

PARAMETER MEASUREMENT INFORMATION

d-c test circuits§ (continued)



1. Each input is tested separately.

TEST TABLE

Apply V_{in} (Test $I_{in(1)}$)	GND
A_1	A_2
A_2	A_1
B_1	B_2
B_2	B_1
A_c	A★
B_c	B★

FIGURE 5

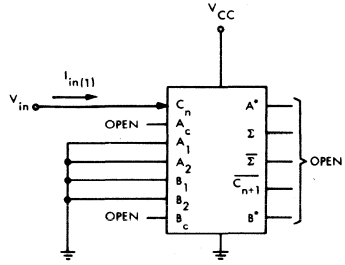
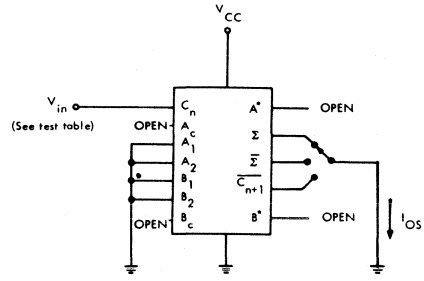


FIGURE 6



1. Each output is tested separately.

TEST TABLE

Output Under Test	V_{in} Value
Σ	V_{CC}
$\overline{\Sigma}$ or $\overline{C_n + 1}$	GND

FIGURE 7

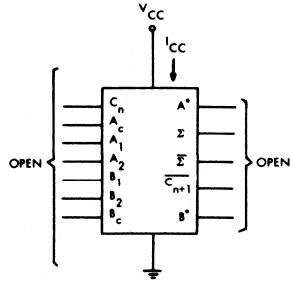
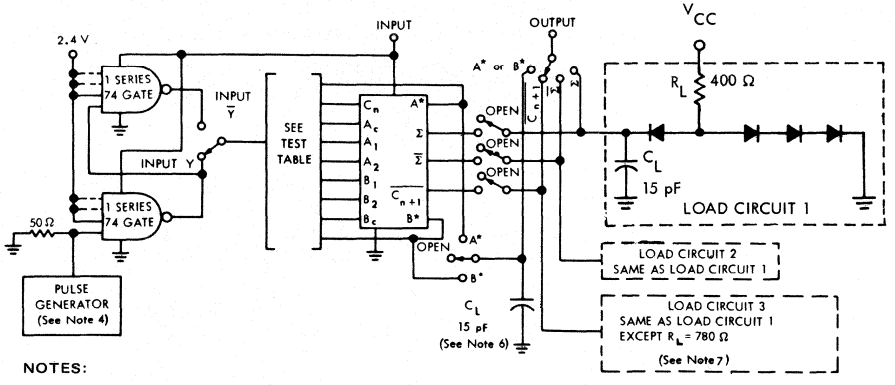


FIGURE 8

§ Arrows indicate actual direction of current flow.

PARAMETER MEASUREMENT INFORMATION

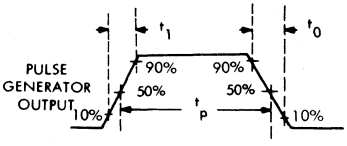
switching characteristics



NOTES:

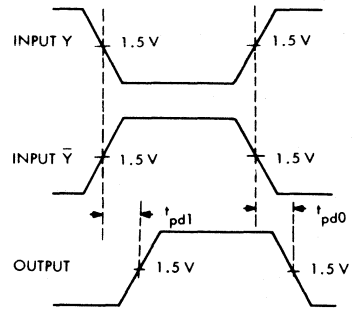
1. Perform test in accordance with test table.
2. Each output is tested separately.
3. Voltage values are with respect to network GND terminal.
4. The generator has the following characteristics: V_{gen} = 3 V, $t_1 = t_0 \leqslant 15$ ns, t_p = 0.5 μs, PRR = 1 MHz, and $Z_{out} \approx 50\ \Omega$.
5. Inputs and outputs not otherwise specified are open.
6. C_L includes probe and jig capacitance.
7. Load circuit 2 simulates output load of 5.
8. All diodes are 1N3064.

TEST CIRCUIT



TEST TABLE (See Note 5)

TEST NO.	OUTPUT UNDER TEST	APPLY INPUT $\overline{Y}$ TO	APPLY INPUT Y TO	APPLY +2.4 V TO	APPLY GND TO	APPLY OUTPUT LOADING TO
1	$\overline{C_{n+1}}$	None	C_n	None	B_1	$\overline{C_{n+1}}$ (N = 5)
2	$\overline{C_{n+1}}$	None	C_n	None	B_1	$\overline{C_{n+1}}$ (N = 5)
3	$\overline{C_{n+1}}$	B_c	None	C_n	A_1, B_1	$\overline{C_{n+1}}$ (N = 5)
4	$\overline{C_{n+1}}$	B_c	None	C_n	A_1, B_1	$\overline{C_{n+1}}$ (N = 5)
5	Σ	A_c	None	C_n	A_1, B_1	Σ (N = 10) $\overline{\Sigma}$ (N = 10) $\overline{C_{n+1}}$ (N = 5)
6	Σ	A_c	None	C_n	A_1, B_1	Σ (N = 10) $\overline{\Sigma}$ (N = 10) $\overline{C_{n+1}}$ (N = 5)
7	$\overline{\Sigma}$	B_c	None	C_n	B_1	$\overline{\Sigma}$ (N = 10)
8	$\overline{\Sigma}$	B_c	None	C_n	B_1	$\overline{\Sigma}$ (N = 10)
9	A★	None	A_1	A_2	None	A★ (C_L = 15 pF)
10	A★	None	A_1	A_2	None	A★ (C_L = 15 pF)
11	B★	None	B_1	B_2	None	B★ (C_L = 15 pF)
12	B★	None	B_1	B_2	None	B★ (C_L = 15 pF)



VOLTAGE WAVEFORMS

FIGURE 9 – SWITCHING TIMES

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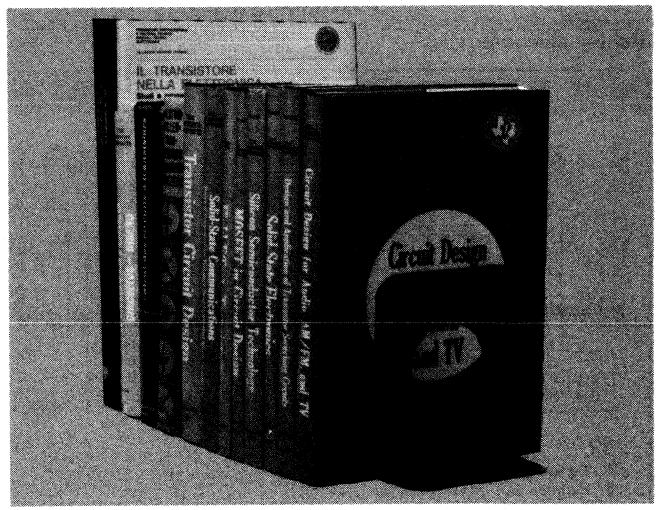

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- Control Systems

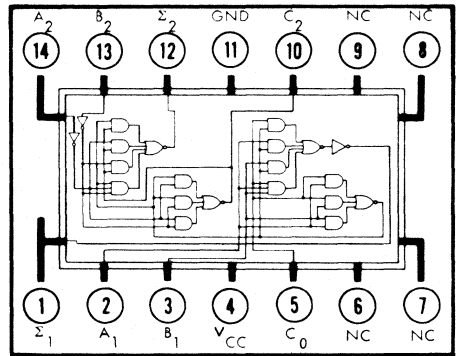
logic

TRUTH TABLE

INPUT				OUTPUT					
				WHEN $C_0 = 0$			WHEN $C_0 = 1$		
A_1	B_1	A_2	B_2	Σ_1	Σ_2	C_2	Σ_1	Σ_2	C_2
0	0	0	0	0	0	0	1	0	0
1	0	0	0	1	0	0	0	1	0
0	1	0	0	1	0	0	0	1	0
1	1	0	0	0	1	0	1	1	0
0	0	1	0	0	1	0	1	1	0
1	0	1	0	1	1	0	0	0	1
0	1	1	0	1	1	0	0	0	1
1	1	1	0	0	0	1	1	0	1
0	0	0	1	0	1	0	1	1	0
1	0	0	1	1	1	0	0	0	1
0	1	0	1	1	1	0	0	0	1
1	1	0	1	0	0	1	1	0	1
0	0	1	1	0	0	1	1	0	1
1	0	1	1	1	0	1	0	1	1
0	1	1	1	1	0	1	0	1	1
1	1	1	1	0	1	1	1	1	1

S

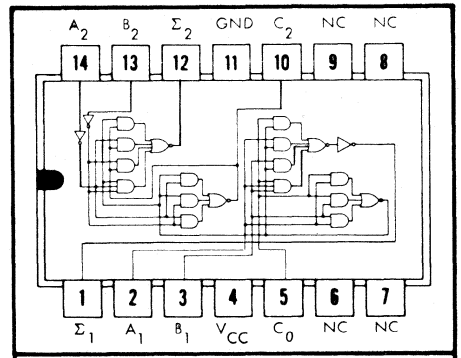
FLAT PACKAGE (TOP VIEW)



positive logic: see truth table

J OR N

DUAL-IN-LINE PACKAGE (TOP VIEW)



positive logic: see truth table

NC—No Internal Connection

description

This full adder performs the addition of two 2-bit binary numbers. The sum (Σ) outputs are provided for each bit and the resultant carry (C_2) is obtained from the second bit. Designed for medium-to-high-speed, multiple-bit, parallel-add/serial-carry applications, the circuit utilizes high-speed, high-fan-out transistor-transistor logic (TTL) but is compatible with both DTL and TTL logic families. The implementation of a single-inversion, high-speed, Darlington-connected serial-carry circuit within each bit minimizes the necessity for extensive "look-ahead" and carry-cascading circuits. The power dissipation level has been maintained considerably below that attainable with equivalent standard integrated circuits connected to perform full-adder functions.

absolute maximum ratings (over operating temperature range unless otherwise noted)

Supply Voltage V_{CC} (See Note 1) . . . . . 7 V
Input Voltage, V_{in} (See Notes 1 and 2) . . . . . 5.5 V
Operating Case Temperature Range: SN5482S . . . . . −55°C to 125°C
Operating Free-Air Temperature Range: SN5482J, SN5482N . . . . . −55°C to 125°C
SN7482 Circuits . . . . . 0°C to 70°C
Storage Temperature Range . . . . . −65°C to 150°C

NOTES: 1. These voltage values are with respect to network ground terminal.
2. Input signals must be zero or positive with respect to network ground terminal.

recommended operating conditions (over operating temperature range)

	MIN	NOM	MAX	UNIT
Supply Voltage V_{CC} (See Note 1): SN5482 Circuits	4.5	5	5.5	V
SN7482 Circuits	4.75	5	5.25	V
Normalized Fan-Out From Outputs:				
C_2			5	
Σ_1 or Σ_2			10	

electrical characteristics (over operating temperature range unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
$V_{in(1)}$	Input voltage required to ensure logical 1 at any input terminal	1 and 2	V_{CC} = MIN		2			V
$V_{in(0)}$	Input voltage required to ensure logical 0 at any input terminal	1 and 2	V_{CC} = MIN				0.8	V
$V_{out(1)}$	Logical 1 output voltage	2	V_{CC} = MIN		2.4			V
$V_{out(0)}$	Logical 0 output voltage	1	V_{CC} = MIN				0.4	V
$I_{in(0)}$	Logical 0 level input current at A_1, B_1, or C_0	3	V_{CC} = MAX, V_{in} = 0.4 V				−6.4	mA
$I_{in(0)}$	Logical 0 level input current at A_2 or B_2	3	V_{CC} = MAX, V_{in} = 0.4 V				−1.6	mA
$I_{in(1)}$	Logical 1 level input current at A_1, B_1, or C_0	3	V_{CC} = MAX, V_{in} = 2.4 V				160	μA
			V_{CC} = MAX, V_{in} = 5.5 V				1	mA
$I_{in(1)}$	Logical 1 level input current at A_2 or B_2	3	V_{CC} = MAX, V_{in} = 2.4 V				40	μA
			V_{CC} = MAX, V_{in} = 5.5 V				1	mA
I_{OS}	Short-circuit output current at Σ_1 or Σ_2 §	4	V_{CC} = MAX	SN5482	−20		−55	mA
				SN7482	−18		−55	mA
I_{OS}	Short-circuit output current at C_2 §	4	V_{CC} = MAX	SN5482	−20		−70	mA
				SN7482	−18		−70	mA
I_{CC}	Supply Current	3	V_{CC} = MAX	SN5482		35	50	mA
				SN7482		35	58	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ Not more than one output should be shorted at a time.

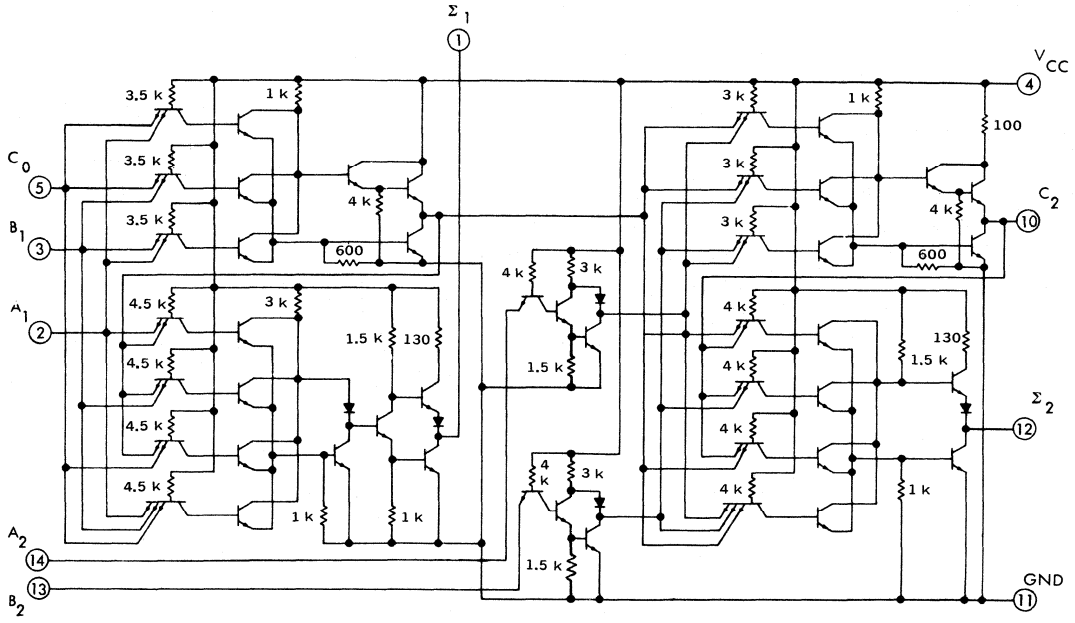
–SEE ORDERING INSTRUCTIONS PAGE 1-1–

switching characteristics, V_{CC} = 5 V, T_A = 25°C (unless otherwise noted N = 10)

PARAMETER§	FROM (INPUT)	TO (OUTPUT)	FIGURE 5 TEST NO.	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{pd1}	C_0	Σ_1	1	C_L = 15 pF, R_L = 400 Ω			34	ns
t_{pd0}			2	C_L = 15 pF, R_L = 400 Ω			40	ns
t_{pd1}	B_2	Σ_2	3	C_L = 15 pF, R_L = 400 Ω			40	ns
t_{pd0}			4	C_L = 15 pF, R_L = 400 Ω			35	ns
t_{pd1}	C_0	Σ_2	5	C_L = 15 pF, R_L = 400 Ω			38	ns
t_{pd0}			6	C_L = 15 pF, R_L = 400 Ω			42	ns
t_{pd1}	C_0	C_2	7	C_L = 15 pF, R_L = 400 Ω		17	27	ns
t_{pd0}			8	C_L = 15 pF, R_L = 400 Ω		12	19	ns

§ t_{pd1} is propagation delay time to logical 1 level. t_{pd0} is propagation delay time to logical 0 level.

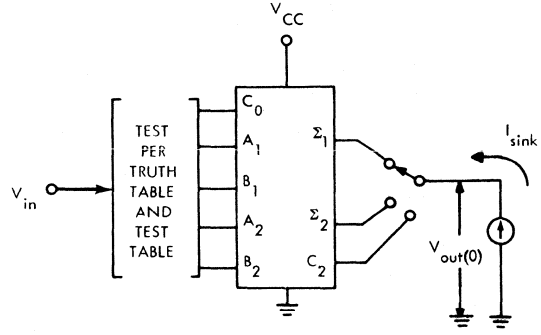
schematic



Component values shown are nominal.
Resistor values are in ohms.

PARAMETER MEASUREMENT INFORMATION

d-c test circuits†

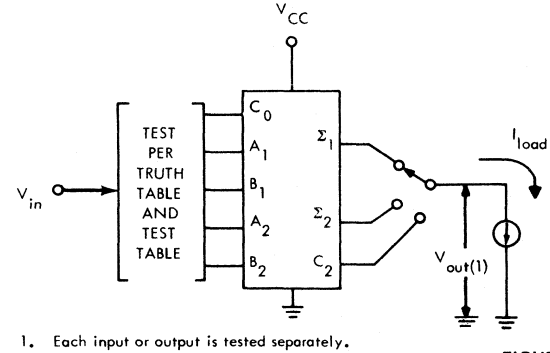


1. Each input or output is tested separately.

TEST TABLE

OUTPUT UNDER TEST	I_{sink}
Σ_1 or Σ_2	16 mA
C_2	8 mA

FIGURE 1



1. Each input or output is tested separately.

TEST TABLE

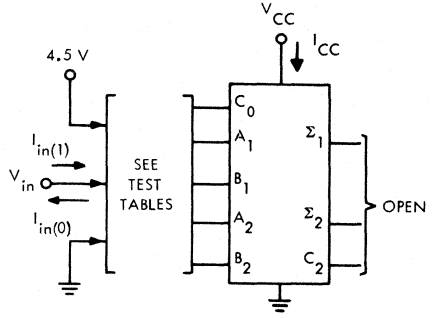
OUTPUT UNDER TEST	I_{load}
Σ_1 or Σ_2	−400 μA
C_2	−200 μA

FIGURE 2

†Arrows indicate actual direction of current flow.

PARAMETER MEASUREMENT INFORMATION

d-c test circuits† (continued)



$I_{in(0)}$ TEST TABLE

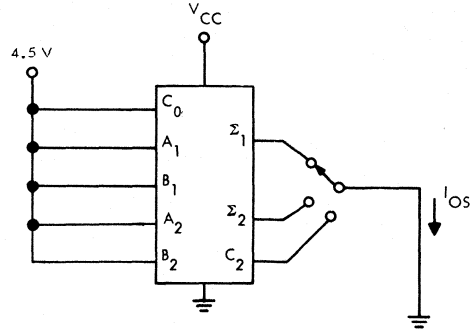
APPLY V_{in} TEST I_{in}	APPLY 4.5 V
C_0	A_1 and B_1
A_1	C_0 and B_1
B_1	C_0 and A_1
A_2	None
B_2	None

$I_{in(1)}$ TEST TABLE

APPLY V_{in} TEST I_{in}	GND
C_0	A_1 and B_1
A_1	C_0 and B_1
B_1	C_0 and A_1
A_2	None
B_2	None

1. Each input is tested separately.
2. When testing I_{CC} apply 4.5 V to A_1, A_2, and C_0; and ground B_1 and B_2.

FIGURE 3



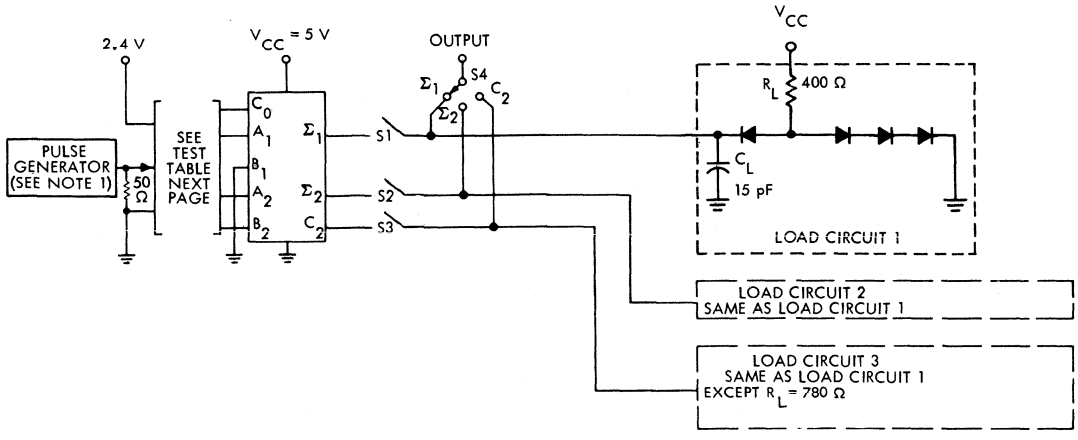
1. Each output is tested separately.

FIGURE 4

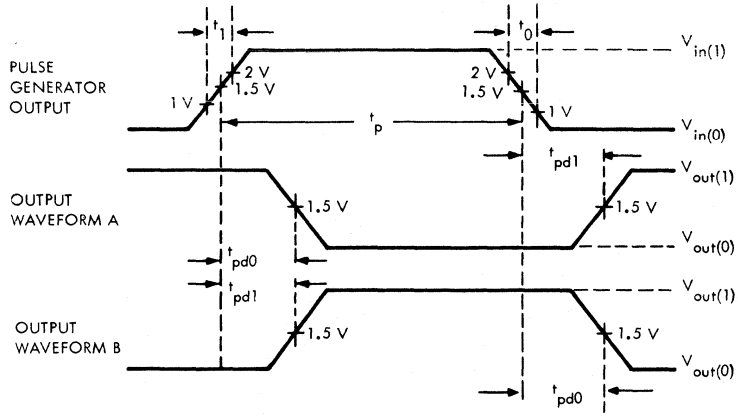
†Arrows indicate actual direction of current flow.

PARAMETER MEASUREMENT INFORMATION

switching characteristics



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES:
1. The generator has the following characteristics: $V_{in(1)} \geq 2.4$ V, $V_{in(0)} \leq 0.4$ V, t_1 = 8 to 15 ns, t_0 = 3 to 5 ns, PRR = 1 MHz, t_p = 200ns, and $Z_{out} \approx 50\ \Omega$.
2. Perform test in accordance with test table.
3. Each output is tested separately.
4. Voltage values are with respect to network ground terminal.
5. C_L includes probe and jig capacitance.
6. All diodes are 1N3064.

FIGURE 5–SWITCHING TIMES

PARAMETER MEASUREMENT INFORMATION

switching characteristics (continued)

SWITCHING TIMES TEST TABLE (SEE NOTE 7)

TEST NO.	PARAMETER	APPLY PULSE GENERATOR OUTPUT TO	OUTPUT UNDER TEST (S4)	APPLY 2.4 V TO	APPLY GND TO	S1	S2	S3
1	t_{pd1}	C_0	Σ_1 (WAVEFORM A)	A_1	A_2, B_1, B_2	CLOSED	OPEN	OPEN
2	t_{pd0}							
3	t_{pd1}	B_2	Σ_2 (WAVEFORM B)	None	A_1, B_1, A_2 and C_0	OPEN	CLOSED	OPEN
4	t_{pd0}							
5	t_{pd1}	C_0	Σ_2 (WAVEFORM A)	A_1, A_2	B_1, B_2	OPEN	CLOSED	CLOSED
6	t_{pd0}							
7	t_{pd1}	C_0	C_2 (WAVEFORM B)	A_1, A_2	B_1, B_2	OPEN	OPEN	CLOSED
8	t_{pd0}							

NOTE 7: Inputs and outputs not otherwise specified are open.

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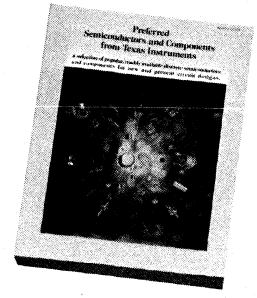
... in Discretes the Trend is Preferred Semiconductors



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HIGH-SPEED TTL 4-BIT FULL ADDERS FOR APPLICATION IN

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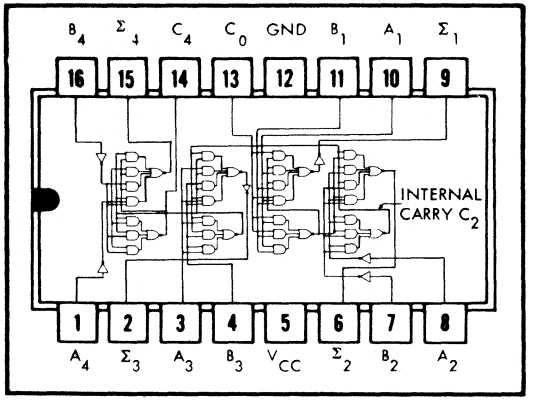
- Control Systems

logic

INPUT				OUTPUT					
				WHEN $C_0 = 0$			WHEN $C_0 = 1$		
				WHEN $C_2 = 0$			WHEN $C_2 = 1$		
A_1 / A_3	B_1 / B_3	A_2 / A_4	B_2 / B_4	Σ_1 / Σ_3	Σ_2 / Σ_4	C_2 / C_4	Σ_1 / Σ_3	Σ_2 / Σ_4	C_2 / C_4
0	0	0	0	0	0	0	1	0	0
1	0	0	0	1	0	0	0	1	0
0	1	0	0	1	0	0	0	1	0
1	1	0	0	0	1	0	1	1	0
0	0	1	0	0	1	0	1	1	0
1	0	1	0	1	1	0	0	0	1
0	1	1	0	1	1	0	0	0	1
1	1	1	0	0	0	1	1	0	1
0	0	0	1	0	1	0	1	1	0
1	0	0	1	1	1	0	0	0	1
0	1	0	1	1	1	0	0	0	1
1	1	0	1	0	0	1	1	0	1
0	0	1	1	0	0	1	1	0	1
1	0	1	1	1	0	1	0	1	1
0	1	1	1	1	0	1	0	1	1
1	1	1	1	0	1	1	1	1	1

NOTE 1: Input conditions at A_1, A_2, B_1, B_2, and C_0 are used to determine outputs Σ_1 and Σ_2, and the value of the internal carry C_2. The values at C_2, A_3, B_3, A_4, and B_4, are then used to determine outputs Σ_3, Σ_4, and C_4.

J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



description

This full adder performs the addition of two 4-bit binary numbers. The sum (Σ) outputs are provided for each bit and the resultant carry (C_4) is obtained from the fourth bit. Designed for medium-to-high-speed, multiple-bit, parallel-add/serial-carry applications, the circuit utilizes high-speed, high-fan-out transistor-transistor logic (TTL) but is compatible with both DTL and TTL families. The implementation of a single-inversion, high-speed, Darlington-connected serial-carry circuit within each bit minimizes the necessity for extensive "look-ahead" and carry-cascading circuits. The power dissipation level has been maintained considerably below that attainable with equivalent standard integrated circuits connected to perform four-bit full-adder functions.

absolute maximum ratings (over operating temperature range unless otherwise noted)

Supply Voltage V_{CC} (See Note 1) . . . . . 7 V
Input Voltage, V_{in} (See Notes 1 and 2) . . . . . 5.5 V
Operating Free-Air Temperature Range: SN5483 Circuits . . . . . −55°C to 125°C
SN7483 Circuits . . . . . 0°C to 70°C
Storage Temperature Range . . . . . −65°C to 150°C

NOTES: 1. These voltage values are with respect to network ground terminal.
2. Input signals must be zero or positive with respect to network ground terminal.

recommended operating conditions (over operating temperature range)

		MIN	NOM	MAX	UNIT
Supply Voltage V_{CC}: (See Note 1)	SN5483 Circuits	4.5	5	5.5	V
	SN7483 Circuits	4.75	5	5.25	V
Normalized Fan-Out From Outputs:					
C_4				5	
$\Sigma_1, \Sigma_2, \Sigma_3$ or Σ_4				10	

electrical characteristics (over operating temperature range unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
$V_{in(1)}$	Input voltage required to ensure logical 1 at any input terminal	1 and 2	V_{CC} = MIN		2			V
$V_{in(0)}$	Input voltage required to ensure logical 0 at any input terminal	1 and 2	V_{CC} = MIN				0.8	V
$V_{out(1)}$	Logical 1 output voltage	2	V_{CC} = MIN		2.4			V
$V_{out(0)}$	Logical 0 output voltage	1	V_{CC} = MIN				0.4	V
$I_{in(0)}$	Logical 0 level input current at A_1, A_3, B_1, B_3, or C_0	3	V_{CC} = MAX,	V_{in} = 0.4 V			−6.4	mA
$I_{in(0)}$	Logical 0 level input current at A_2, A_4, B_2, or B_4	3	V_{CC} = MAX,	V_{in} = 0.4 V			−1.6	mA
$I_{in(1)}$	Logical 1 level input current at A_1, A_3, B_1, B_3, or C_0	3	V_{CC} = MAX,	V_{in} = 2.4 V			160	μA
			V_{CC} = MAX,	V_{in} = 5.5 V			1	mA
$I_{in(1)}$	Logical 1 level input current at A_2, A_4, B_2, or B_4	3	V_{CC} = MAX,	V_{in} = 2.4 V			40	μA
			V_{CC} = MAX,	V_{in} = 5.5 V			1	mA
I_{OS}	Short-circuit output current at $\Sigma_1, \Sigma_2, \Sigma_3$, or Σ_4§	4	V_{CC} = MAX	SN 5483	−20		−55	mA
				SN7483	−18		−55	mA
I_{OS}	Short-circuit output current at C_4§	4	V_{CC} = MAX	SN5483	−20		−70	mA
				SN7483	−18		−70	mA
I_{CC}	Supply Current	3	V_{CC} = MAX,	SN5483		78	110	mA
				SN7483		78	128	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

§ Not more than one output should be shorted at a time.

—SEE ORDERING INSTRUCTIONS PAGE 1-1—

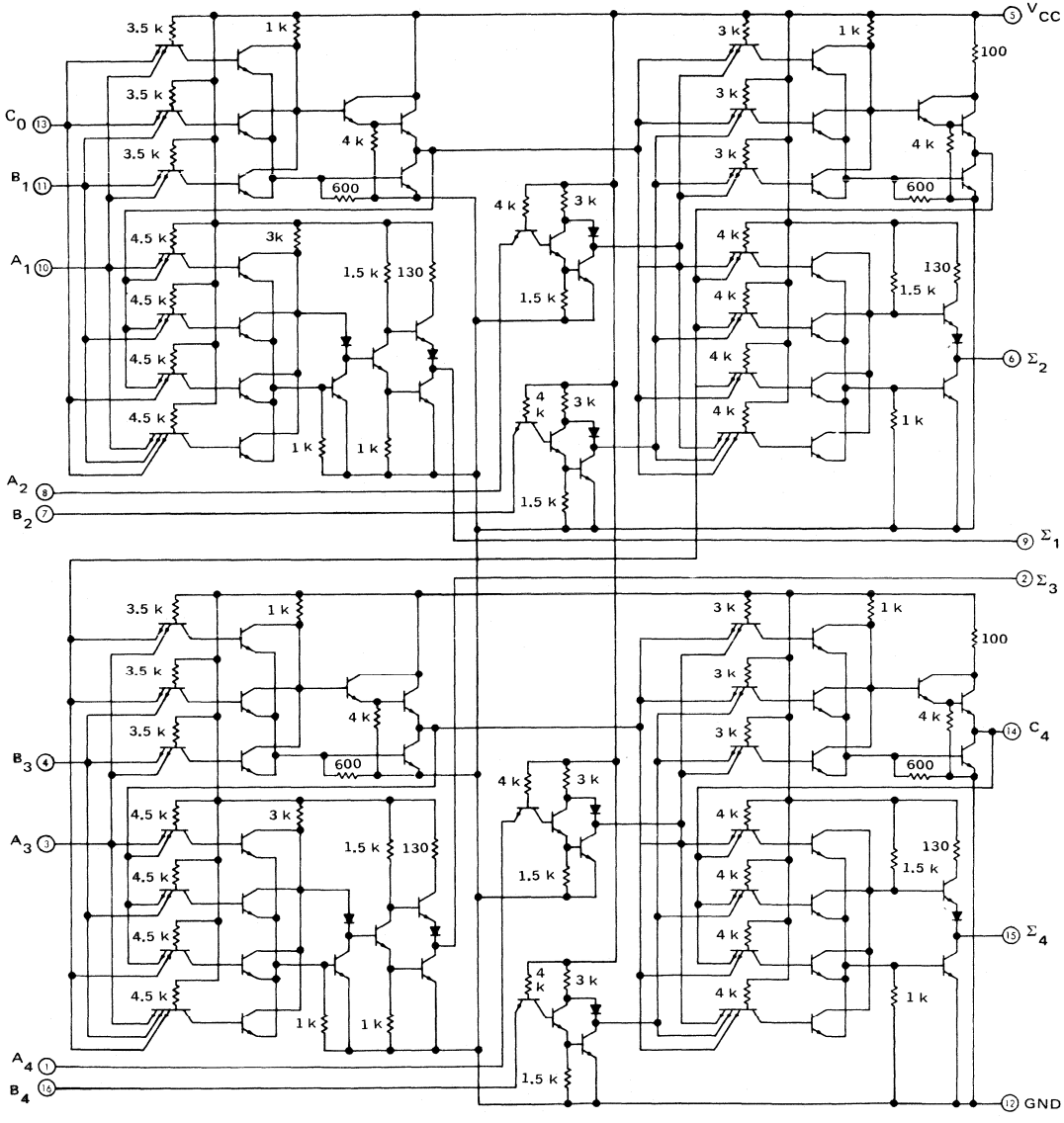
switching characteristics, V_{CC} = 5 V, T_A = 25°C (unless otherwise noted N = 10)

PARAMETER§	FROM (INPUT)	TO (OUTPUT)	FIGURE 5 TEST NO.	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{pd1}	C_0	1	1	C_L = 15 pF, R_L = 400 Ω			34	ns
t_{pd0}			2	C_L = 15 pF. R_L = 400 Ω			40	ns
t_{pd1}	C_0	2	3	C_L = 15 pF, R_L = 400 Ω			38	ns
t_{pd0}			4	C_L = 15 pF, R_L = 400 Ω			42	ns
t_{pd1}	C_0	3	5	C_L = 15 pF, R_L = 400 Ω			50	ns
t_{pd0}			6	C_L = 15 pF, R_L = 400 Ω			60	ns
t_{pd1}	C_0	4	7	C_L = 15 pF, R_L = 400 Ω			55	ns
t_{pd0}			8	C_L = 15 pF, R_L = 400 Ω			55	ns
t_{pd1}	C_0	C_4	9	C_L = 15 pF, R_L = 780 Ω		35	48	ns
t_{pd0}			10	C_L = 15 pF, R_L = 780 Ω		22	32	ns
t_{pd1}	A_2 or B_2	2	11 and 13	C_L = 15 pF, R_L = 400 Ω			40	ns
t_{pd0}			12 and 14	C_L = 15 pF, R_L = 400 Ω			35	ns
t_{pd1}	A_4 or B_4	4	15 and 17	C_L = 15 pF, R_L = 400 Ω			40	ns
t_{pd0}			16 and 18	C_L = 15 pF, R_L = 400 Ω			35	ns

§ t_{pd1} is propagation delay time to logical 1 level. t_{pd0} is propagation delay time to logical 0 level.

–SEE ORDERING INSTRUCTIONS PAGE 1-1–

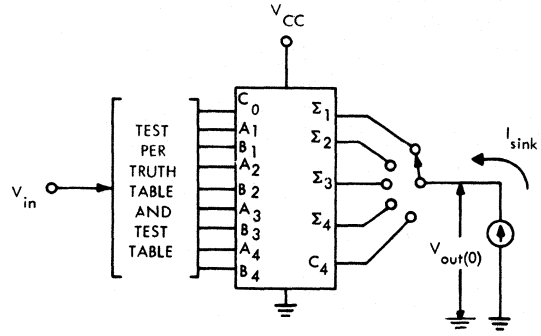
schematic



Component values shown are nominal.
Resistor values are in ohms.

PARAMETER MEASUREMENT INFORMATION

d-c test circuits†

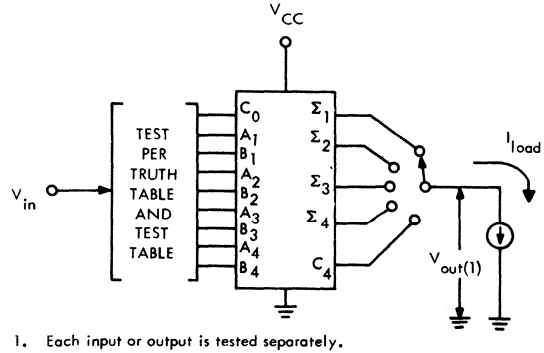


TEST TABLE

OUTPUT UNDER TEST	I_{sink}
Σ_1, Σ_2, Σ_3, or Σ_4	16 mA
C_4	8 mA

1. Each input or output is tested separately.

FIGURE 1



TEST TABLE

OUTPUT UNDER TEST	I_{load}
Σ_1, Σ_2, Σ_3, or Σ_4	− 400 μA
C_4	− 200 μA

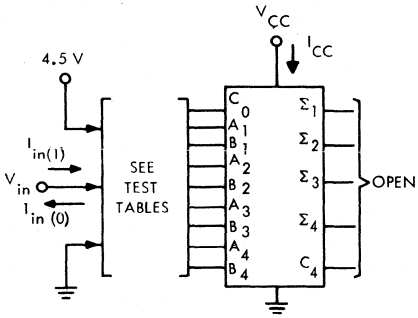
1. Each input or output is tested separately.

FIGURE 2

†Arrows indicate actual direction of current flow.

PARAMETER MEASUREMENT INFORMATION

d-c test circuits† (continued)



1. Each input is tested separately.
2. When testing I_{CC} apply 4.5 V to A_1, A_2, A_3, A_4, and C_0; and ground B_1, B_2, B_3 and B_4.

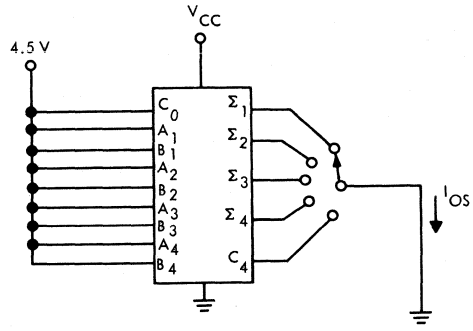
$I_{in(0)}$ TEST TABLE

APPLY V_{in} TEST I_{in}	APPLY 4.5 V
C_0	A_1 and B_1
A_1	C_0 and B_1
B_1	C_0 and A_1
A_2	None
B_2	None
A_3	A_2, B_2, and B_3
B_3	A_2, B_2, and A_3
A_4	None
B_4	None

$I_{in(1)}$ TEST TABLE

APPLY V_{in} TEST I_{in}	GND
C_0	A_1 and B_1
A_1	C_0 and B_1
B_1	C_0 and A_1
A_2	None
B_2	None
A_3	A_2, B_2, and B_3
B_3	A_2, B_2, and A_3
A_4	None
B_4	None

FIGURE 3



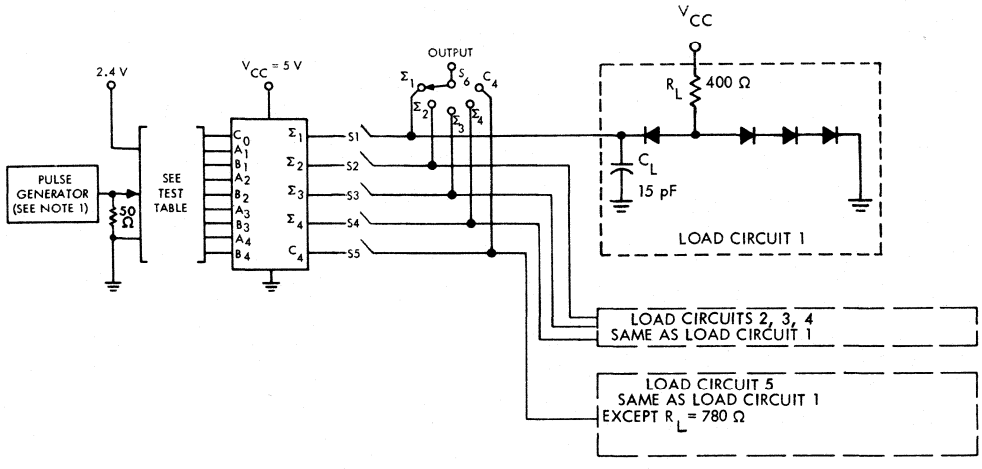
1. Each output is tested separately.

FIGURE 4

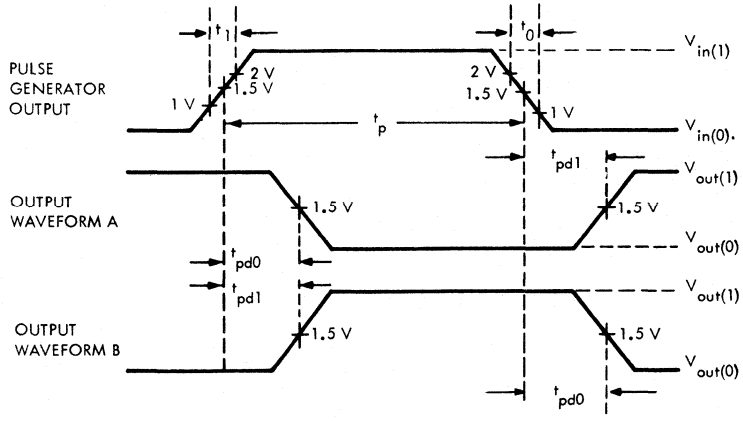
†Arrows indicate actual direction of current flow.

PARAMETER MEASUREMENT INFORMATION

switching characteristics



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES: 1. Pulse generator output pulse characteristics: $V_{in(1)} \geq$ 2.4 V, $V_{in(0)} \leq$ 0.4 V, t_1 = 8 to 15 ns, t_0 = 3 to 5 ns, PRR = 1 MHz, t_p = 200 ns, and $Z_{out} \approx$ 50 Ω.

2. Perform test in accordance with test table. (See sheet 2 of this figure.)
3. Each output is tested separately.
4. Voltage values are with respect to network ground terminal.
5. C_L includes probe and jig capacitance.
6. All diodes are 1N3064

FIGURE 5–SWITCHING TIMES (SHEET 1 OF 2)

PARAMETER MEASUREMENT INFORMATION

switching characteristics (continued)

TEST TABLE (SEE NOTE 7)

TEST NO.	PARA-METER	APPLY PULSE GENERATOR OUTPUT TO	OUTPUT UNDER TEST (S6)	APPLY 2.4 V TO	APPLY GND TO	S1	S2	S3	S4	S5
1	t_{pd1}	C_0	Σ_1 (WAVEFORM A)	A_1	B_1, A_2, and B_2	CLOSED	OPEN	OPEN	OPEN	OPEN
2	t_{pd0}									
3	t_{pd1}	C_0	Σ_2 (WAVEFORM A)	A_1 and A_2	B_1 and B_2	OPEN	CLOSED	OPEN	OPEN	OPEN
4	t_{pd0}									
5	t_{pd1}	C_0	Σ_3 (WAVEFORM A)	A_1, A_2, and A_3	B_1, B_2, and B_3	OPEN	OPEN	CLOSED	OPEN	OPEN
6	t_{pd0}									
7	t_{pd1}	C_0	Σ_4 (WAVEFORM A)	A_1, A_2, A_3, and A_4	B_1, B_2, B_3, and B_4	OPEN	OPEN	OPEN	CLOSED	CLOSED
8	t_{pd0}									
9	t_{pd1}	C_0	C_4 (WAVEFORM B)	A_1, A_2, A3, and A_4	B_1, B_2, B_3, and B_4	OPEN	OPEN	OPEN	OPEN	CLOSED
10	t_{pd0}									
11	t_{pd1}	A_2	Σ_2 (WAVEFORM B)	None	A_1, B_1, B_2, and C_0	OPEN	CLOSED	OPEN	OPEN	OPEN
12	t_{pd0}									
13	t_{pd1}	B_2	Σ_2 (WAVEFORM B)	None	A_1, B_1, A_2, and C_0	OPEN	CLOSED	OPEN	OPEN	OPEN
14	t_{pd0}									
15	t_{pd1}	A_4	Σ_4 (WAVEFORM B)	None	A_3, B_3, and B_4	OPEN	OPEN	OPEN	CLOSED	OPEN
16	t_{pd0}									
17	t_{pd1}	B_4	Σ_4 (WAVEFORM B)	None	A_3, B_3, and A_4	OPEN	OPEN	OPEN	CLOSED	OPEN
18	t_{pd0}									

NOTE 7: Inputs and outputs not otherwise specified are open.

FIGURE 5 – SWITCHING TIMES (SHEET 2 of 2)

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

CIRCUIT TYPES SN5486, SN7486
QUADRUPLE 2-INPUT EXCLUSIVE-OR GATES

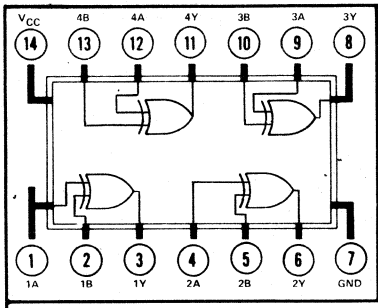
- Input-Clamping Diodes Simplify System Design
- Fully Compatible with TTL, DTL, and Other MSI Circuits
- Typical Propagation Delay Times: 12 ns

logic

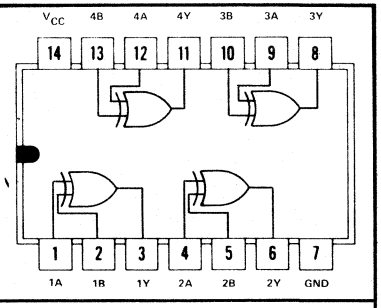
TRUTH TABLE

INPUTS		OUTPUT
A	B	Y
0	0	0
0	1	1
1	0	1
1	1	0

S
FLAT PACKAGE (TOP VIEW)



J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



positive logic: $Y = A \oplus B$

description

Each of these monolithic, quadruple 2-input exclusive-OR gates utilize TTL circuitry to perform the function: $Y = A\bar{B} + \bar{A}B$. When the input states are complementary, the output goes to a logical 1.

These circuits are fully compatible for use with other TTL or DTL circuits. Input clamping diodes are provided to minimize transmission line effects and thereby simplify system design. Input buffers are used to lower the fan-in requirement to only one normalized series 54/74 load. A full fan-out to 10 normalized series 54/74 loads is available from each of the outputs in the logical 0 state. A fan-out of 20 is provided in the logical 1 state to facilitate connection of unused inputs to used inputs. Propagation delay is 12 nanoseconds and power dissipation is 37.5 milliwatts typically for each exclusive-OR function.

The SN5486 is characterized for operation over the full military temperature range of −55°C to 125°C and the SN7486 is characterized for operation from 0°C to 70°C.

absolute maximum ratings (over operating temperature range unless otherwise noted)

Supply Voltage V_{CC} (See Note 1)	7 V
Input Voltage, V_{in} (See Note 1)	5.5 V
Operating Case Temperature Range: SN5486S	−55°C to 125°C
Operating Free-Air Temperature Range: SN5486J, SN5486N	−55°C to 125°C
SN7486 Circuits	0°C to 70°C
Storage Temperature Range	−65°C to 150°C

NOTE 1: These voltage values are with respect to network ground terminal.

recommended operating conditions (over operating temperature range)

	MIN	NOM	MAX	UNIT
Supply Voltage V_{CC} (See Note 1): SN5486 Circuits	4.5	5	5.5	V
SN7486 Circuits	4.75	5	5.25	V
Normalized Fan-out from each output, N: Logical 0			10	
Logical 1			20	

electrical characteristics (over operating temperature range unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS †		MIN	TYP ‡	MAX	UNIT
$V_{in(1)}$	Input voltage required to ensure logical 1 at any input terminal	1	V_{CC} = MIN		2			V
$V_{in(0)}$	Input voltage required to ensure logical 0 at any input terminal	1	V_{CC} = MIN				0.8	V
$V_{out(1)}$	Logical 1 output voltage	1	V_{CC} = MIN, $V_{in(1)}$ = 2 V, $V_{in(0)}$ = 0.8 V, I_{load} = −800 μA		2.4			V
$V_{out(0)}$	Logical 0 output voltage	2	V_{CC} = MIN, $V_{in(1)}$ = 2 V, $V_{in(0)}$ = 0.8 V, I_{sink} = 16 mA				0.4	V
$I_{in(1)}$	Logical 1 level input current (each input)	3	V_{CC} = MAX, V_{in} = 2.4 V				40	μA
			V_{CC} = MAX, V_{in} = 5.5 V				1	mA
$I_{in(0)}$	Logical 0 level input current (each input)	4	V_{CC} = MAX, V_{in} = 0.4 V				−1.6	mA
I_{OS}	Short circuit output current §	5	V_{CC} = MAX, $V_{in(1)}$ = 4.5 V, $V_{in(0)}$ = 0	SN5486	−20		−55	mA
				SN7486	−18		−55	mA
I_{CC}	Supply current	6	V_{CC} = MAX, V_{in} = 4.5 V	SN5486		30	43	mA
				SN7486		30	50	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable circuit type.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ Not more than one output should be shorted at a time.

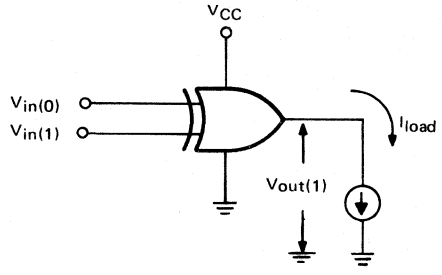
switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{pd0}	Propagation delay time to logical 0 level (other input low)	7	C_L = 15 pF, R_L = 400 Ω		11	17	ns
t_{pd1}	Propagation delay time to logical 1 level (other input low)	7	C_L = 15 pF, R_L = 400 Ω		15	23	ns
t_{pd0}	Propagation delay time to logical 0 level (other input high)	7	C_L = 15 pF, R_L = 400 Ω		13	22	ns
t_{pd1}	Propagation delay time to logical 1 level (other input high)	7	C_L = 15 pF, R_L = 400 Ω		18	30	ns

—SEE ORDERING INSTRUCTIONS PAGE 1-1—

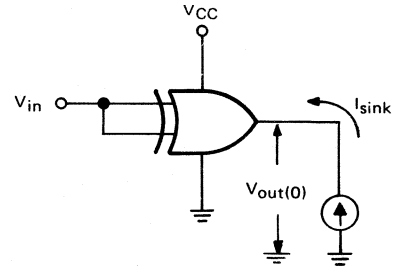
PARAMETER MEASUREMENT INFORMATION

d-c test circuits†



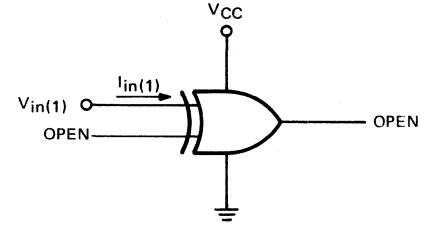
1. Each input is tested separately.

FIGURE 1



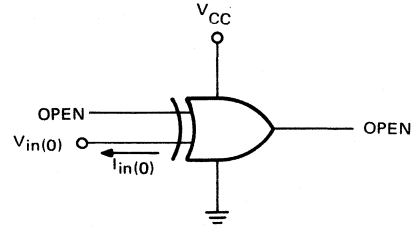
1. Logical 0 and logical 1 input conditions are tested.

FIGURE 2



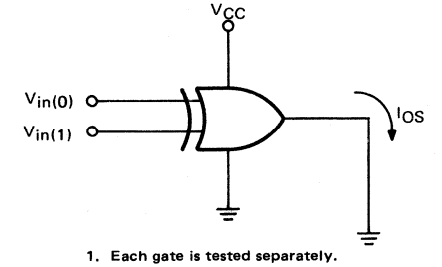
1. Each input is tested separately.

FIGURE 3



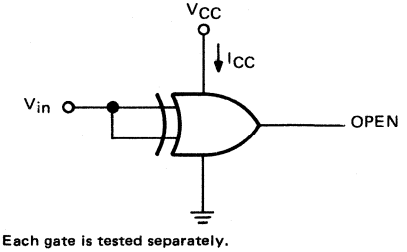
1. Each input is tested separately.

FIGURE 4



1. Each gate is tested separately.

FIGURE 5



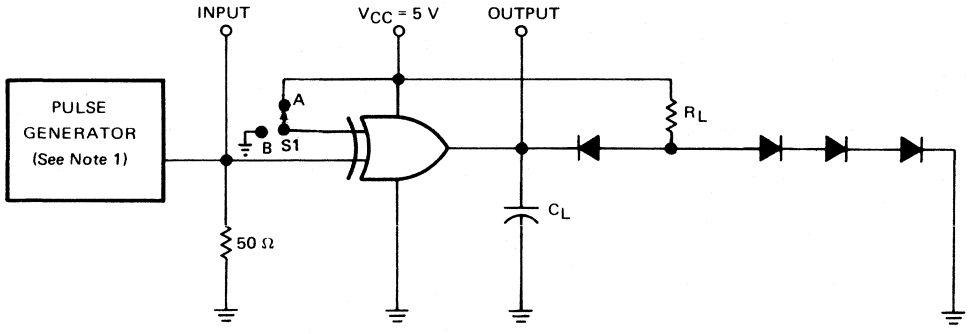
1. Each gate is tested separately.
2. Logical 0 and logical 1 input conditions are tested.

FIGURE 6

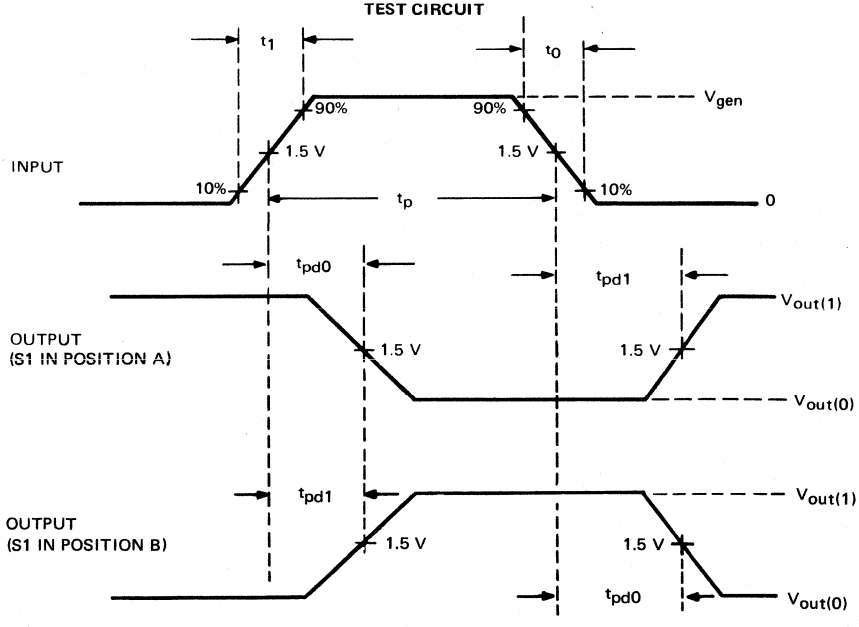
† Arrows indicate actual direction of current flow.

PARAMETER MEASUREMENT INFORMATION

switching characteristics



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES: 1. The generator has the following characteristics: V_{gen} = 3 V, $t_0 = t_1 \leqslant 15$ ns, t_p = 0.5 μs, PRR = 1 MHz, $Z_{out} \approx 50\ \Omega$.
2. All diodes are 1N3064
3. $t_{pd} = \dfrac{t_{pd0} + t_{pd1}}{2}$
4. C_L includes probe and jig capacitance.
5. Each gate tested separately.

FIGURE 7

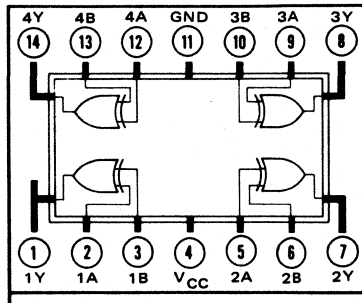
TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

CIRCUIT TYPES SN54L86, SN74L86
QUADRUPLE 2-INPUT EXCLUSIVE-OR GATES

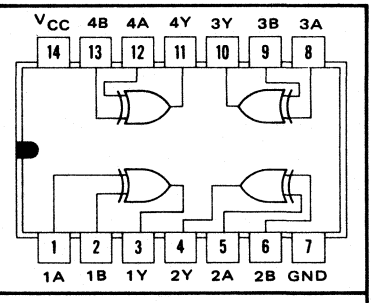
- Fully Compatible with TTL, DTL, and Other MSI Circuits
- Typical Propagation Delay Time: 43 ns

logic

T
FLAT PACKAGE (TOP VIEW)



J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



positive logic: $Y = A \oplus B$

TRUTH TABLE

INPUTS		OUTPUT
A	B	Y
0	0	0
0	1	1
1	0	1
1	1	0

description

Each of these low-power, monolithic, quadruple 2-input exclusive-OR gates utilize TTL circuitry to perform the function: $Y = A\overline{B} + \overline{A}B$. When the input states are complementary the output goes to a logical 1.

These circuits are fully compatible for use with other TTL or DTL circuits. A full fan-out to 10 series 54L/74L loads is available from each of the outputs. Typical power dissipation is 3.75 milliwatts for each exclusive-OR function.

The SN54L86 is characterized for operation over the full military temperature range of −55°C to 125°C and the SN74L86 is characterized for operation from 0°C to 70°C.

absolute maximum ratings (over operating free-air temperature range unless otherwise noted)

Supply Voltage V_{CC} (See Note 1) . . . . . 8 V
Input Voltage, V_{in} (See Note 1) . . . . . 5.5 V
Operating Free-Air Temperature Range: SN54L86 Circuits . . . . . −55°C to 125°C
SN74L86 Circuits . . . . . 0°C to 70°C
Storage Temperature Range . . . . . −65°C to 150°C

NOTE 1: These voltage values are with respect to network ground terminal.

recommended operating conditions (over operating temperature range)

	MIN	NOM	MAX	UNIT
Supply Voltage V_{CC} (See Note 1): SN54L86	4.5	5	5.5	V
SN74L86	4.75	5	5.25	V
Normalized Fan-out from each output, N			10	

electrical characteristics (over operating free-air temperature range unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS†	MIN	TYP‡	MAX	UNIT
$V_{in(1)}$	Input voltage required to ensure logical 1 at any input terminal	1	V_{CC} = MIN	2			V
$V_{in(0)}$	Input voltage required to ensure logical 0 at any input terminal	1	V_{CC} = MIN			0.7	V
$V_{out(1)}$	Logical 1 output voltage	1	V_{CC} = MIN, $V_{in(1)}$ = 2 V, $V_{in(0)}$ = 0.7 V, I_{load} = −100 μA	2.4			V
$V_{out(0)}$	Logical 0 output voltage	2	V_{CC} = MIN, $V_{in(1)}$ = 2 V, $V_{in(0)}$ = 0.7 V, I_{sink} = 2 mA			0.3	V
$I_{in(1)}$	Logical 1 level input current (each input)	3	V_{CC} = MAX, V_{in} = 2.4 V			20	μA
			V_{CC} = MAX, V_{in} = 5.5 V			200	μA
$I_{in(0)}$	Logical 0 level input current (each input)	4	V_{CC} = MAX, V_{in} = 0.3 V			−0.36	mA
I_{OS}	Short circuit output current	5	V_{CC} = MAX, $V_{in(1)}$ = 4.5 V, $V_{in(0)}$ = 0	−3		−15	mA
$I_{CC(0)}$	Supply current	6	V_{CC} = MAX, V_{in} = 4.5 V			1.67	mA
$I_{CC(1)}$	Supply current	5	V_{CC} = MAX $V_{in(1)}$ = 4.5 V, $V_{in(0)}$ = 0			1.1	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable circuit type.

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

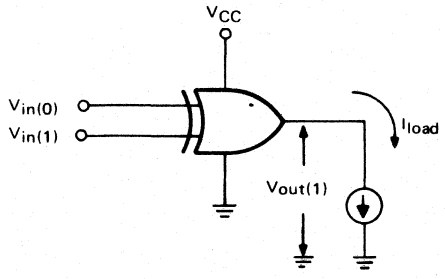
switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{pd0}	Propagation delay time to logical 0 level (other input low)	7	C_L = 50 pF, R_L = 4 kΩ		60	150	ns
t_{pd1}	Propagation delay time to logical 1 level (other input low)	7	C_L = 50 pF, R_L = 4 kΩ		75	150	ns
t_{pd0}	Propagation delay time to logical 0 level (other input high)	7	C_L = 50 pF, R_L = 4 kΩ		35	60	ns
t_{pd1}	Propagation delay time to logical 1 level (other input high)	7	C_L = 50 pF, R_L = 4 kΩ		50	90	ns

–SEE ORDERING INSTRUCTIONS PAGE 1-1–

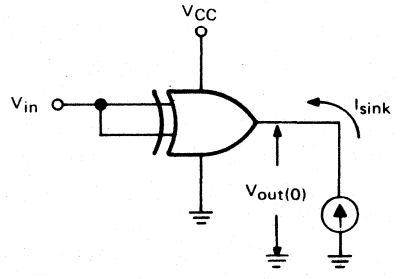
PARAMETER MEASUREMENT INFORMATION

d-c test circuits†



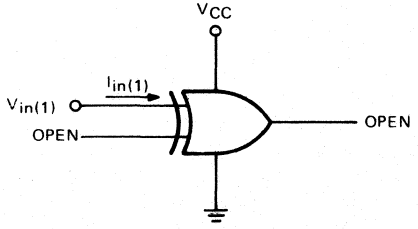
1. Each input is tested separately.

FIGURE 1



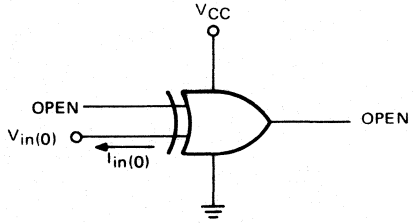
1. Logical 0 and logical 1 input conditions are tested.

FIGURE 2



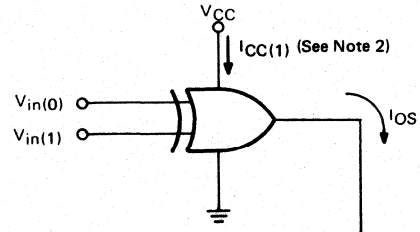
1. Each input is tested separately.

FIGURE 3



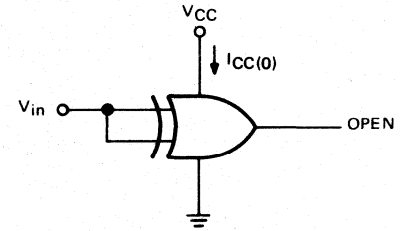
1. Each input is tested separately.

FIGURE 4



1. Each gate is tested separately.
2. When testing $I_{CC(1)}$, the output is open.

FIGURE 5



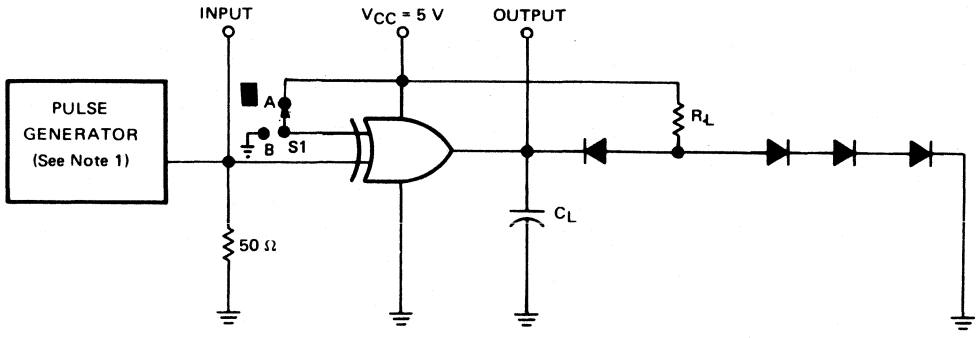
1. Each gate is tested separately.
2. Logical 0 and logical 1 input conditions are tested.

FIGURE 6

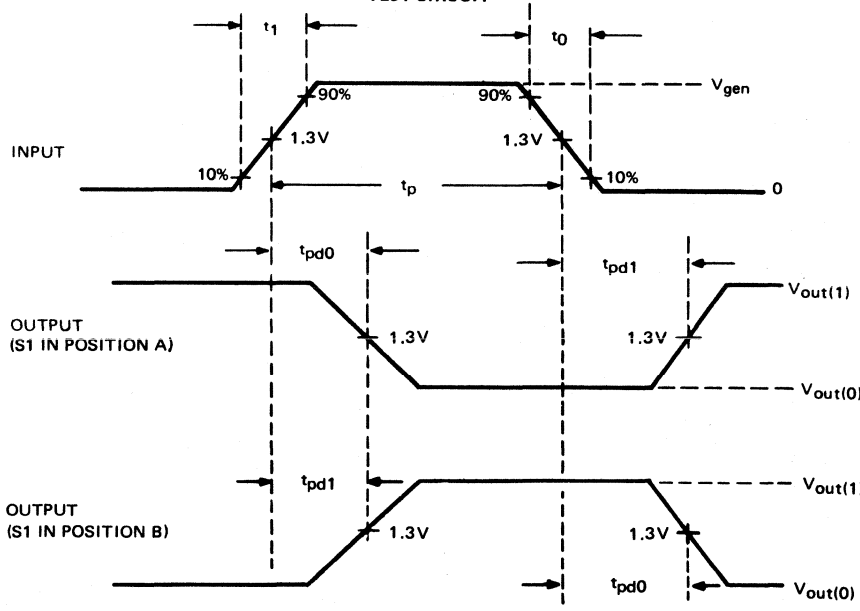
†Arrows indicate actual direction of current flow.

PARAMETER MEASUREMENT INFORMATION

switching characteristics



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES: 1. The generator has the following characteristics: V_{gen} = 3 V, $t_0 = t_1 \leq 15$ ns, t_p = 0.5 μs, PRR = 1 MHz, $Z_{out} \approx 50\ \Omega$.
2. All diodes are 1N916.
3. $t_{pd} = \dfrac{t_{pd0} + t_{pd1}}{2}$
4. C_L includes probe and jig capacitance.
5. Each gate tested separately.

FIGURE 7.

TEXAS INSTRUMENTS
INCORPORATED
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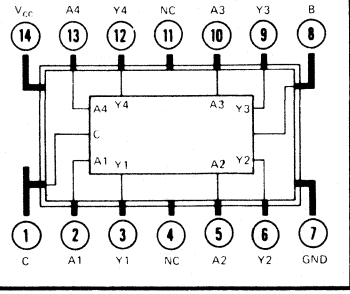
CIRCUIT TYPES SN54H87, SN74H87
4-BIT TRUE/COMPLEMENT, ZERO/ONE ELEMENT

logic

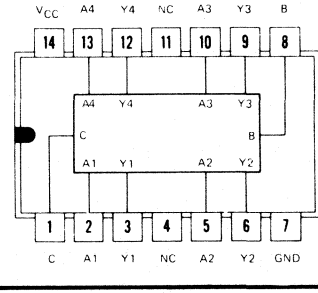
TRUTH TABLE

CONTROL INPUTS		OUTPUT			
B	C	Y1	Y2	Y3	Y4
0	0	$\overline{A1}$	$\overline{A2}$	$\overline{A3}$	$\overline{A4}$
0	1	1	1	1	1
1	0	A1	A2	A3	A4
1	1	0	0	0	0

S
FLAT PACKAGE (TOP VIEW)



J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



positive logic: See truth table

description

These monolithic 4-bit true/complement elements, with the use of the two control lines (B, C), will transfer a 4-bit binary input (A) to the output (Y) in either true or complementary form. Furthermore, the control lines will also set all outputs to either a logical 0 or logical 1 independent of the state of the data inputs.

These circuits are fully compatible for use with other TTL or DTL circuits. Input clamping diodes are provided to minimize transmission line effects and thereby simplify system design. Each input represents only one normalized series 54H/74H load, and full fan-out to 10 series 54H/74H loads is available from each of the outputs in the logical 0 condition. In the logical 1 state, a fan-out of 20 is available to facilitate tying unused inputs to used inputs.

Power dissipation is 270 mW typically with an average propagation delay of 14 ns from data inputs to output.

The SN54H87 is characterized for operation over the full military temperature range of −55°C to 125°C, and the SN74H87 is characterized for operation from 0°C to 70°C.

absolute maximum ratings (over operating temperature range unless otherwise noted)

Supply Voltage V_{CC} (See Note 1) . . . . . 7 V
Input Voltage, V_{in} (See Note 1) . . . . . 5.5 V
Operating Case Temperature Range, SN54H87S . . . . . −55°C to 125°C
Operating Free-Air Temperature Range: SN54H87J, SN54H87N . . . . . −55°C to 125°C
SN74H87 Circuits . . . . . 0°C to 70°C
Storage Temperature Range . . . . . −65°C to 150°C

Note 1: These voltage values are with respect to network ground terminal.

recommended operating conditions (over operating temperature range)

		MIN	NOM	MAX	UNIT
Supply Voltage V_{CC} (See Note 1):	SN54H87 Circuits	4.5	5	5.5	V
	SN74H87 Circuits	4.75	5	5.25	V
Normalized Fan-Out from Each Output (N):	Logical 0			10	
	Logical 1			20	

NOTE 1: These voltage values are with respect to network ground terminal.

electrical characteristics (over operating temperature range unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS†	MIN	TYP‡	MAX	UNIT
$V_{in(1)}$	Input voltage required to ensure logical 1 at any input terminal	1	V_{CC} = MIN	2			V
$V_{in(0)}$	Input voltage required to ensure logical 0 at any input terminal	1	V_{CC} = MIN			0.8	V
$V_{out(1)}$	Logical 1 output voltage	1	V_{CC} = MIN, $V_{in(1)}$ = 2 V, $V_{in(0)}$ = 0.8 V, I_{load} = −1 mA	2.4			V
$V_{out(0)}$	Logical 0 output voltage	1	V_{CC} = MIN, $V_{in(1)}$ = 2 V, $V_{in(0)}$ = 0.8 V, I_{sink} = 20 mA			0.4	V
$I_{in(1)}$	Logical 1 level input current (each input)	2	V_{CC} = MAX, V_{in} = 2.4 V			50	μA
			V_{CC} = MAX, V_{in} = 5.5 V			1	mA
$I_{in(0)}$	Logical 0 level input current (each input)	3	V_{CC} = MAX, V_{in} = 0.4 V			−2	mA
I_{OS}	Short circuit output current§	4	V_{CC} = MAX, V_{out} = 0	−40		−100	mA
I_{CC}	Supply current (SN54H87)	5	V_{CC} = MAX		54	78	mA
I_{CC}	Supply current (SN74H87)	5	V_{CC} = MAX		54	89	mA

switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP‡	MAX	UNIT
t_{pd0}	Propagation delay time to logical 0 level from data inputs to outputs	6	C_L = 25 pF, R_L = 280 Ω		13	19	ns
t_{pd1}	Propagation delay time to logical 1 level from data inputs to outputs	6	C_L = 25 pF, R_L = 280 Ω		14	20	ns
t_{pd0}	Propagation delay time to logical 0 level from control inputs to outputs	6	C_L = 25 pF, R_L = 280 Ω		17	25	ns
t_{pd1}	Propagation delay time to logical 1 level from control inputs to outputs	6	C_L = 25 pF, R_L = 280 Ω		17	25	ns

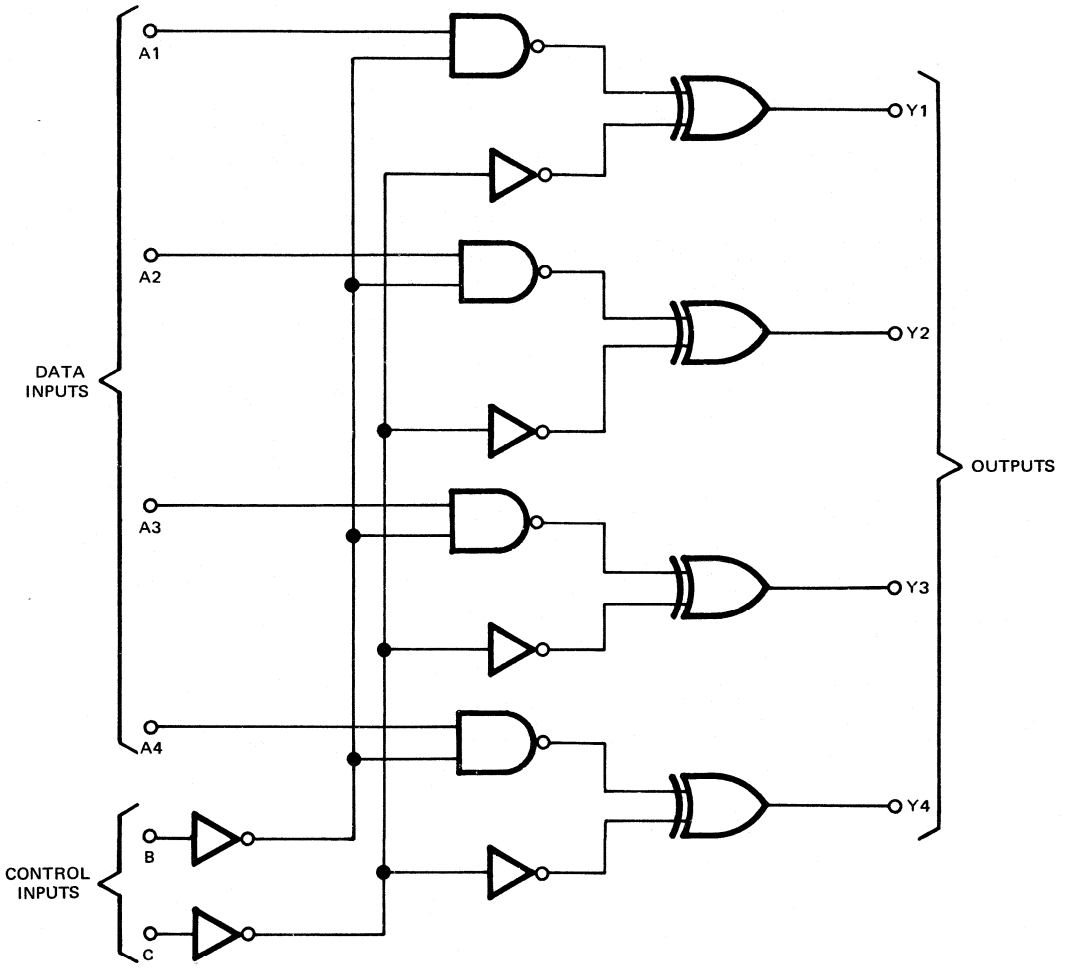
† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable circuit type.

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C

§ Not more than one output should be shorted at a time.

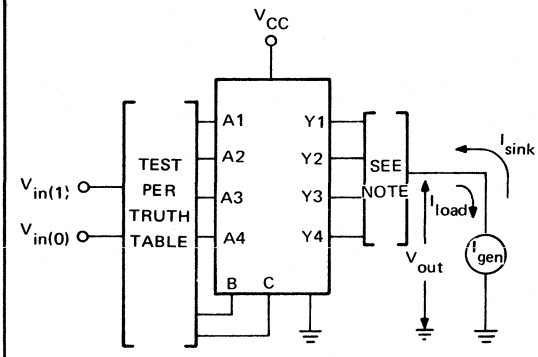
— SEE ORDERING INSTRUCTIONS PAGE 1-1 —

functional block diagram



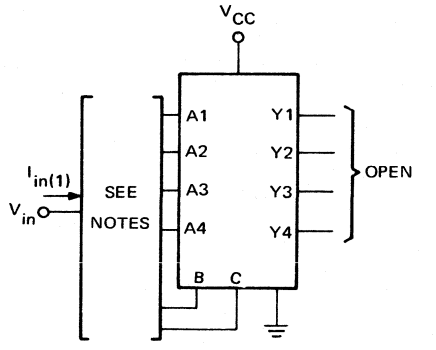
PARAMETER MEASUREMENT INFORMATION

d-c test circuits†



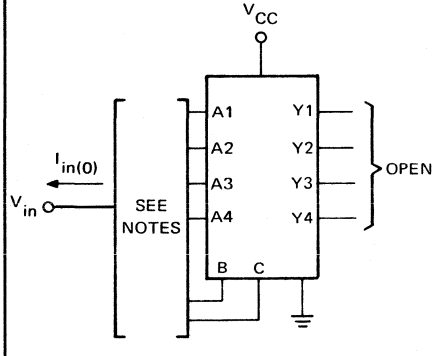
1. Each output is tested separately.

FIGURE 1



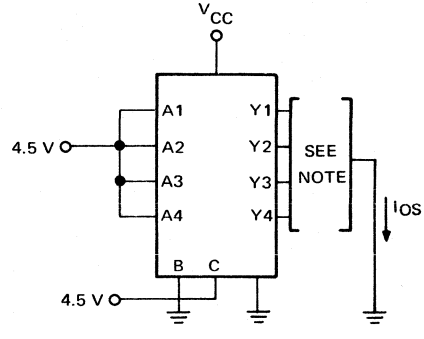
1. Each input is tested separately.
2. When testing A1, A2, A3, or A4 input B is at 4.5 V.

FIGURE 2



1. Each input is tested **separately**
2. When testing A1, A2, A3, or A4 input B is grounded.

FIGURE 3



1. Each output is tested separately.

FIGURE 4

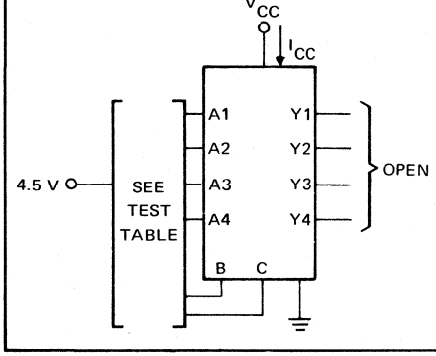


FIGURE 5

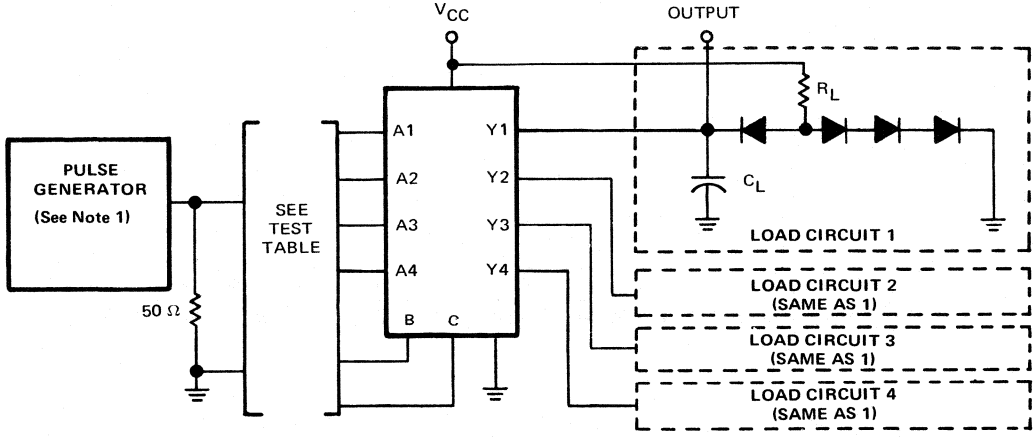
TEST TABLE

TEST NO.	APPLY 4.5 V	GROUND
1	A1, A2, A3, A4, B	B,C
2	C	A1, A2, A3, A4

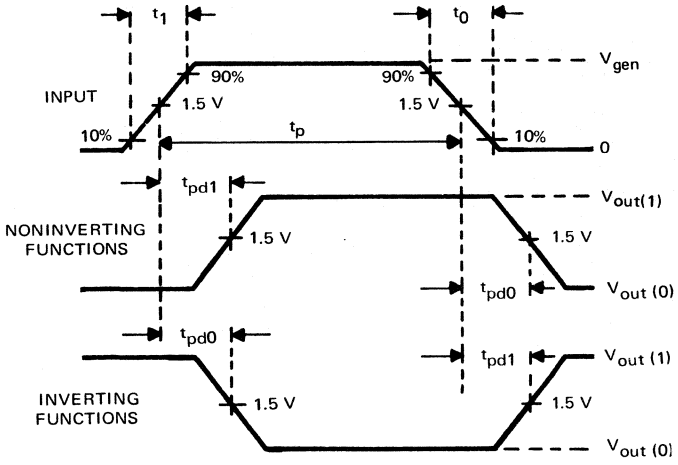
† Arrows indicate actual direction of current flow.

PARAMETER MEASUREMENT INFORMATION

switching characteristics



TEST CIRCUIT



VOLTAGE WAVEFORMS

TEST TABLE (See Note 2)

GND	INPUT	OUTPUT
B, C	A1	Y1
B, C	A2	Y2
B, C	A3	Y3
B, C	A4	Y4
C	B	Y1
C	B	Y2
C	B	Y3
C	B	Y4
B	C	Y1
B	C	Y2
B	C	Y3
B	C	Y4

NOTES: 1. The pulse generator has the following characteristics: V_{gen} = 3 V, $t_1 = t_0$ = 7 ns, t_p = 500 ns, PRR = 1 MHz, and $Z_{out} \approx 50\Omega$.
2. Inputs not specified are open.
3. C_L includes probe and jig capacitance.
4. All diodes are 1N3064.

FIGURE 6 – SWITCHING TIMES

Is Speed Your Need?

Use TI's new 50 MHZ flip-flops for your state-of-the-art counter and shift register designs

See Pages 3-46 to 3-58 for Specifications.

CIRCUIT TYPES SN5492, SN7492
DIVIDE-BY-TWELVE COUNTERS
(DIVIDE-BY-TWO AND DIVIDE-BY-SIX)

MSI TTL HIGH-SPEED COUNTERS

for applications in

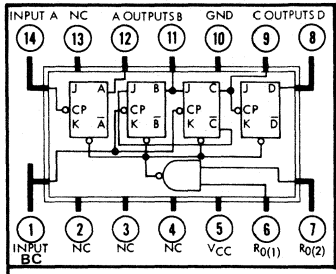
- Digital Computer Systems
- Data-Handling Systems
- Control Systems

logic

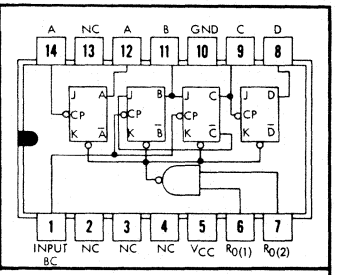
TRUTH TABLE (See Notes 1, 2, and 3)

COUNT	OUTPUT			
	D	C	B	A
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	1	0	0	0
7	1	0	0	1
8	1	0	1	0
9	1	0	1	1
10	1	1	0	0
11	1	1	0	1

S
FLAT PACKAGE (TOP VIEW)



J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



positive logic: see truth table

'NC—No Internal Connection

NOTES: 1. Output A connected to input B
2. To reset all outputs to logical 0 both $R_{0(1)}$ and $R_{0(2)}$ inputs must be at logical 1.
3. Either (or both) reset inputs $R_{0(1)}$ and $R_{0(2)}$ must be at a logical 0 to count.

description

These high-speed, monolithic 4-bit binary counters consist of four master slave flip-flops which are internally interconnected to provide a divide-by-two counter and a divide-by-six counter. A gated direct reset line is provided which inhibits the count inputs and simultaneously returns the four flip-flop outputs to a logical 0. As the output from flip-flop A is not internally connected to the succeeding flip-flops, the counter may be operated in two independent modes:

1. When used as a divide-by-twelve counter, output A must be externally connected to input BC. The input count pulses are applied to input A. Simultaneous divisions of 2, 6, and 12 are performed at the A, C, and D outputs as shown in the truth table above.

2. When used as a divide-by-six counter, the input count pulses are applied to input BC. Simultaneously, frequency divisions of 3 and 6 are available at the C and D outputs. Independent use of flip-flop A is available if the reset function coincides with reset of the divide-by-six counter.

These circuits are completely compatible with Series 54/74 TTL and DTL logic families. Average power dissipation is 155 mW.

absolute maximum ratings (over operating temperature range unless otherwise noted)

Supply Voltage V_{CC} (See Note 4)		7 V
Input Voltage V_{in} (See Notes 4 and 5)		5.5 V
Operating Case Temperature Range:	SN5492S	−55°C to 125°C
Operating Free-Air Temperature Range:	SN5492J, SN5492N	−55°C to 125°C
	SN7492 Circuits	0°C to 70°C
Storage Temperature Range		−65°C to 150°C

NOTES: 4. These voltage values are with respect to network ground terminal.
5. Input signals must be zero or positive with respect to network ground terminal.

recommended operating conditions (over operating temperature range)

	MIN	NOM	MAX	UNIT
Supply Voltage V_{CC} (See Note 4): SN5492 Circuits	4.5	5	5.5	V
SN7492 Circuits	4.75	5	5.25	V
Normalized Fan-Out From Each Output (See Note 6)			10	
Width of Input Count Pulse, $t_{p(in)}$	50			ns
Width of Reset Pulse, $t_{p(reset)}$	50			ns

NOTE: 6. Fan-out from output A to input BC and to 10 additional Series 54/74 loads is permitted.

electrical characteristics (over operating temperature range unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
$V_{in(1)}$	Input voltage required to ensure logical 1 at any input terminal	1	V_{CC} = MIN		2			V
$V_{in(0)}$	Input voltage required to ensure logical 0 at any input terminal	2	V_{CC} = MIN				0.8	V
$V_{out(1)}$	Logical 1 output voltage	2	V_{CC} = MIN, I_{load} = −400 μA		2.4			V
$V_{out(0)}$	Logical 0 output voltage	1	V_{CC} = MIN, I_{sink} = 16 mA				0.4	V
$I_{in(1)}$	Logical 1 level input current at $R_{0(1)}$ or $R_{0(2)}$ inputs	3	V_{CC} = MAX, V_{in} = 2.4 V				40	μA
			V_{CC} = MAX, V_{in} = 5.5 V				1	mA
$I_{in(1)}$	Logical 1 level input current at input A	3	V_{CC} = MAX, V_{in} = 2.4 V				80	μA
			V_{CC} = MAX, V_{in} = 5.5 V				1	mA
$I_{in(1)}$	Logical 1 level input current at input BC	3	V_{CC} = MAX, V_{in} = 2.4 V				160	μA
			V_{CC} = MAX, V_{in} = 5.5 V				1	mA
$I_{in(0)}$	Logical 0 level input current at $R_{0(1)}$ or $R_{0(2)}$ inputs	4	V_{CC} = MAX, V_{in} = 0.4 V				−1.6	mA
$I_{in(0)}$	Logical 0 level input current input A	4	V_{CC} = MAX, V_{in} = 0.4 V				−3.2	mA
$I_{in(0)}$	Logical 0 level input current at input BC	4	V_{CC} = MAX, V_{in} = 0.4 V				−6.4	mA
I_{OS}	Short-circuit output current§	5	V_{CC} = MAX, V_{out} = 0	SN5492	−20		−57	mA
				SN7492	−18		−57	mA
I_{CC}	Supply current	3	V_{CC} = MAX, V_{in} = 4.5 V	SN5492		31	44	mA
				SN7492		31	51	mA

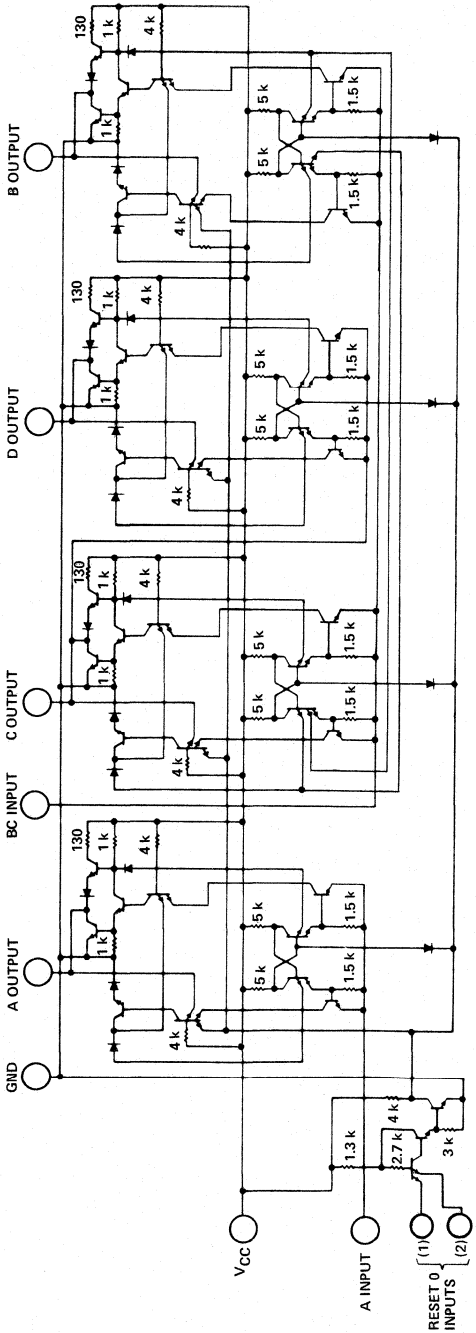
† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the particular circuit type.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ Not more than one output should be shorted at a time.

switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max}	Maximum frequency of input count pulses		C_L = 15 pF, R_L = 400 Ω	10	18		MHz
t_{pd1}	Propagation delay time to logical 1 level from input count pulse to output D	6	C_L = 15 pF, R_L = 400 Ω		60	100	ns
t_{pd0}	Propagation delay time to logical 0 level from input count pulse to output D	6	C_L = 15 pF, R_L = 400 Ω		60	100	ns

–SEE ORDERING INSTRUCTIONS PAGE 1-1–

schematic

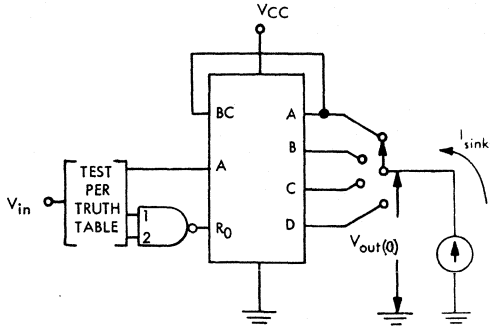


Component values shown are nominal.

Resistor values are in ohms.

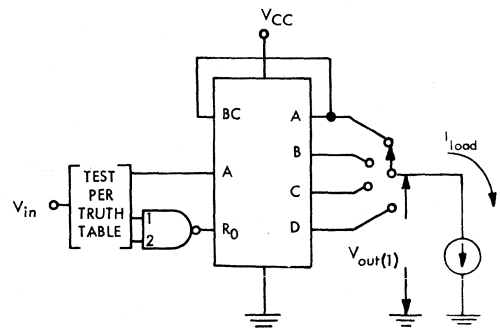
PARAMETER MEASUREMENT INFORMATION

d-c test circuits†



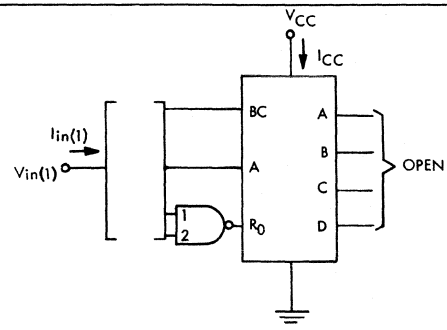
1. Each output is tested in the logical 0 state.

FIGURE 1



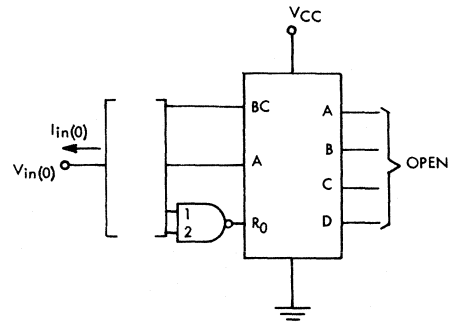
1. Each output is tested in the logical 1 state.

FIGURE 2



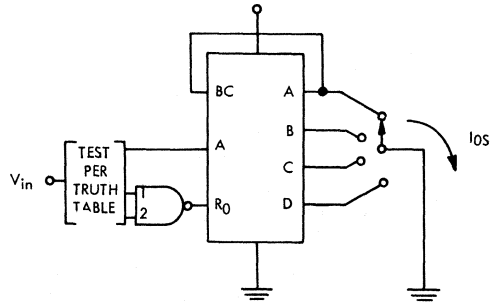
1. Each input is tested separately.
2. When testing $R_0(1)$ ground $R_0(2)$.
3. When testing $R_0(2)$ ground $R_0(1)$.
4. When testing I_{CC} reset all outputs to logical 0, ground all inputs, then measure I_{CC}.

FIGURE 3



1. Each input is tested separately.
2. When testing $R_0(1)$ apply 4.5 V to $R_0(2)$.
3. When testing $R_0(2)$ apply 4.5 V to $R_0(1)$.

FIGURE 4

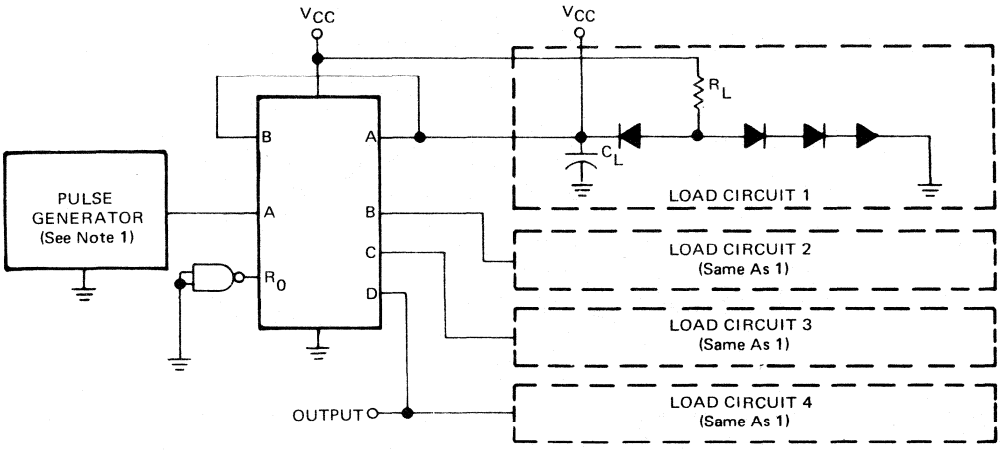


1. Each output is tested in the logical 1 state.

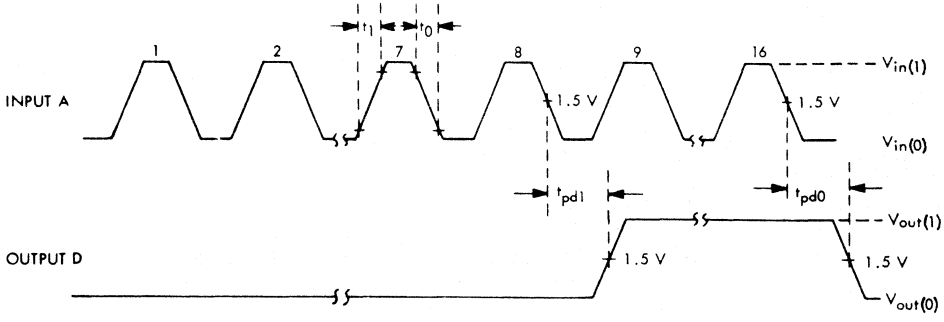
FIGURE 5

†Arrows indicate actual direction of current flow

switching characteristics — PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES: 1. The pulse generator has the following characteristics: V_{gen} = 3 V, $t_0 = t_1 \leqslant 15$ ns, t_p = 0.5 μs, PRR = 1 MHz, $Z_{out} \approx 50\ \Omega$.
2. All diodes are 1N3064.
3. C_L includes probe and jig capacitance.
4. $t_{pd} = \frac{t_{pd0} + t_{pd1}}{2}$
5. Voltage values are with respect to ground terminal.

FIGURE 6-SWITCHING TIMES

SN54121/SN74121
The One-Shot
Heard 'Round the World

Pulse Width: 40 Nanoseconds to 40 Seconds

Pulse Stability: ±0.2%

Triggering: Ramps Up to One Volt Per Second

See Page 2-38 for specifications and Page B-1 for abstract and ordering information of Application Report CA-128

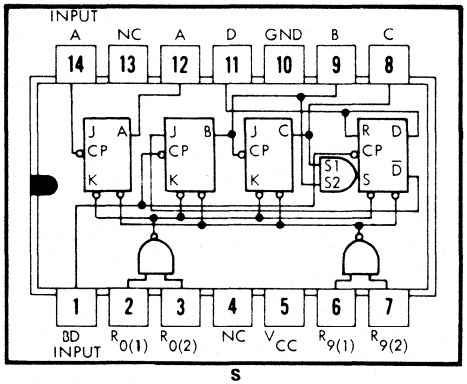
MSI TTL HIGH-SPEED DECADE COUNTERS

for applications in

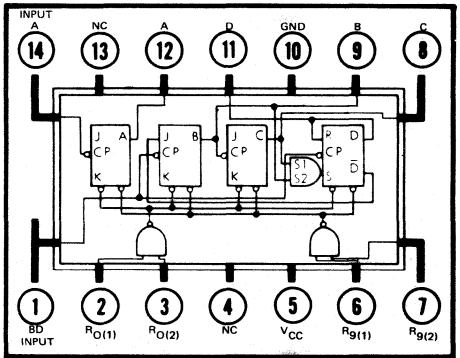
- Digital Computer Systems
- Data-Handling Systems
- Control Systems

logic

J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



S
FLAT PACKAGE (TOP VIEW)



positive logic: see truth table

TRUTH TABLES

BCD COUNT SEQUENCE
(See Note 1)

COUNT	OUTPUT D	C	B	A
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1

RESET/COUNT (See Note 2)

RESET INPUTS $R_{0(1)}$	$R_{0(2)}$	$R_{9(1)}$	$R_{9(2)}$	OUTPUT D C B A
1	1	0	X	0 0 0 0
1	1	X	0	0 0 0 0
X	X	1	1	1 0 0 1
X	0	X	0	COUNT
0	X	0	X	COUNT
0	X	X	0	COUNT
X	0	0	X	COUNT

NC—No Internal Connection

NOTES: 1. Output A connected to input BD for BCD count.
2. X indicates that either a logical 1 or a logical 0 may be present.

description and typical count configurations

These high-speed, monolithic decade counters consist of four dual-rank, master-slave flip-flops internally interconnected to provide a divide-by-two counter and a divide-by-five counter. Gated direct reset lines are provided to inhibit count inputs and return all outputs to logical zero or to a binary coded decimal (BCD) count of 9. As the output from flip-flop A is not internally connected to the succeeding stages, the count may be separated in three independent count modes:

1. When used as a binary coded decimal decade counter, the BD input must be externally connected to the A output. The A input receives the incoming count, and a count sequence is obtained in accordance with the BCD count sequence truth table shown above. In addition to a conventional zero reset, inputs are provided to reset a BCD count for nine's complement decimal applications.

2. If a symmetrical divide-by-ten count is desired for frequency synthesizers or other applications requiring division of a binary count by a power of ten, the D output must be externally connected to the A input. The input count is then applied at the BD input and a divide-by-ten square wave is obtained at output A.

3. For operation as a divide-by-two counter and a divide-by-five counter, no external interconnections are required. Flip-flop A is used as a binary element for the divide-by-two function. The BD input is used to obtain binary divide-by-five operation at the B, C, and D outputs. In this mode, the two counters operate independently; however, all four flip-flops are reset simultaneously.

These circuits are completely compatible with Series 54/74 TTL and DTL logic families. Average power dissipation is 160 mW.

absolute maximum ratings (over operating temperature range unless otherwise noted)

Supply Voltage V_{CC} (See Note 3) . . . . . 7 V
Input Voltage, V_{in} (See Notes 3 and 4) . . . . . 5.5 V
Operating Case Temperature Range: SN5490S . . . . . −55°C to 125°C
Operating Free-Air Temperature Range: SN5490J, SN5490N . . . . . −55°C to 125°C
SN7490 Circuits . . . . . 0°C to 70°C
Storage Temperature Range . . . . . −65°C to 150°C

NOTES: 3. These voltage values are with respect to network ground terminal.
4. Input signals must be zero or positive with respect to network ground terminal.

recommended operating conditions (over operating temperature range)

	MIN	NOM	MAX	UNIT
Supply Voltage V_{CC} (See Note 3): SN5490 Circuits	4.5	5	5.5	V
SN7490 Circuits	4.75	5	5.25	V
Normalized Fan-Out From Each Output (See Note 5)			10	
Width of Input Count Pulse, $t_{p(in)}$	50			ns
Width of Reset Pulse, $t_{p(reset)}$	50			ns

NOTE 5. Fan-out from output A to input BD and to 10 additional Series 54/74 loads is permitted.

electrical characteristics (over operating temperature range unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
$V_{in(1)}$	Input voltage required to ensure logical 1 at any input terminal	1	V_{CC} = MIN		2			V
$V_{in(0)}$	Input voltage required to ensure logical 0 at any input terminal	2	V_{CC} = MIN				0.8	V
$V_{out(1)}$	Logical 1 output voltage	2	V_{CC} = MIN, I_{load} = −400 μA		2.4			V
$V_{out(0)}$	Logical 0 output voltage	1	V_{CC} = MIN, I_{sink} = 16 mA				0.4	V
$I_{in(1)}$	Logical 1 level input current at $R_{0(1)}$, $R_{0(2)}$, $R_{9(1)}$, or $R_{9(2)}$	3	V_{CC} = MAX, V_{in} = 2.4 V				40	μA
			V_{CC} = MAX, V_{in} = 5.5 V				1	mA
$I_{in(1)}$	Logical 1 level input current at input A	3	V_{CC} = MAX, V_{in} = 2.4 V				80	μA
			V_{CC} = MAX, V_{in} = 5.5 V				1	mA
$I_{in(1)}$	Logical 1 level input current at input BD	3	V_{CC} = MAX, V_{in} = 2.4 V				160	μA
			V_{CC} = MAX, V_{in} = 5.5 V				1	mA
$I_{in(0)}$	Logical 0 level input current at $R_{0(1)}$, $R_{0(2)}$, $R_{9(1)}$, or $R_{9(2)}$	4	V_{CC} = MAX, V_{in} = 0.4 V				−1.6	mA
$I_{in(0)}$	Logical 0 level input current at input A	4	V_{CC} = MAX, V_{in} = 0.4 V				−3.2	mA
$I_{in(0)}$	Logical 0 level input current at input BD	4	V_{CC} = MAX, V_{in} = 0.4 V				−6.4	mA
I_{OS}	Short-circuit output current§	5	V_{CC} = MAX, V_{out} = 0 V	SN5490	−20		−57	mA
				SN7490	−18		−57	mA
I_{CC}	Supply current	3	V_{CC} = MAX, V_{in} = 4.5 V	SN5490		32	46	mA
				SN7490		32	53	mA

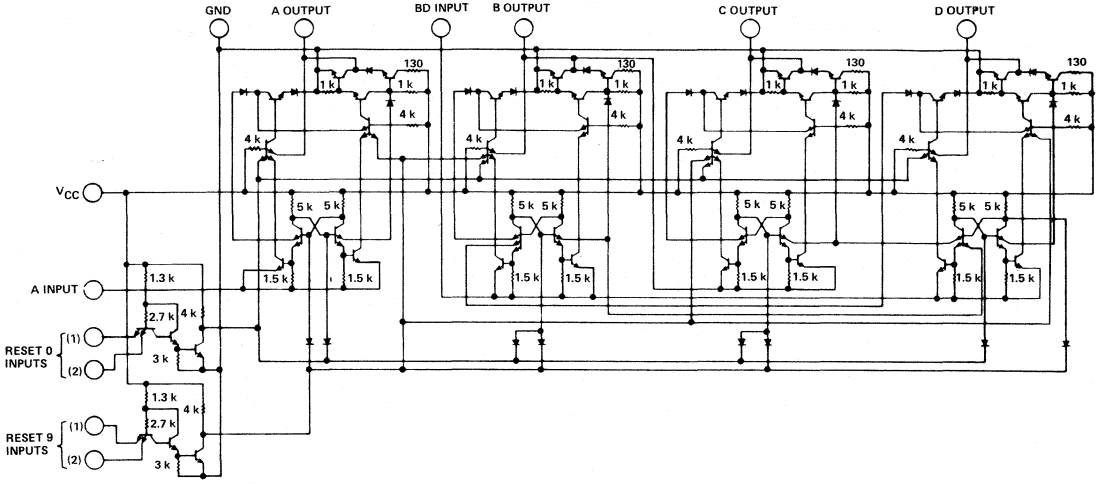
† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the particular circuit type.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C
§ Not more than one output should be shorted at a time.

—SEE ORDERING INSTRUCTIONS PAGE 1-1—

switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max}	Maximum frequency of input count pulses		C_L = 15 pF, R_L = 400 Ω	10	18		MHz
t_{pd1}	Propagation delay time to logical 1 level from input count pulse to output C	6	C_L = 15 pF, R_L = 400 Ω		60	100	ns
t_{pd0}	Propagation delay time to logical 0 level from input count pulse to output C	6	C_L = 15 pF, R_L = 400 Ω		60	100	ns

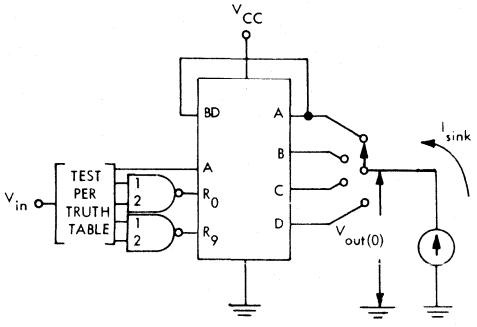
schematic



Component values shown are nominal.
Resistor values are in ohms.

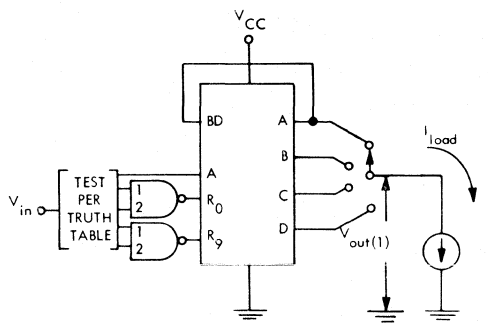
PARAMETER MEASUREMENT INFORMATION

d-c test circuits†



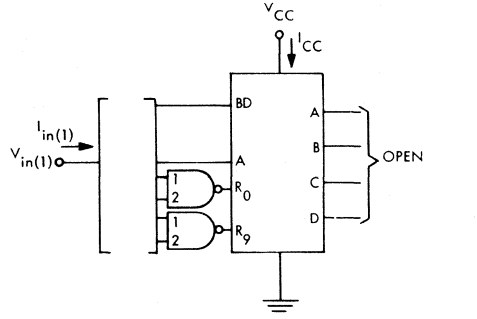
1. Each output is tested in the logical 0 state.

FIGURE 1



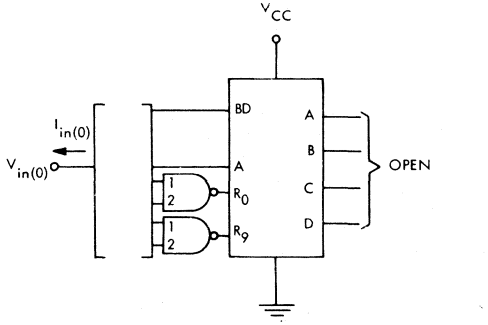
1. Each output is tested in the logical 1 state.

FIGURE 2



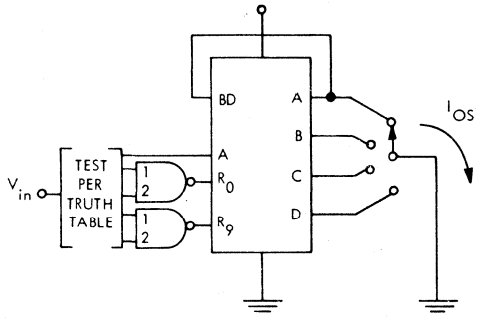
1. Each input is tested separately.
2. When testing $R_{0(1)}$ or $R_{9(1)}$ ground $R_{0(2)}$ or $R_{9(2)}$
3. When testing $R_{0(2)}$ or $R_{9(2)}$ ground $R_{0(1)}$ or $R_{9(1)}$
4. When testing I_{CC} reset all outputs to logical 0, ground all inputs, then measure I_{CC}.

FIGURE 3



1. Each input is tested separately.
2. When testing $R_{0(1)}$ or $R_{9(1)}$ apply 4.5 V to $R_{0(2)}$ or $R_{9(2)}$.
3. When testing $R_{0(2)}$ or $R_{9(2)}$ apply 4.5 V to $R_{0(1)}$ or $R_{9(1)}$.

FIGURE 4

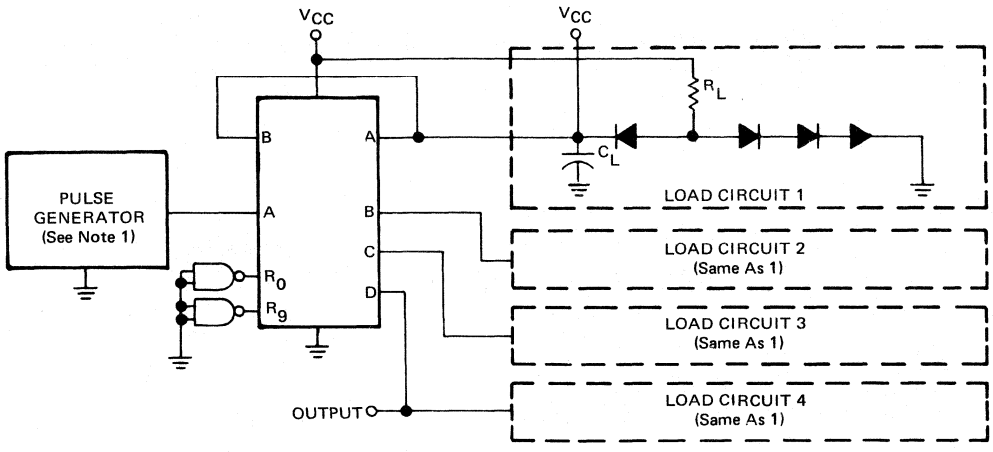


1. Each output is tested in the logical 1 state.

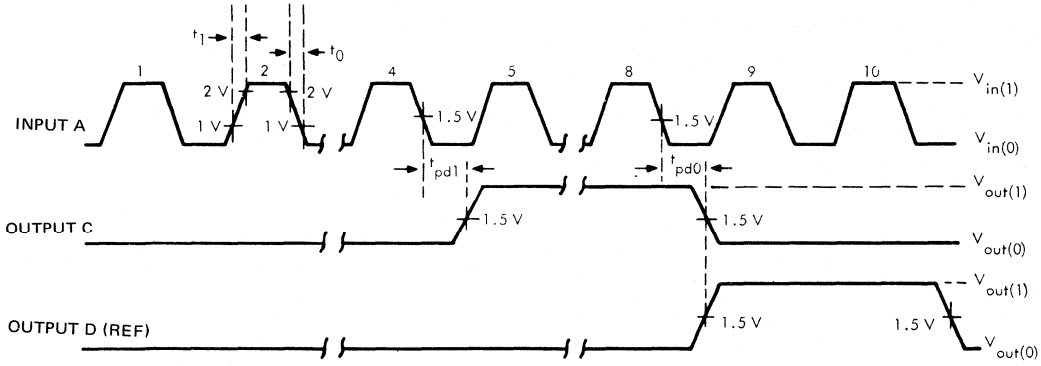
FIGURE 5

† Arrows indicate actual direction of current flow.

switching characteristics — PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



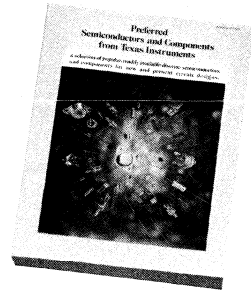
VOLTAGE WAVEFORMS

NOTES: 1. The pulse generator has the following characteristics: V_{gen} = 3 V, $t_0 = t_1 \leqslant 15$ ns, t_p = 0.5 μs, PRR = 1 MHz, $Z_{out} \approx 50\ \Omega$.
2. All diodes are 1N3064.
3. C_L includes probe and jig capacitance.
4. $t_{pd} = \frac{t_{pd0} + t_{pd1}}{2}$
5. Voltage values are with respect to ground terminal.

FIGURE 6-SWITCHING TIMES

The Trend is TTL in Integrated Circuits...

... in Discretes the Trend is Preferred Semiconductors



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TEXAS INSTRUMENTS
INCORPORATED

CIRCUIT TYPES SN5493, SN7493
4-BIT BINARY COUNTERS

MSI TTL HIGH-SPEED RIPPLE-THROUGH COUNTERS

for applications in

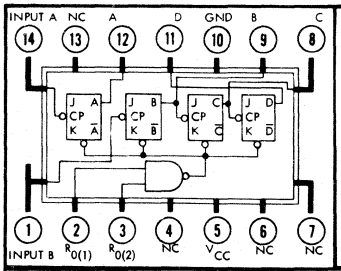
- **Digital Computer Systems**
- **Data-Handling Systems**
- **Control Systems**

logic

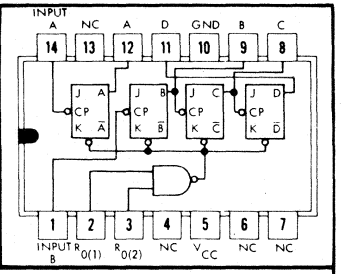
TRUTH TABLE (See Notes 1, 2, and 3)

COUNT	OUTPUT D	C	B	A
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1
10	1	0	1	0
11	1	0	1	1
12	1	1	0	0
13	1	1	0	1
14	1	1	1	0
15	1	1	1	1

S
FLAT PACKAGE (TOP VIEW)



J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



positive logic: see truth table

NC—No Internal Connection

NOTES: 1. Output A connected to input B
2. To reset all outputs to logical 0 both $R_{0(1)}$ and $R_{0(2)}$ inputs must be at logical 1.
3. Either (or both) reset inputs $R_{0(1)}$ and $R_{0(2)}$ must be at a logical 0 to count.

description

These high-speed, monolithic 4-bit binary counters consist of four master-slave flip-flops which are internally interconnected to provide a divide-by-two counter and a divide-by-eight counter. A gated direct reset line is provided which inhibits the count inputs and simultaneously returns the four flip-flop outputs to a logical 0. As the output from flip-flop A is not internally connected to the succeeding flip-flops the counter may be operated in two independent modes:

1. When used as a 4-bit ripple-through counter, output A must be externally connected to input B. The input count pulses are applied to input A. Simultaneous divisions of 2, 4, 8, and 16 are performed at the A, B, C, and D outputs as shown in the truth table above.

2. When used as a 3-bit ripple-through counter, the input count pulses are applied to input B. Simultaneous frequency divisions of 2, 4, and 8 are available at the B, C, and D outputs. Independent use of flip-flop A is available if the reset function coincides with reset of the 3-bit ripple-through counter.

These circuits are completely compatible with Series 54/74 TTL and DTL logic families. Average power dissipation is 32 mW per flip-flop (128 mW total).

absolute maximum ratings (over operating temperature range unless otherwise noted)

Supply Voltage V_{CC} (See Note 4)	7 V
Input Voltage, V_{in} (See Notes 4 and 5)	5.5 V
Operating Case Temperature Range: SN5493S	−55°C to 125°C
Operating Free-Air Temperature Range: SN5493J, SN5493N	−55°C to 125°C
SN7493 Circuits	0°C to 70°C
Storage Temperature Range	−65°C to 150°C

NOTES: 4. These voltage values are with respect to network ground terminal.
5. Input signals must be zero or positive with respect to network ground terminal.

recommended operating conditions (over operating temperature range)

	MIN	NOM	MAX	UNIT
Supply Voltage V_{CC} (See Note 4): SN5493 Circuits	4.5	5	5.5	V
SN7493 Circuits	4.75	5	5.25	V
Normalized Fan-Out From Each Output (See Note 6)			10	
Width of Input Count Pulse, $t_{p(in)}$	50			ns
Width of Reset Pulse, $t_{p(reset)}$	50			ns

NOTE: 6. Fan-out from output A to input B and to 10 additional Series 54/74 loads is permitted.

electrical characteristics (over operating temperature range unless otherwise noted)

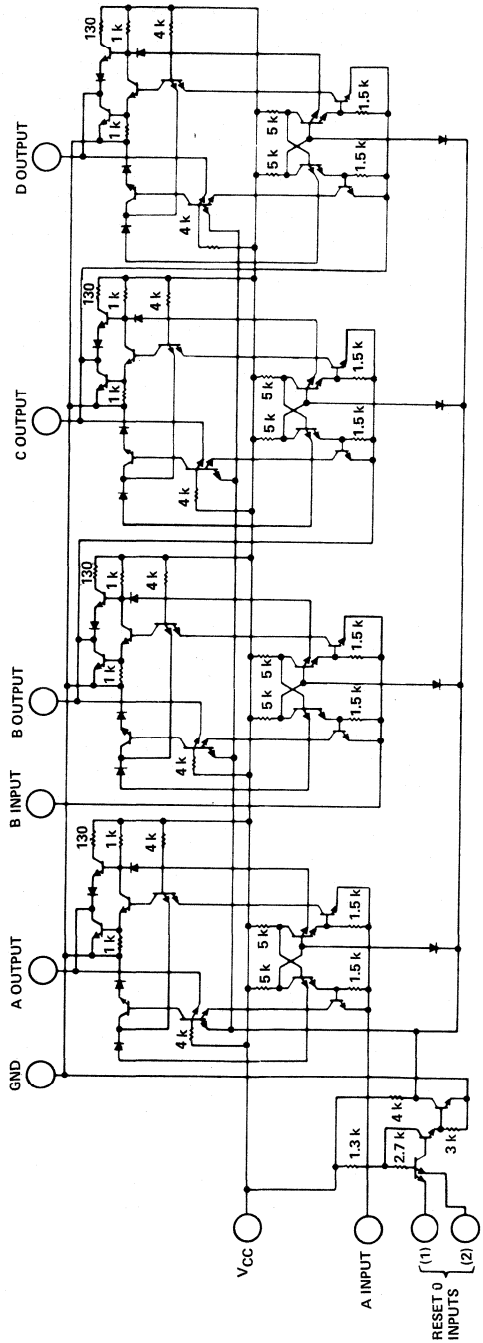
PARAMETER		TEST FIGURE	TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
$V_{in(1)}$	Input voltage required to ensure logical 1 at any input terminal	1	V_{CC} = MIN		2			V
$V_{in(0)}$	Input voltage required to ensure logical 0 at any input terminal	2	V_{CC} = MIN				0.8	V
$V_{out(1)}$	Logical 1 output voltage	2	V_{CC} = MIN, I_{load} = −400 μA		2.4			V
$V_{out(0)}$	Logical 0 output voltage	1	V_{CC} = MIN, I_{sink} = 16 mA				0.4	V
$I_{in(1)}$	Logical 1 level input current at $R_{0(1)}$ or $R_{0(2)}$ inputs	3	V_{CC} = MAX, V_{in} = 2.4 V				40	μA
			V_{CC} = MAX, V_{in} = 5.5 V				1	mA
$I_{in(1)}$	Logical 1 level input current at A or B inputs	3	V_{CC} = MAX, V_{in} = 2.4 V				80	μA
			V_{CC} = MAX, V_{in} = 5.5 V				1	mA
$I_{in(0)}$	Logical 0 level input current at $R_{0(1)}$ or $R_{0(2)}$ inputs	4	V_{CC} = MAX, V_{in} = 0.4 V				−1.6	mA
$I_{in(0)}$	Logical 0 level input current at A or B inputs	4	V_{CC} = MAX, V_{in} = 0.4 V				−3.2	mA
I_{OS}	Short-circuit output current§	5	V_{CC} = MAX, V_{out}=0	SN5493	−20		−57	mA
				SN7493	−18		−57	mA
I_{CC}	Supply current	3	V_{CC} = MAX, V_{in} = 4.5 V	SN5493		32	46	mA
				SN7493		32	53	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable circuit type.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ Not more than one output should be shorted at a time.

switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max}	Maximum frequency of input count pulses		C_L = 15 pF, R_L = 400 Ω	10	18		MHz
t_{pd1}	Propagation delay time to logical 1 level from input count pulse to output D	6	C_L = 15 pF, R_L = 400 Ω		75	135	ns
t_{pd0}	Propagation delay time to logical 0 level from input count pulse to output D	6	C_L = 15 pF, R_L = 400 Ω		75	135	ns

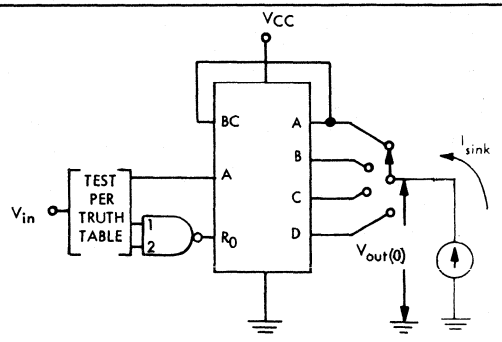
schematic



Component values shown are nominal.
Resistor values are in ohms.

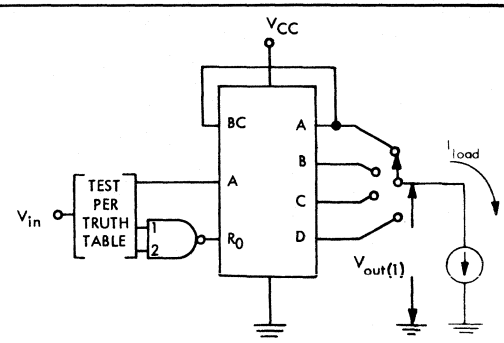
PARAMETER MEASUREMENT INFORMATION

d-c test circuits†



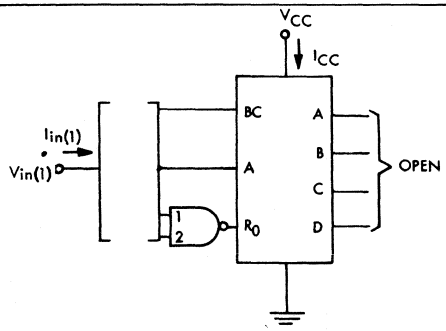
1. Each output is tested in the logical 0 state.

FIGURE 1



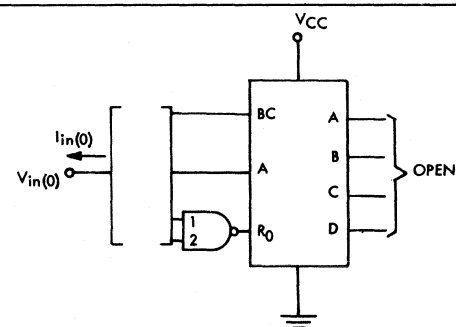
1. Each output is tested in the logical 1 state.

FIGURE 2



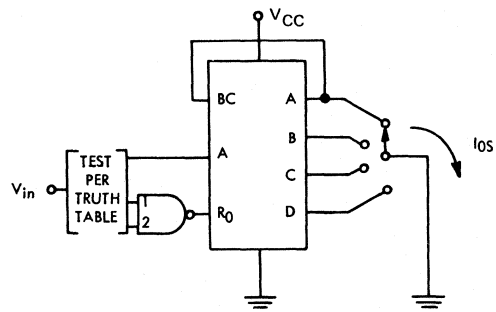
1. Each input is tested separately.
2. When testing $R_0(1)$ ground $R_0(2)$.
3. When testing $R_0(2)$ ground $R_0(1)$.
4. When testing I_{CC} all inputs and outputs are open.

FIGURE 3



1. Each input is tested separately.
2. When testing $R_0(1)$ apply 4.5 V to $R_0(2)$.
3. When testing $R_0(2)$ apply 4.5 V to $R_0(1)$.

FIGURE 4



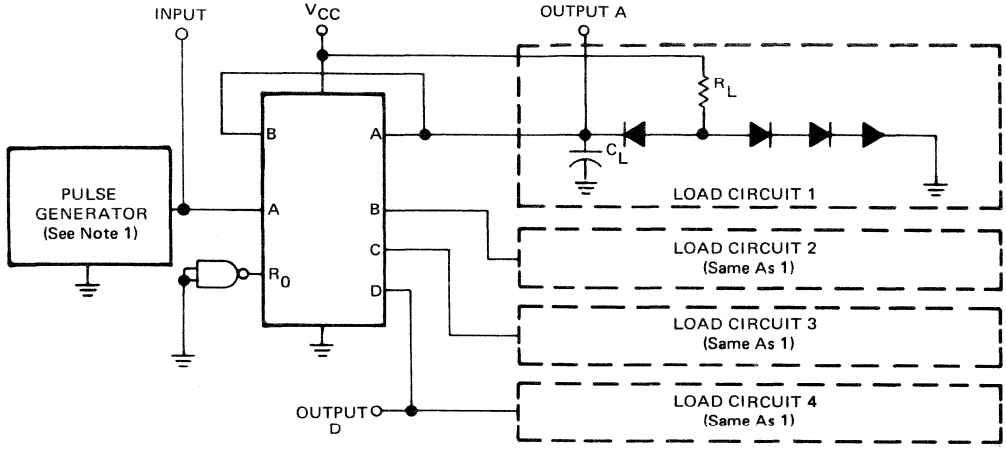
1. Each output is tested in the logical 1 state.

FIGURE 5

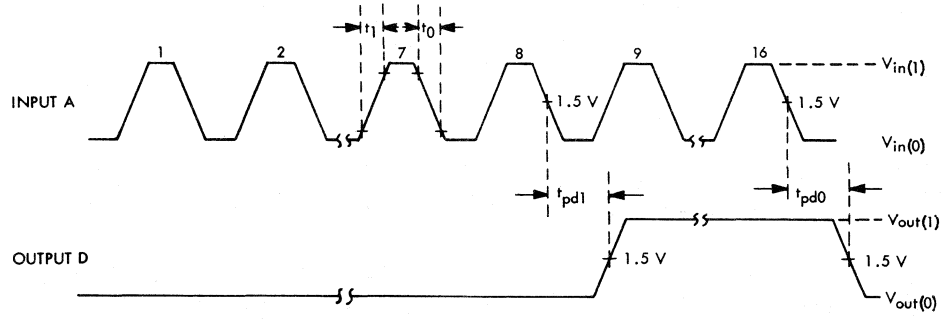
†Arrows indicate actual direction of current flow.

PARAMETER MEASUREMENT INFORMATION

switching characteristics



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES: 1. The pulse generator has the following characteristics: V_{gen} = 3 V, $t_0 = t_1 \leqslant 15$ ns, t_p = 0.5 μs, PRR = 1 MHz, $Z_{out} \approx 50\ \Omega$.
2. All diodes are 1N3064
3. C_L includes probe and jig capacitance.
4. $t_{pd} = \frac{t_{pd0} + t_{pd1}}{2}$
5. Voltage values are with respect to ground terminal.

FIGURE 6-SWITCHING TIMES

FAN-OUT? That's Simple....

$$\frac{300/65}{20/12+4/18+1/6.5+40/24+2/0.8+30\,pF} = ?$$

Now let's see: 20+4+1+40+2=67
And: 12+18+6.5+24+0.8=61.3
Hmmm....67/61.3 and 30 puffs.
Now, what happens at −55°C?

A few minutes reviewing TTL LOADING DATA, Section 12,

will put you on your way to designing mixed systems using COMPATIBLE TTL with loading rules you can remember. Even when it gets tight, the decimals are round.

CIRCUIT TYPES SN54L93, SN74L93
4-BIT BINARY COUNTERS

A SERIES 54L/74L TTL LOW-POWER RIPPLE-THROUGH COUNTER FOR APPLICATIONS IN

● Digital Computer Systems ● Data-Handling Systems ● Control Systems

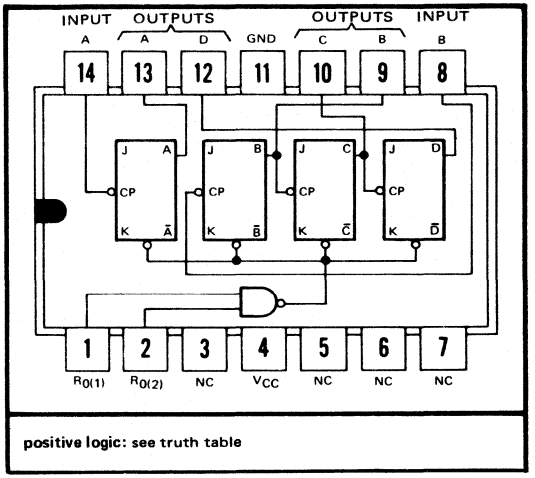
logic

TRUTH TABLE (See Notes 1 and 2)

COUNT	OUTPUT			
	D	C	B	A
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1
10	1	0	1	0
11	1	0	1	1
12	1	1	0	0
13	1	1	0	1
14	1	1	1	0
15	1	1	1	1

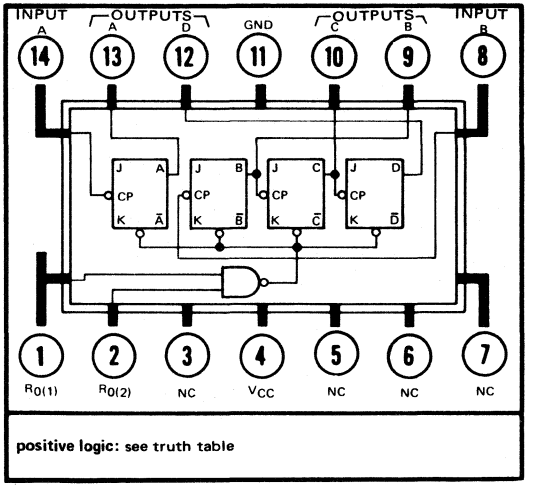
NOTES: 1. Output A connected to input B.
2. To reset all outputs to logical 0 both $R_{0(1)}$ and $R_{0(2)}$. Inputs must be at a logical 1.
3. Either (or both) reset inputs $R_{0(1)}$ and $R_{0(2)}$ must be at a logical 0 to count.

J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



positive logic: see truth table

T FLAT PACKAGE (TOP VIEW)



positive logic: see truth table

NC—No Internal Connection

description

The SN54L93/SN74L93 are low-power TTL monolithic 4-bit binary counters consisting of four master-slave flip-flops which are internally interconnected to provide a divide-by-two counter and a divide-by-eight counter. A gated direct reset line is provided which inhibits the count inputs and simultaneously returns the four flip-flop outputs to a logical 0. As the output from flip-flop A is not internally connected to the succeeding flip-flops the counter may be operated in two independent modes:

1. When used as a 4-bit ripple-through counter, output A must be externally connected to input B. The input count pulses are applied to input A. Simultaneous divisions of 2, 4, 8, and 16 are performed at the A, B, C, and D outputs as shown in the truth table above.
2. When used as a 3-bit ripple-through counter, the input count pulses are applied to input B. Simultaneous frequency divisions of 2, 4, and 8 are available at the B, C, and D outputs. Independent use of flip-flop A is available if the reset function coincides with reset of the 3-bit ripple-through counter.

The SN54L93/SN74L93 is completely compatible with TTL and DTL logic families. Average power dissipation is typically 16 mW.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply Voltage V_{CC} (See Note 4) . . . . . 8 V
Input Voltage, V_{in} (See Notes 4 and 5) . . . . . 5.5 V
Operating Free Air Temperature Ranges: SN54L93 Circuits . . . . . −55°C to 125°C
SN74L93 Circuits . . . . . 0°C to 70°C
Storage Temperature Range . . . . . −65°C to 150°C

NOTES: 4. These voltage values are with respect to network ground terminal.
5. Input signals must be zero or positive with respect to network ground terminal.

recommended operating conditions

Supply Voltage V_{CC}: SN54L93 Circuits . . . . . 4.5 V to 5.5 V
SN74L93 Circuits . . . . . 4.75 V to 5.25 V
Maximum Normalized Fan-Out From Each Output (See Note 6) 10
Width of Input Count Pulse, $t_{p(in)}$ . . . . . ⩾ 200 ns
Width of Reset Pulse, $t_{p(reset)}$ . . . . . ⩾ 200 ns

NOTE: 6. Fan-out from output A to input B and to 10 additional Series 54L/74L loads is permitted.

electrical characteristics over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS†	MIN	TYP‡	MAX	UNIT
$V_{in(1)}$	Input voltage required to ensure logical 1 of any input	1	V_{CC} = MIN	2			V
$V_{in(0)}$	Input voltage required to ensure logical 0 of any input	2	V_{CC} = MIN			0.7	V
$V_{out(1)}$	Logical 1 output voltage	2	V_{CC} = MIN, I_{load} = −100 μA	2.4			V
$V_{out(0)}$	Logical 0 output voltage	1	V_{CC} = MIN, I_{sink} = 2 mA			0.3	V
$I_{in(1)}$	Logical 1 level input current at $R_{0(1)}$ or $R_{0(2)}$ inputs	3	V_{CC} = MAX, V_{in} = 2.4 V			10	μA
			V_{CC} = MAX, V_{in} = 5.5 V			100	μA
$I_{in(1)}$	Logical 1 level input current at A or B inputs	3	V_{CC} = MAX, V_{in} = 2.4 V			20	μA
			V_{CC} = MAX, V_{in} = 5.5 V			200	μA
$I_{in(0)}$	Logical 0 level input current at $R_{0(1)}$ or $R_{0(2)}$ inputs	4	V_{CC} = MAX, V_{in} = 0.3 V			−0.18	mA
$I_{in(0)}$	Logical 0 level input current at A or B inputs	4	V_{CC} = MAX, V_{in} = 0.3 V			−0.36	mA
I_{OS}	Short-circuit output current	5	V_{CC} = MAX, V_{out} = 0	−3		−15	mA
I_{CC}	Supply current	3	V_{CC} = MAX		3.2	6.6	mA

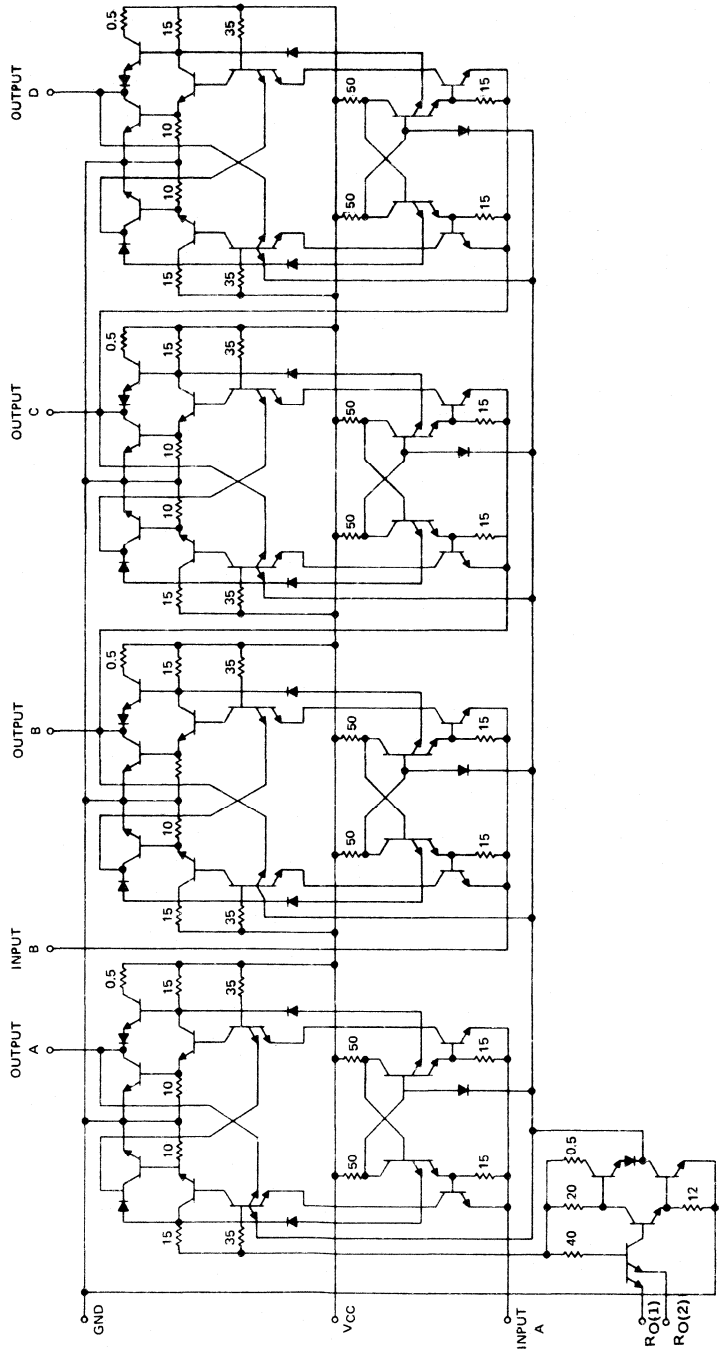
† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
‡ These typical values are at V_{CC} = 5 V, T_A = 25°C.

switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max}	Maximum frequency of input count pulses		C_L = 50 pF, R_L = 4 kΩ		3		MHz
t_{pd1}	Propagation delay time to logical 1 level from input count pulse to output D	6	C_L = 50 pF, R_L = 4 kΩ		280	450	ns
t_{pd0}	Propagation delay time to logical 0 level from input count pulse to ouput D	6	C_L = 50 pF, R_L = 4 kΩ		280	450	ns

— SEE ORDERING INSTRUCTIONS PAGE 1-1 —

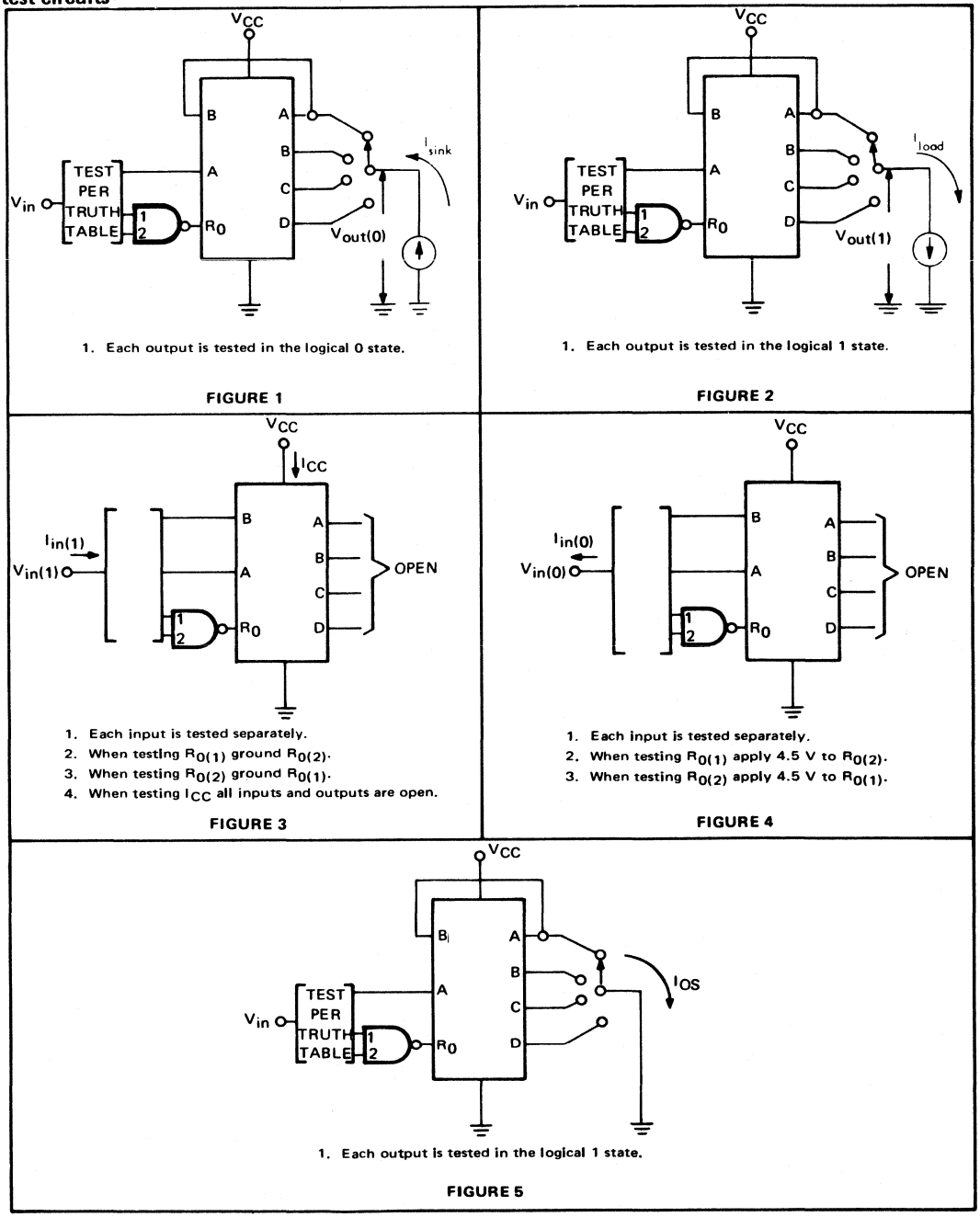
schematic



NOTES: 1. Component values shown are nominal.
2. All resistor values are in kΩ.

PARAMETER MEASUREMENT INFORMATION

d-c test circuits†



1. Each output is tested in the logical 0 state.

FIGURE 1

1. Each output is tested in the logical 1 state.

FIGURE 2

1. Each input is tested separately.
2. When testing $R_{0(1)}$ ground $R_{0(2)}$.
3. When testing $R_{0(2)}$ ground $R_{0(1)}$.
4. When testing I_{CC} all inputs and outputs are open.

FIGURE 3

1. Each input is tested separately.
2. When testing $R_{0(1)}$ apply 4.5 V to $R_{0(2)}$.
3. When testing $R_{0(2)}$ apply 4.5 V to $R_{0(1)}$.

FIGURE 4

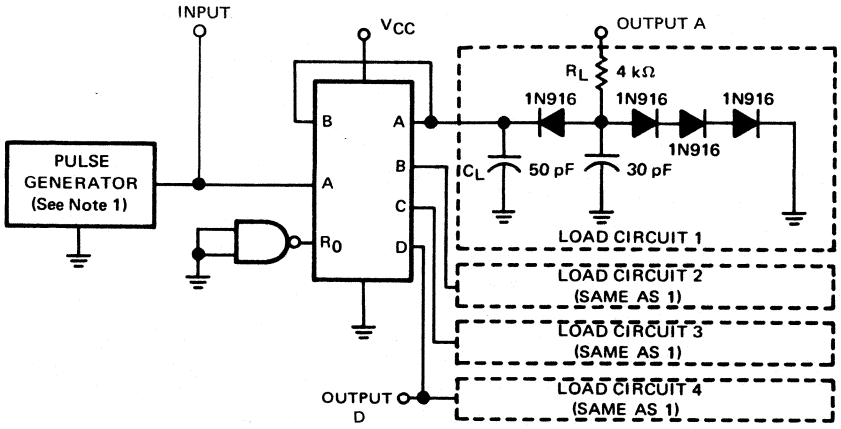
1. Each output is tested in the logical 1 state.

FIGURE 5

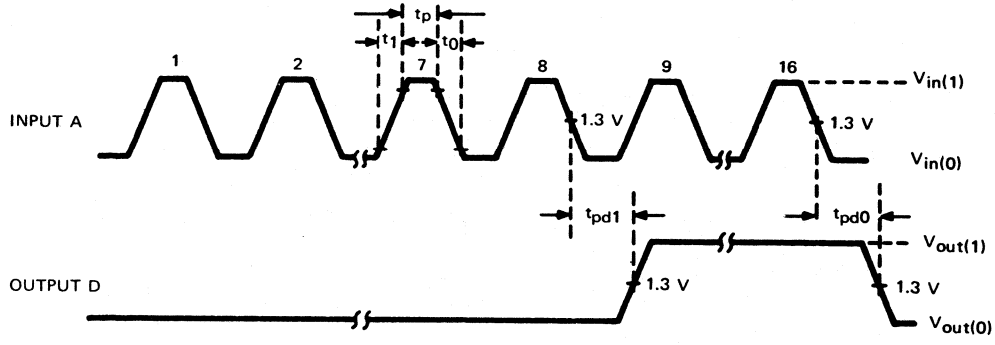
† Arrows indicate actual direction of current flow.

PARAMETER MEASUREMENT INFORMATION

switching characteristics



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES: 1. The pulse generator has the following characteristics: $t_0 = t_1 = 15$ ns, PRR = 500 kHz, $t_p \geqslant 200$ ns, and $Z_{out} \approx 50\ \Omega$.
2. Voltage values are with respect to network ground terminal.
3. C_L includes probe and jig capacitance.

FIGURE 6 – SWITCHING TIMES

Simplify Your Design of Complex Shift Registers and Counters with MSI/TTL Integrated Circuits

See Sections 8 and 9 for specifications, and Page B-1 for abstract and ordering information of Application Report CA-102.

CIRCUIT TYPES SN5491A, SN7491A
8-BIT SHIFT REGISTERS

MSI TTL SHIFT REGISTERS
for applications in

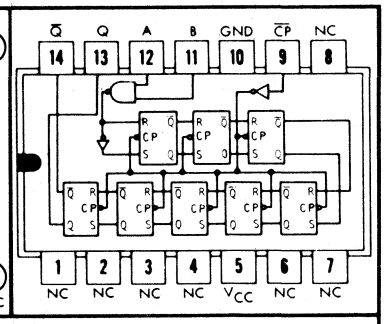
- Digital Computer Systems
- Data-Handling Systems
- Control Systems

logic

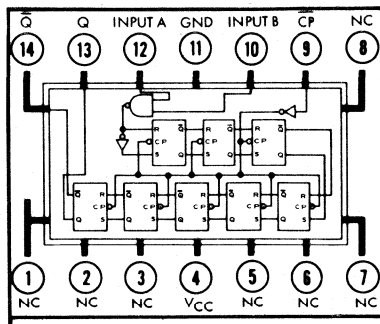
t_n		t_{n+8}
A	B	Q
0	0	0
0	1	0
1	0	0
1	1	1

NOTES:
1. t_n = bit time before clock.
2. t_{n+8} = bit time after 8 clock pulses.

J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



S
FLAT PACKAGE (TOP VIEW)



positive logic: See Truth Table

NC—No Internal Connection

description

These monolithic serial-in, serial-out, 8-bit shift registers utilizing transistor-transistor logic (TTL) circuits, are composed of eight R-S master-slave flip-flops, input gating, and a clock driver. The register is capable of storing and transferring data at clock rates up to 18 MHz while maintaining a typical noise-immunity level of 1 volt. Power dissipation is typically 175 milliwatts, and a full fan-out of 10 is available from the outputs.

Single-rail data and input control are gated through inputs A and B and an internal inverter to form the complementary inputs to the first bit of the shift register. Drive for the internal common clock line is provided by an inverting clock driver. Each of the inputs (A, B,and $\overline{CP}$) appear as only one TTL input load.

The clock pulse inverter/driver causes these circuits to shift information to the output on the positive edge of an input clock pulse, thus enabling the shift-register to be fully compatible with other edge-triggered synchronous functions.

absolute maximum ratings (over operating temperature range unless otherwise noted)

Supply Voltage V_{CC} (See Note 3) . . . . . 7 V
Input Voltage, V_{in} (See Notes 3 and 4) . . . . . 5.5 V
Operating Case Temperature Range: SN5491AS . . . . . −55°C to 125°C
Operating Free-Air Temperature Range: SN5491AJ, SN5491AN. . . . . −55°C to 125°C
SN7491A Circuits . . . . . 0°C to 70°C
Storage Temperature Range . . . . . −65°C to 150°C

NOTES: 3. These voltage values are with respect to network ground terminal.
4. Input signals must be zero or positive with respect to network ground terminal.

recommended operating conditions (over operating temperature range)

	MIN	NOM	MAX	UNIT
Supply Voltage V_{CC} (See Note 3): SN5491A Circuits	4.5	5	5.5	V
SN7491A Circuits	4.75	5	5.25	V
Normalized Fan-Out From Outputs			10	
Width of Clock Pulse, $t_{p(clock)}$ (See Figure 7)	25			ns
Input Setup Time, t_{setup} (See Figure 7)	25			ns
Input Hold Time, t_{hold} (See Figure 7)	0			

electrical characteristics (over operating temperature range unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
$V_{in(1)}$	Input voltage required to ensure logical 1 at any input terminal	1	V_{CC} = MIN		2			V
$V_{in(0)}$	Input voltage required to ensure logical 0 at any input terminal	2	V_{CC} = MIN				0.8	V
$V_{out(1)}$	Logical 1 output voltage	1	V_{CC} = MIN, I_{load} = −400 μA		2.4	3.5		V
$V_{out(0)}$	Logical 0 output voltage	2	V_{CC} = MIN, I_{sink} = 16 mA			0.22	0.4	V
$I_{in(0)}$	Logical 0 level input current	3	V_{CC} = MAX, V_{in} = 0.4 V				−1.6	mA
$I_{in(1)}$	Logical 1 level input current	4	V_{CC} = MAX, V_{in} = 2.4 V				40	μA
			V_{CC} = MAX, V_{in} = 5.5 V				1	mA
I_{OS}	Short-circuit output current§	5	V_{CC} = MAX, V_{out} = 0	SN5491A	−20		−57	mA
				SN7491A	−18		−57	mA
I_{CC}	Supply current	6	V_{CC} = MAX, V_{in} = 4.5 V	SN5491A		35	50	mA
				SN7491A		35	58	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable circuit type.

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

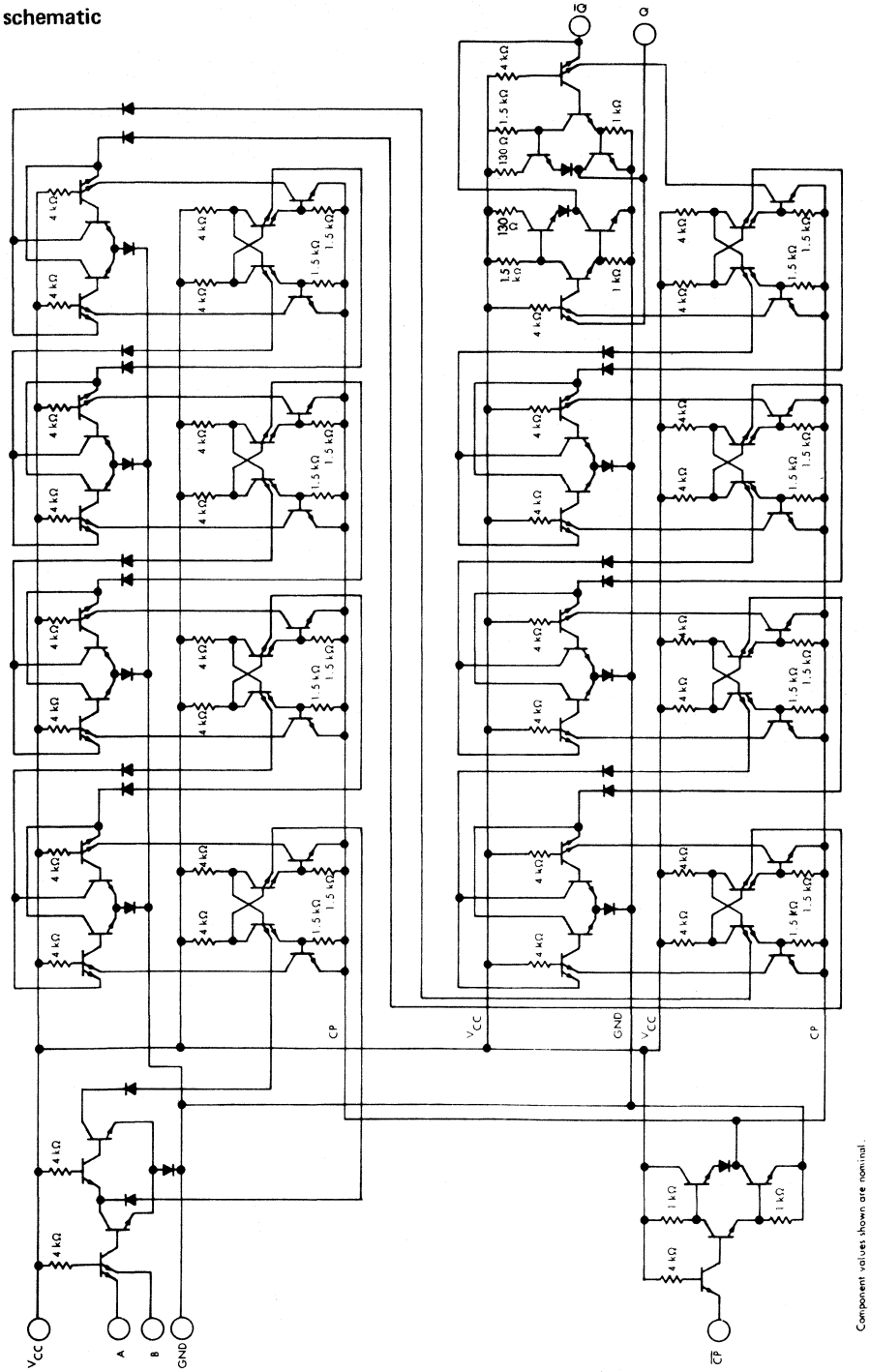
§ Not more than one output should be shorted at a time.

switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max}	Maximum shift frequency		C_L = 15 pF, R_L = 400 Ω	10	18		MHz
t_{pd1}	Propagation delay time to logical 1 level from clock to output	7	C_L = 15 pF, R_L = 400 Ω		24	40	ns
t_{pd0}	Propagation delay time to logical 0 level from clock to output	7	C_L = 15 pF, R_L = 400 Ω		27	40	ns

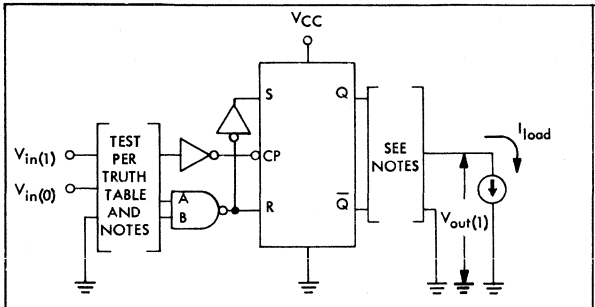
—SEE ORDERING INSTRUCTIONS PAGE 1-1—

schematic


Q̄
Q
4 kΩ
1.5 kΩ
130 Ω
1 kΩ
VCC
A
B
GND
CP
CP̄
Component values shown are nominal.

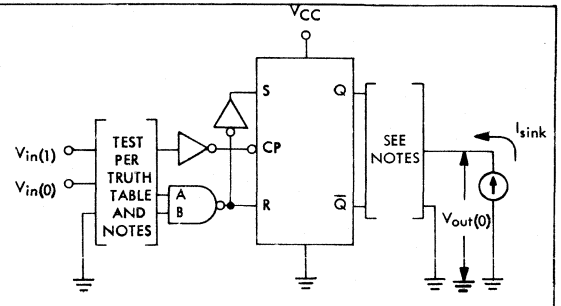
PARAMETER MEASUREMENT INFORMATION

d-c test circuits†



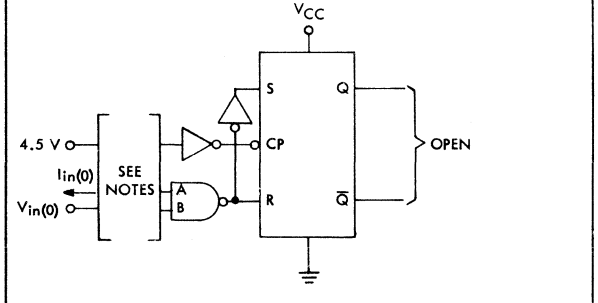
1. Each output is tested separately.
2. When testing $V_{out(1)}$ and I_{load}, ground all inputs and the unused output, then measure parameters specified.

FIGURE 1



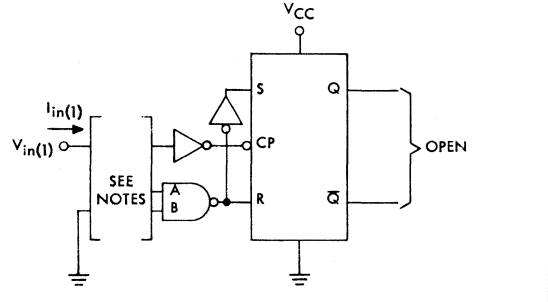
1. Each output is tested separately.
2. When testing $V_{out(0)}$ and I_{sink}, ground all inputs. Apply a momentary ground to the output to be tested then measure parameters specified.

FIGURE 2



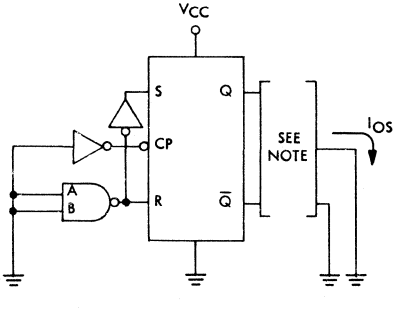
1. When testing input A apply 4.5 V to input B.
2. When testing input B apply 4.5 V to input A.

FIGURE 3



1. When testing input A ground input B.
2. When testing input B ground input A.

FIGURE 4



1. Ground the unused output then measure parameter specified.

FIGURE 5

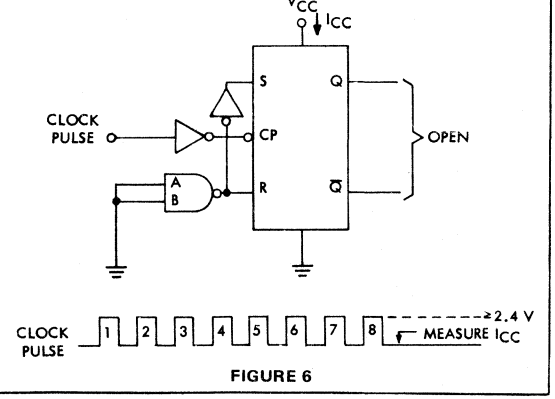
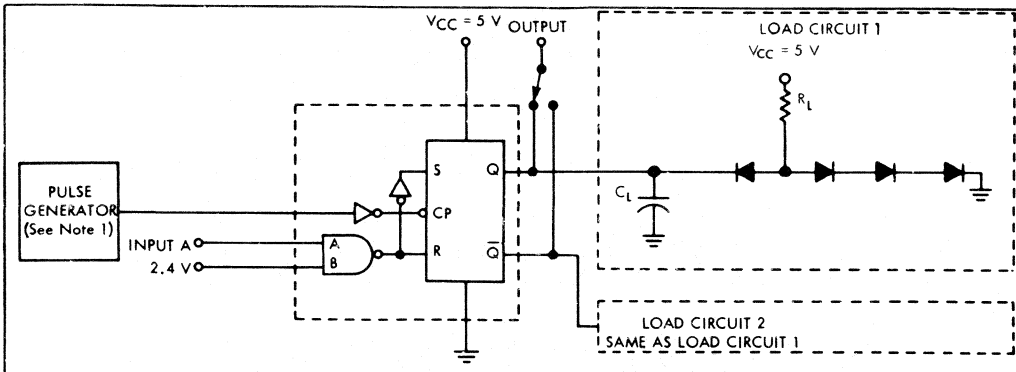


FIGURE 6

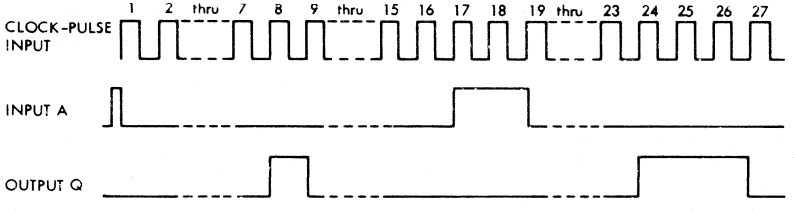
† Arrows indicate actual direction of current flow.

PARAMETER MEASUREMENT INFORMATION

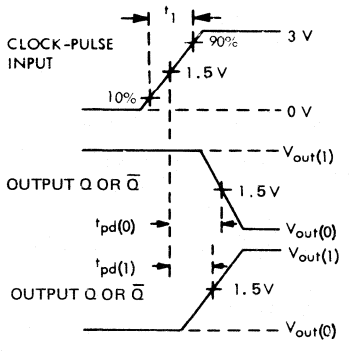
switching characteristics



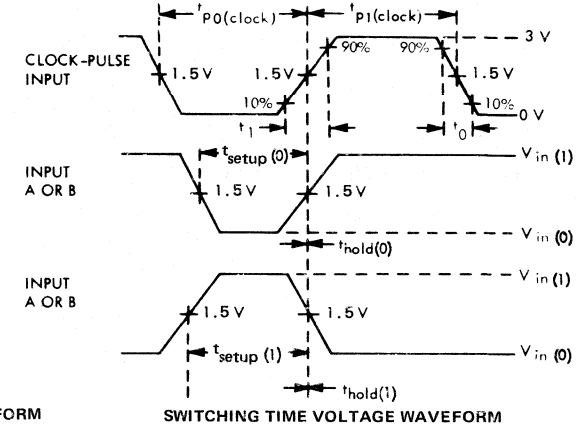
TEST CIRCUIT



TYPICAL INPUT/OUTPUT WAVEFORMS



PROPAGATION DELAY TIME VOLTAGE WAVEFORM



SWITCHING TIME VOLTAGE WAVEFORM

NOTES: 1. The generator has the following characteristics: $V_{in(0)} \leq 0.3$ V, $V_{in(1)} \geq 2.4$ V, $t_t = t_0 = 10$ ns, $t_{p1(clock)} = 500$ ns, $t_{p0(clock)} = 500$ ns, PRR = 1 MHz, and $Z_{out} \approx 50\ \Omega$.
2. C_L includes probe and jig capacitance.
3. Each output is tested separately.
4. Voltage values are with respect to network ground terminal.
5. All diodes are 1N3064.

FIGURE 7 -- SN5491A/SN7491A SWITCHING TIMES

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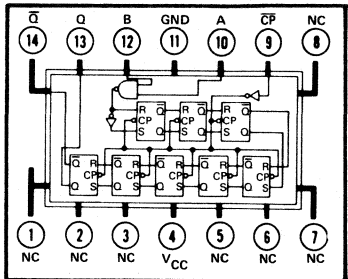
CIRCUIT TYPES SN54L91, SN74L91
8-BIT SHIFT REGISTERS

logic

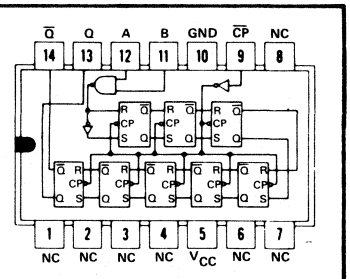
TRUTH TABLE		
t_n		t_{n+8}
A	B	Q
0	0	0
0	1	0
1	0	0
1	1	1

NOTES:
1. t_n = Bit time before clock pulse.
2. t_{n+8} = Bit time after 8 clock pulses.
3. NC — No internal connection.

T
FLAT PACKAGE (TOP VIEW)



J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



positive logic: see truth table

description

This monolithic serial-in, serial-out, 8-bit shift register utilizes low-power transistor-transistor logic (TTL) circuits. The shift register, composed of eight R-S master-slave flip-flops, includes input gating and a clock driver. The register is capable of storing and transferring data at typical clock rates of 6.5 MHz while maintaining a typical noise-immunity level of 0.9 volt. Power dissipation is typically 17.5 milliwatts, and full fan-out of 10 is available from the outputs.

Single-rail data and input control are gated through inputs A and B and an internal inverter to form the complementary inputs to the first bit of the shift register. Drive for the internal common clock line is provided by an inverting clock driver. Each of the inputs (A, B, and clock) appear as only one low-power TTL input load.

The clock pulse inverter/driver causes the register to shift information to the output on the positive edge of an input clock pulse, thus enabling the shift register to be fully compatible with edge-triggering flip-flops.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply Voltage V_{CC}: SN54L91 Circuits	4.5	5	5.5	V
SN74L91 Circuits	4.75	5	5.25	V
Normalized Fan-Out From Each Output, N			10	
Input Setup Time, t_{setup} (See Figure 7)	120			ns
Input Hold Time, t_{hold} (See Figure 7)	0			
Width of Logical 0 Level Clock Pulse, $t_{p0(clock)}$ (See Figure 7)	150			ns
Width of Logical 1 Level Clock Pulse, $t_{p1(clock)}$ (See Figure 7)	100			ns
Operating Free-Air Temperature Range, T_A: SN54L91 Circuits	−55	25	125	°C
SN74L91 Circuits	0	25	70	°C

absolute maximum ratings (over recommended operating free-air temperature when otherwise noted)

Supply Voltage V_{CC} (See Note 1) . . . . . 8 V
Input Voltage, V_{in} (See Notes 1 and 2) . . . . . 5.5 V
Operating Free-Air Temperature Range: SN54L91 Circuits . . . . . −55°C to 125°C
SN74L91 Circuits . . . . . 0°C to 70°C
Storage Temperature Range . . . . . −65°C to 150°C

NOTES: 1. Voltage values are with respect to network ground terminal.
2. Input signals must be zero or positive with respect to network ground terminal.

electrical characteristics (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS†	MIN	MAX	UNIT
$V_{in(1)}$	Input voltage required to ensure logical 1 at any input terminal	1	V_{CC} = MIN	2		V
$V_{in(0)}$	Input voltage required to ensure logical 0 at any input terminal	2	V_{CC} = MIN		0.7	V
$V_{out(1)}$	Logical 1 output voltage	1	V_{CC} = MIN, I_{load} = −100 μA	2.4		V
$V_{out(0)}$	Logical 0 output voltage	2	V_{CC} = MIN, I_{sink} = 2 mA		0.3	V
$I_{in(0)}$	Logical 0 level input current	3	V_{CC} = MAX, V_{in} = 0.3 V		-0.18	mA
$I_{in(1)}$	Logical 1 level input current	4	V_{CC} = MAX, V_{in} = 2.4 V		10	μA
			V_{CC} = MAX, V_{in} = 5.5 V		100	μA
I_{OS}	Short-circuit output current	5	V_{CC} = MAX, V_{in} = 0, V_{out} = 0	−3	−15	mA
I_{CC}	Supply current	6	V_{CC} = MAX, V_{in} = 5 V		6.6	mA

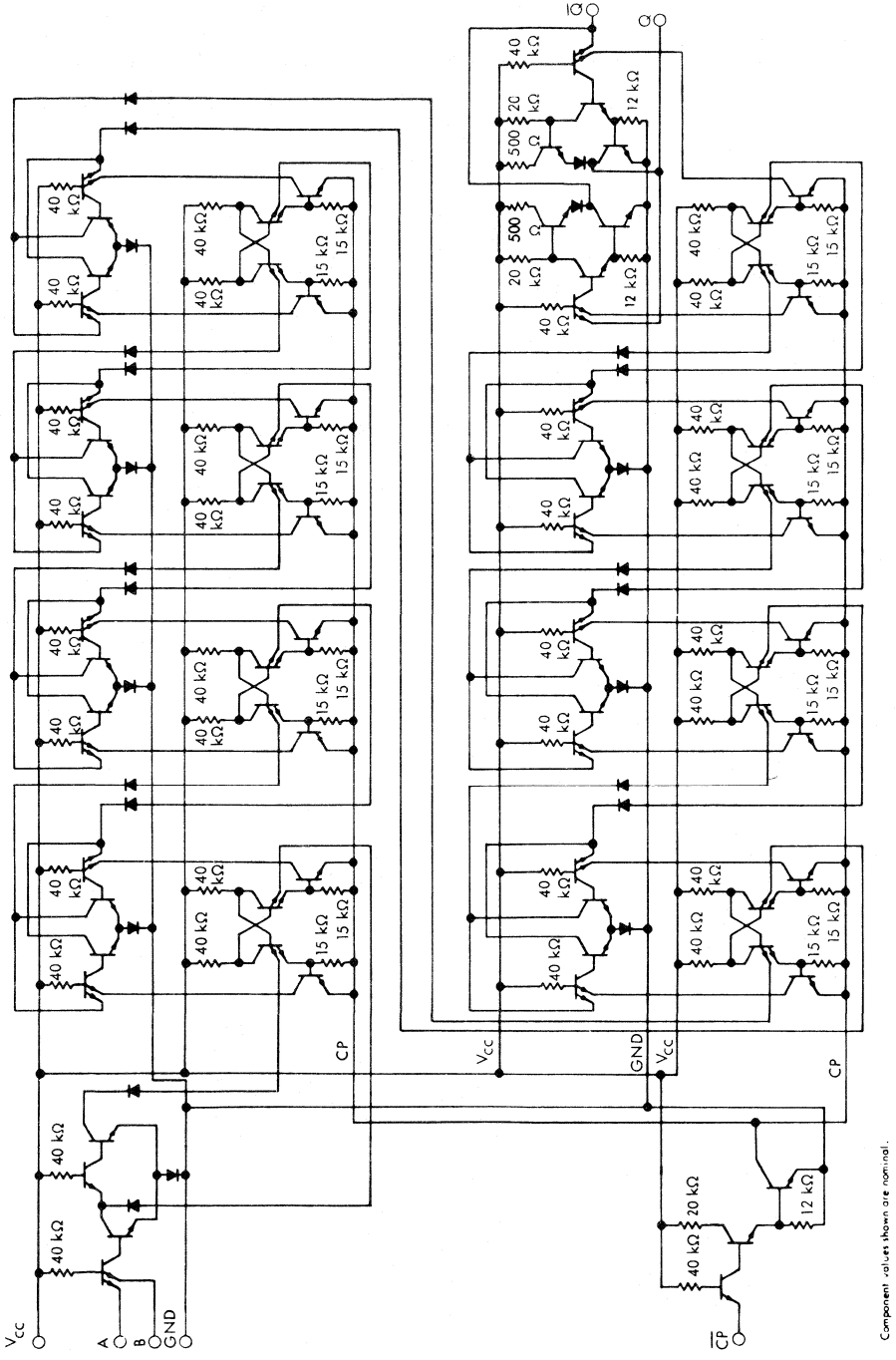
†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable circuit type.

switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{p0(clock)}$	Minimum width of logical 0 level clock pulse	7	C_L = 50 pF, R_L = 4 kΩ		105		ns
$t_{p1(clock)}$	Minimum width of logical 1 level clock pulse	7	C_L = 50 pF, R_L = 4 kΩ		45		ns
t_{pd0}	Propagation delay time to logical 0 level from clock to output	7	C_L = 50 pF, R_L = 4 kΩ		100	150	ns
t_{pd1}	Propagation delay time to logical 1 level from clock to output	7	C_L = 50 pF, R_L = 4 kΩ		55	100	ns

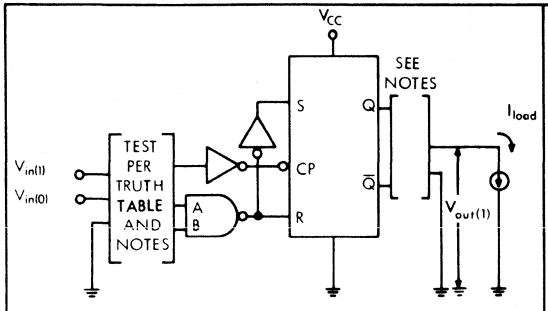
—SEE ORDERING INSTRUCTIONS PAGE 1-1—

schematic


Q
40 kΩ
2C kΩ
500 Ω
12 kΩ
20 kΩ
15 kΩ
CP
V_{CC}
GND
A
B
Component values shown are nominal.

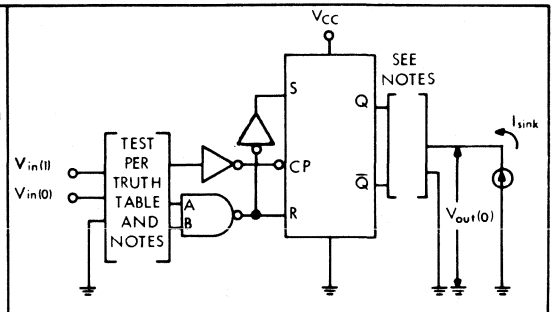
PARAMETER MEASUREMENT INFORMATION

d-c test circuits§



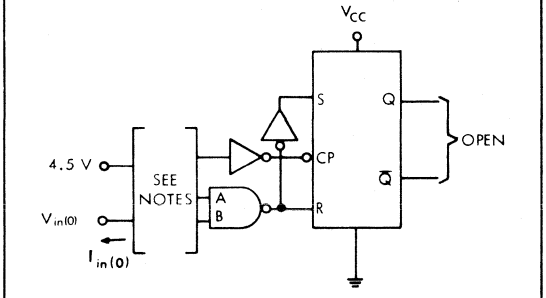
1. Each output is tested separately.
2. When testing $V_{out(1)}$ and I_{load}, ground all inputs and momentarily ground the unused output, then measure parameters specified.

FIGURE 1



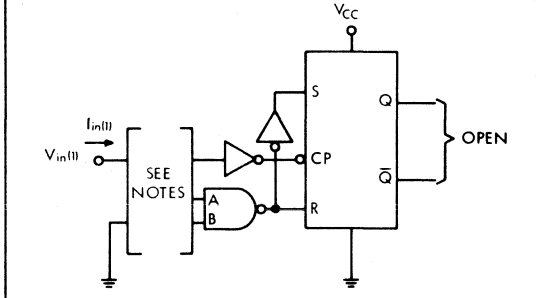
1. Each output is tested separately.
2. When testing $V_{out(0)}$ and I_{sink}, ground all inputs. Apply a momentary ground to the output to be tested, then measure parameters specified.

FIGURE 2



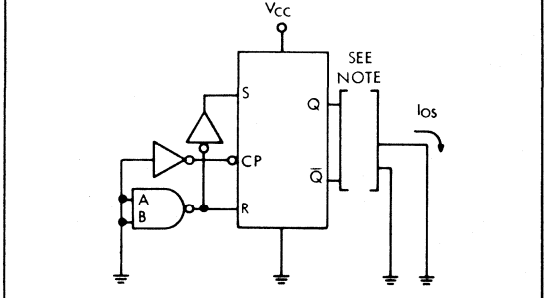
1. When testing input A apply 4.5 V to input B.
2. When testing input B apply 4.5 V to input A.

FIGURE 3



1. When testing input A ground input B.
2. When testing input B ground input A.

FIGURE 4



1. Ground the unused output, then measure parameters specified.

FIGURE 5

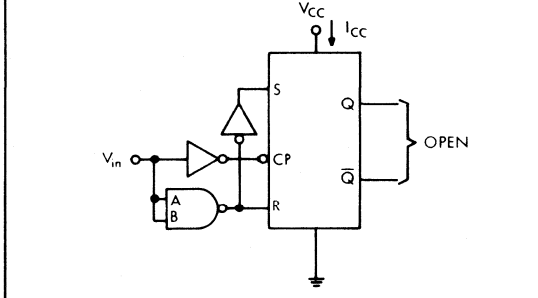
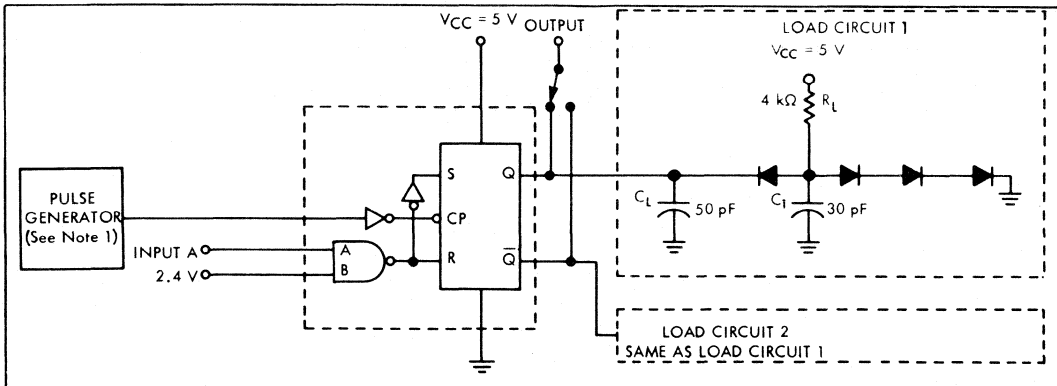


FIGURE 6

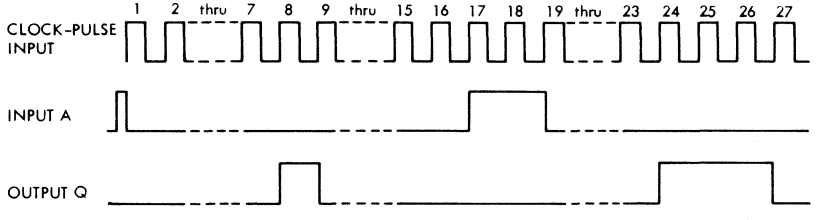
§Arrows indicate actual direction of current flow.

PARAMETER MEASUREMENT INFORMATION

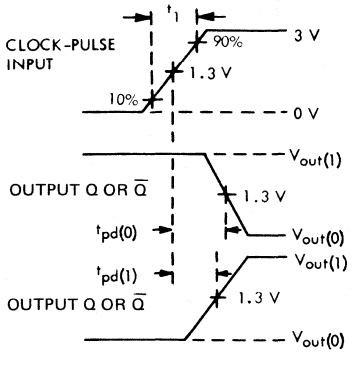
switching characteristics



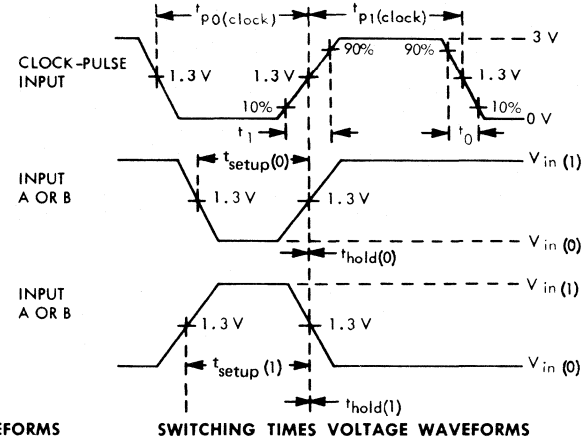
TEST CIRCUIT



TYPICAL INPUT/OUTPUT WAVEFORMS



PROPAGATION DELAY TIMES VOLTAGE WAVEFORMS

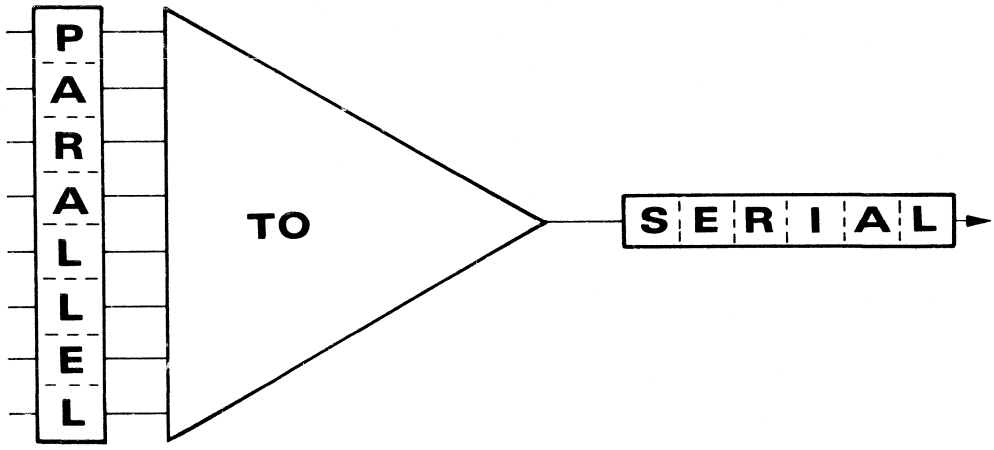


SWITCHING TIMES VOLTAGE WAVEFORMS

NOTES: 1. The generator has the following characteristics: $V_{in(0)} \leq 0.3$ V, $V_{in(1)} \geq 2.4$ V, $t_r = t_f = 15$ ns, $t_{p1(clock)} = 500$ ns, $t_{p0(clock)} = 500$ ns, PRR = 1 MHz, and $Z_{out} \approx 50\ \Omega$.
2. C_L includes probe and jig capacitance.
3. Each output is tested separately.
4. Voltage values are with respect to network ground terminal.
5. All diodes are 1N916.

FIGURE 7 – SN54L91/SN74L91 SWITCHING TIMES

At Some Time You Must Go...



Six New MSI Data Selectors/Multiplexers

Simplify the job

See Page 10-1

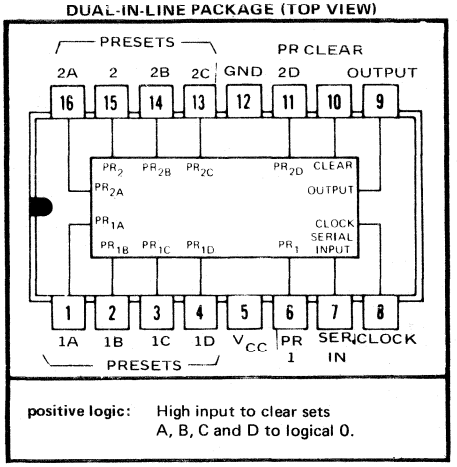
CIRCUIT TYPES SN5494, SN7494
4-BIT SHIFT REGISTERS

TTL MSI PARALLEL-IN SERIAL-OUT REGISTERS

for application as

- Dual-Source, Parallel-To-Serial Converter
- Serial-In Serial-Out Register

J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



positive logic: High input to clear sets A, B, C and D to logical 0.

description

This monolithic shift register, utilizing transistor-transistor logic (TTL) circuits in the familiar Series 74 configuration, is composed of four R-S master-slave flip-flops, four AND-OR-INVERT gates, and four inverter-drivers. Internal interconnections of these functions provide a versatile register which performs right-shift operations as a serial-in, serial-out register or as a dual-source, parallel-to-serial converter. A number of these registers may be connected in series to form an n-bit register.

All flip-flops are simultaneously set to the logical 0 state by applying a logical 1 voltage to the clear input. This condition may be applied independent of the state of the clock input, but not independent of state of the preset input. Preset input is independent of the clock and clear states.

The flip-flops are simultaneously set to the logical 1 state from either of two preset input sources. Preset inputs 1A through 1D are activated during the time that a positive pulse is applied to preset 1 if preset 2 is at a logical 0 level. When the logic levels at preset 1 and preset 2 are reversed, preset inputs 2A through 2D are active.

Transfer of information to the outputs occurs when the clock input goes from a logical 0 to a logical 1. Since the flip-flops are R-S master-slave circuits, the proper information must appear at the R-S inputs of each flip-flop prior to the rising edge of the clock input waveform. The serial input provides this information for the first flip-flop. The outputs of the subsequent flip-flops provide information for the remaining R-S inputs. The clear input and either preset 1 or preset 2 must be at a logical 0 when clocking occurs.

This register is completely compatible for use with TTL and DTL logic circuits and when used with other TTL circuits, noise margins are typically one volt. Typical average power dissipation is 175 milliwatts, and propagation delay times from clock to output are typically 25 nanoseconds.

absolute maximum ratings (over operating temperature range unless otherwise noted)

Supply Voltage V_{CC} (See Note 1)		7 V
Input Voltage V_{in} (See Notes 1 and 2)		5.5 V
Operating Free-Air Temperature Range:	SN5494 Circuits	−55°C to 125°C
	SN7494 Circuits	0°C to 70°C
Storage Temperature Range		−65°C to 150°C

NOTES: 1. The voltage values are with respect to network ground terminal.
2. Input signals must be zero or positive with respect to network ground terminal.

PRELIMINARY DATA SHEET:
Supplementary data will be published at a later date.

recommended operating conditions (over operating temperature range)

	MIN	TYP	MAX	UNIT
Supply Voltage V_{CC} (See Note 1): SN5494 Circuits	4.5	5	5.5	V
SN7494 Circuits	4.75	5	5.25	V
Normalized Fan-Out From Each Output			10	
Width of Clock Pulse, $t_{p(clock)}$	35			ns
Width of Clear Pulse, $t_{p(clear)}$	30			ns
Width of Preset Pulse, $t_{p(preset)}$	30			ns
Serial Input Setup Time: $t_{setup(1)}$	35			ns
$t_{setup(0)}$	25			ns
Serial Input Hold Time, t_{hold}	0			

NOTE: 1. These voltage values are with respect to network ground terminal.

electrical characteristics (over operating temperature range unless otherwise noted)

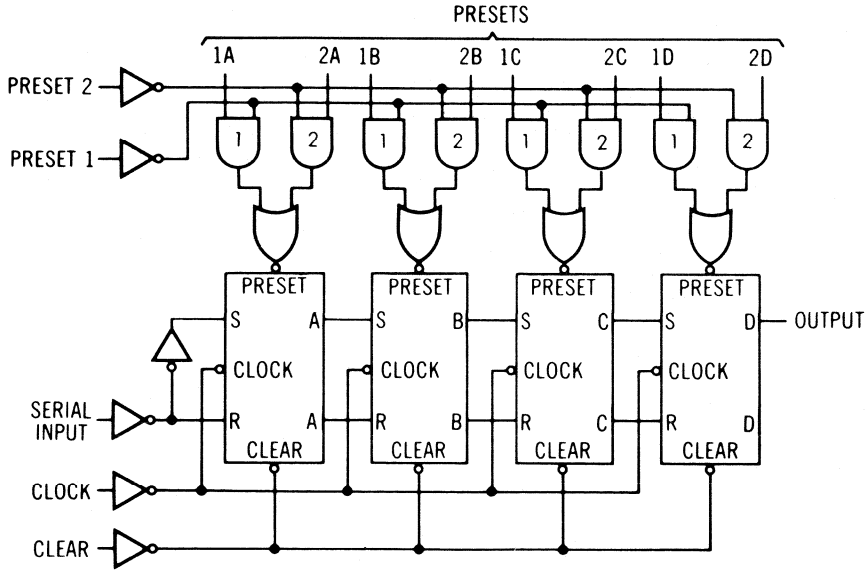
	PARAMETER	TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
$V_{in(1)}$	Input voltage required to ensure logical 1 at any input terminal	V_{CC} = MIN		2			V
$V_{in(0)}$	Input voltage required to ensure logical 0 at any input terminal	V_{CC} = MIN				0.8	V
$V_{out(1)}$	Logical 1 output voltage	V_{CC} = MIN, I_{load} = −400 μA		2.4	3.5		V
$V_{out(0)}$	Logical 0 output voltage	V_{CC} = MIN, I_{sink} = 16 mA			0.22	0.4	V
$I_{in(1)}$	Logical 1 level input current at any input except preset 1 and preset 2	V_{CC} = MAX, V_{in} = 2.4 V				40	μA
		V_{CC} = MAX, V_{in} = 5.5 V				1	mA
$I_{in(1)}$	Logical 1 level input current at preset 1 and preset 2	V_{CC} = MAX, V_{in} = 2.4 V				160	μA
		V_{CC} = MAX, V_{in} = 5.5 V				1	mA
$I_{in(0)}$	Logical 0 level input current at any input except preset 1 and preset 2	V_{CC} = MAX, V_{in} = 0.4 V				−1.6	mA
$I_{in(0)}$	Logical 0 level input current at preset 1 and preset 2	V_{CC} = MAX, V_{in} = 0.4 V				−6.4	mA
I_{OS}	Short-circuit input current§	V_{CC} = MAX, V_{out} = 0	SN5494	−20		−57	mA
			SN7494	−18		−57	mA
I_{CC}	Supply current	V_{CC} = MAX	SN5494		35	50	mA
			SN7494		35	58	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the particular circuit type.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time.

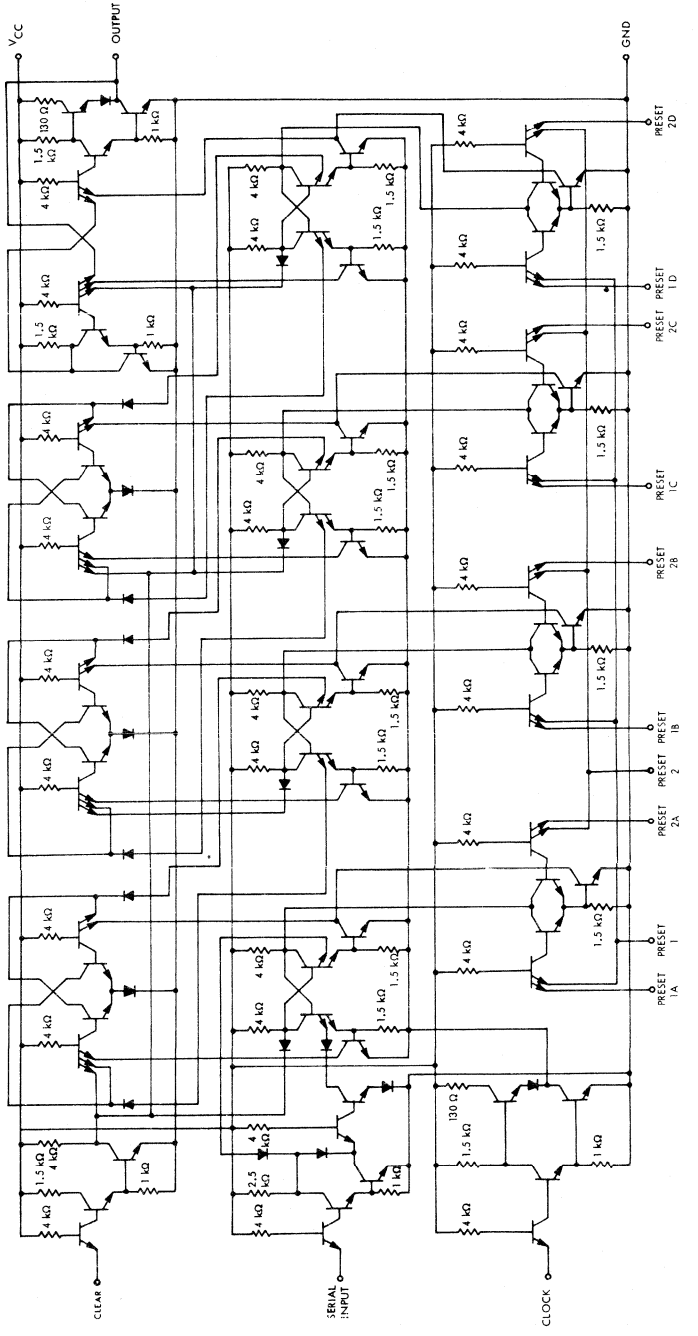
switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max}	Maximum clock frequency	C_L = 15 pF, R_L = 400 Ω	10			MHz
t_{pd1}	Propagation delay time to logical 1 level from clock to output to output	C_L = 15 pF, R_L = 400 Ω		25	40	ns
t_{pd0}	Propagation delay time to logical 0 level from clock to output	C_L = 15 pF, R_L = 400 Ω		25	40	ns
t_{pd1}	Propagation delay time to logical 1 level from preset to output	C_L = 15 pF, R_L = 400 Ω			35	ns
t_{pd0}	Propagation delay time to logical 0 level from clear to output	C_L = 15 pF, R_L = 400 Ω			40	ns

functional block diagram



schematic



Component values shown are nominal.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

CIRCUIT TYPES SN54L95, SN74L95
4-BIT RIGHT-SHIFT LEFT-SHIFT REGISTERS

A SERIES 54L/74L PARALLEL-IN PARALLEL-OUT REGISTER
for application as

- N-Bit Serial-To-Parallel Converter
- N-Bit Parallel-To-Serial Converter
- N-Bit Storage Register

description

This monolithic shift register, utilizing transistor-transistor logic (TTL) circuits in the familiar Series 54L/74L configuration, is composed of four R-S master-slave flip-flops, four AND-OR-INVERT gates, one AND-OR gate, and six inverter-drivers. Internal interconnections of these functions provide a versatile register which will perform right-shift or left-shift operations dependent upon the logical input level to the mode control. A number of these registers may be connected in series to form an n-bit right-shift or left-shift register. This register can also be used as a parallel-in, parallel-out storage register with gate (mode) control.

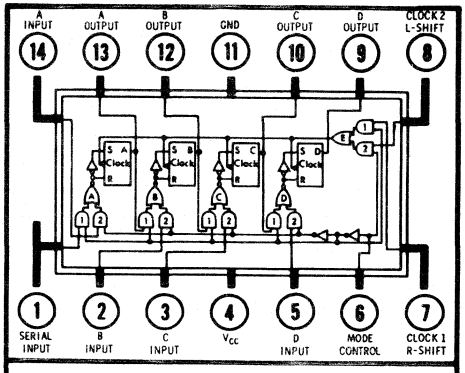
When a logical 0 level is applied to the mode control input, the number 1 AND gates are enabled and the number 2 AND gates are inhibited. In this mode the output of each flip-flip is coupled to the R-S inputs of the succeeding flip-flop, right-shift operation is performed by clocking at the clock 1 input, and serial data is entered at the serial input. Clock 2 and parallel inputs A through D are inhibited by the number 2 AND gates.

When a logical 1 level is applied to the mode-control input, the number 1 AND gates are inhibited (decoupling the outputs from the succeeding R-S inputs to prevent right-shift) and the number 2 AND gates are enabled to allow entry of data through parallel inputs A through D and clock 2. This mode permits parallel loading of the register or, with external interconnection, shift-left operation. In this mode, shift-left can be accomplished by connecting the output of each flip-flop to the parallel input of the previous flip-flop (D output to input C, and etc.), and serial data is entered at input D.

Clocking for the shift register is accomplished through the AND-OR gate E which permits separate clock sources to be used for the shift-right and shift-left modes. If both modes can be clocked from the same source, the clock input may be applied commonly to clock 1 and clock 2. Information must be present at the R-S inputs of the master-slave flip-flops prior to clocking.

The shift register is completely compatible for use with TTL and DTL logic families. Average power dissipation is typically 19 milliwatts.

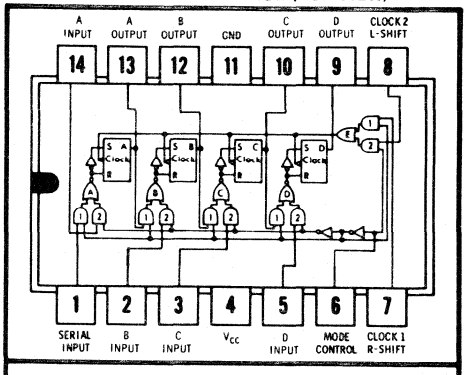
S
FLAT PACKAGE (TOP VIEW)



positive logic

Mode Control = 0 for right shift
Mode Control = 1 for left shift or parallel load

J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



positive logic

Mode Control = 0 for right shift
Mode Control = 1 for left shift or parallel load

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply Voltage V_{CC} (See Note 1) . . . . . 8 V
Input Voltage, V_{in} (See Notes 1 and 2) . . . . . 5.5 V
Operating Free-Air Temperature Range: SN54L95 Circuits . . . . . -55°C to 125°C
SN74L95 Circuits . . . . . 0°C to 70°C
Storage Temperature Range . . . . . -65°C to 150°C

NOTES: 1. Voltage values are with respect to network ground terminal.
2. Input voltages must be zero or positive with respect to network ground terminal.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply Voltage V_{CC} (See Note 1): SN54L95 Circuits	4.5	5	5.5	V
SN74L95 Circuits	4.75	5	5.25	V
Normalized Fan-Out From Each Output			10	
Width of Clock Pulse, $t_{p(clock)}$ (See Figure 9)	200			ns
Logical 1 Setup Time Required at Serial, A, B, C, or D Inputs, $t_{setup(1)}$ (See Figure 9)	100			ns
Logical 0 Setup Time Required at Serial, A, B, C, or D Inputs, $t_{setup(0)}$	120			ns
Hold Time Required at Serial, A, B, C, or D Inputs, t_{hold} (See Figure 9)	0			ns
Logical 0 Level Setup Time Required at Mode Control (t1 in Figure 10) (With Respect to Clock 1 Input)	225			ns
Logical 1 Level Setup Time Required at Mode Control (t2 in Figure 10) (With Respect to Clock 2 Input)	200			ns
Logical 0 Level Setup Time Required at Mode Control (t3 in Figure 10) (With Respect to Clock 2 Input)	0			ns
Logical 1 Level Setup Time Required at Mode Control (t4 in Figure 10) (With Respect to Clock 1 Input)	100			ns

NOTE: 1. Voltage values are with respect to network ground terminal.

electrical characteristics (over operating free-air temperature range unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS †	MIN	TYP‡	MAX	UNIT
$V_{in(1)}$	Input voltage required to ensure logical 1 at any input terminal	1 and 3	V_{CC} = MIN	2			V
$V_{in(0)}$	Input voltage required to ensure logical 0 at any input terminal	2 and 4	V_{CC} = MIN			0.7	V
$V_{out(1)}$	Logical 1 output voltage	1 and 3	V_{CC} = MIN, $V_{in(1)}$ = 2 V, $V_{in(0)}$ = 0.7 V, I_{load} = −100 μA	2.4			V
$V_{out(0)}$	Logical 0 output voltage	2 and 4	V_{CC} = MIN, $V_{in(1)}$ = 2 V, $V_{in(0)}$ = 0.7 V, I_{sink} = 2 mA		0.16	0.3	V
$I_{in(0)}$	Logical 0 level input current at any input except mode control	5	V_{CC} = MAX, V_{in} = 0.3 V			-0.18	mA
$I_{in(0)}$	Logical 0 level input current at mode control	5	V_{CC} = MAX, V_{in} = 0.3 V			-0.36	mA
$I_{in(1)}$	Logical 1 level input current at any input except mode control	6	V_{CC} = MAX, V_{in} = 2.4 V			10	μA
			V_{CC} = MAX, V_{in} = 5.5 V			100	μA
$I_{in(1)}$	Logical 1 level input current at mode control	6	V_{CC} = MAX, V_{in} = 2.4 V			20	μA
			V_{CC} = MAX, V_{in} = 5.5 V			200	μA
I_{OS}	Short-circuit output current §	7	V_{CC} = MAX, V_{in} = 4.5 V	-3		-15	mA
I_{CC}	Supply current	8	V_{CC} = MAX, $V_{in(1)}$ = 4.5 V, $V_{in(0)}$ = 0		3.8	9	mA

† For conditions shown as MIN or MAX use the appropriate value specified under recommended operating conditions for the applicable device type.

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

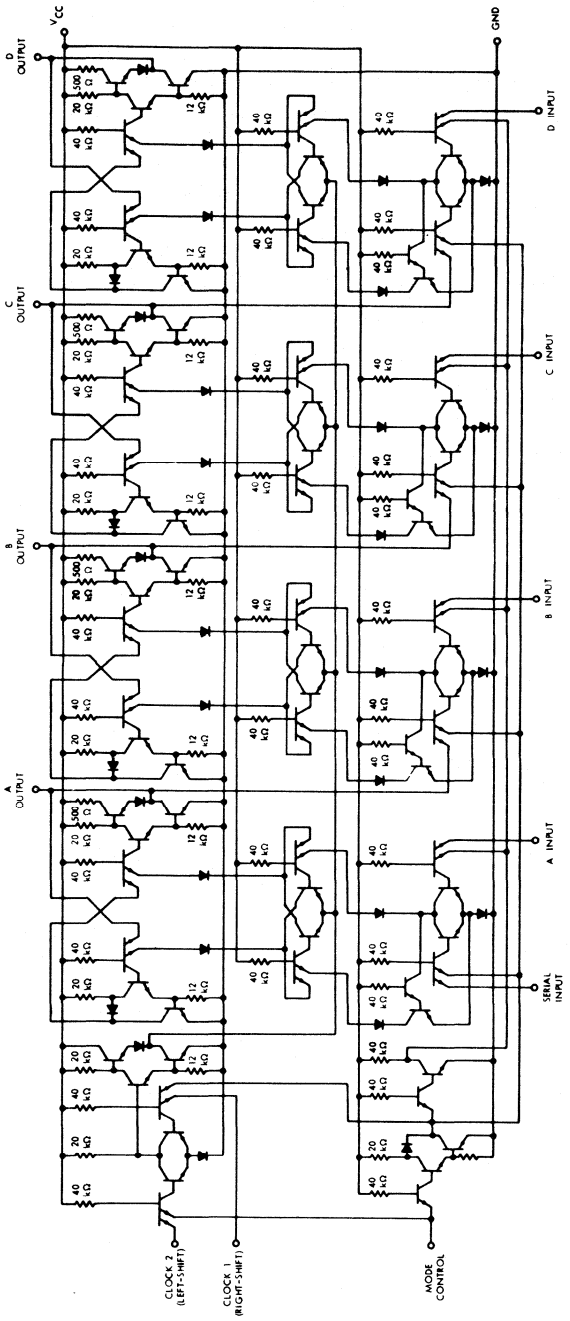
§ Not more than one output should be shorted at a time.

switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max}	Maximum shift frequency	9	C_L = 50 pF, R_L = 4 kΩ	3	5		MHz
t_{pd1}	Propagation delay time to logical 1 level from clock 1 or clock 2 to outputs	9	C_L = 50 pF, R_L = 4 kΩ		115	200	ns
t_{pd0}	Propagation delay time to logical 0 level from clock 1 or clock 2 to outputs	9	C_L = 50 pF, R_L = 4 kΩ		125	200	ns

—SEE ORDERING INSTRUCTIONS PAGE 1-1—

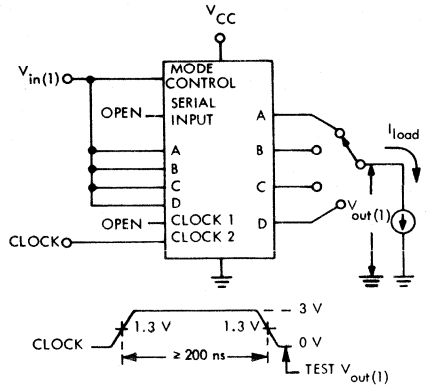
schematic



NOTE: Component values shown are nominal.

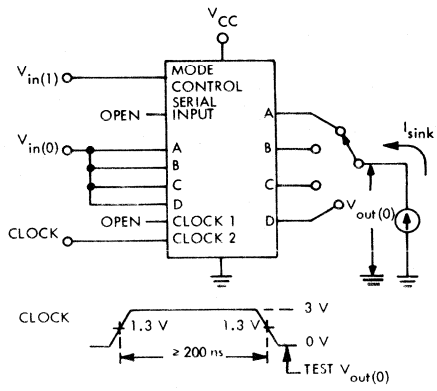
PARAMETER MEASUREMENT INFORMATION

d-c test circuits†



1. Each output is tested separately.

FIGURE 1



1. Each output is tested separately.

FIGURE 2

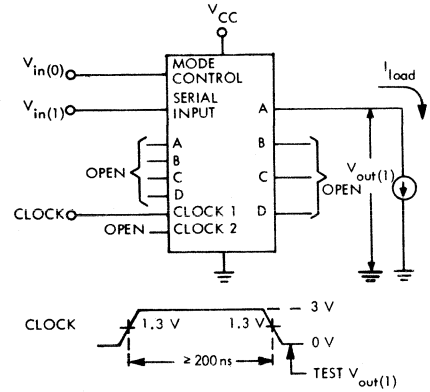


FIGURE 3

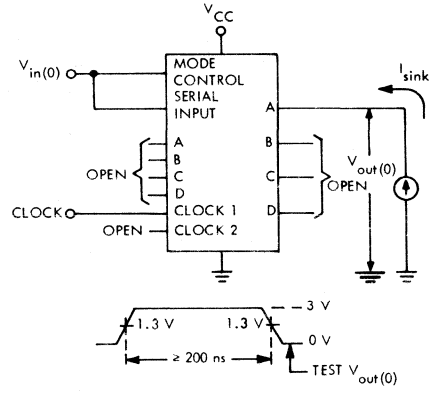
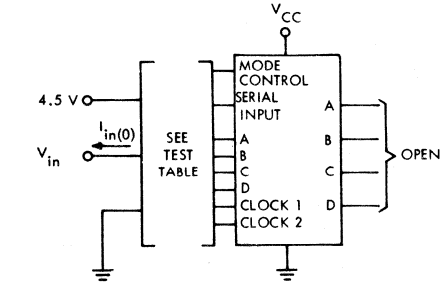


FIGURE 4



1. Each input is tested separately.

TEST TABLE

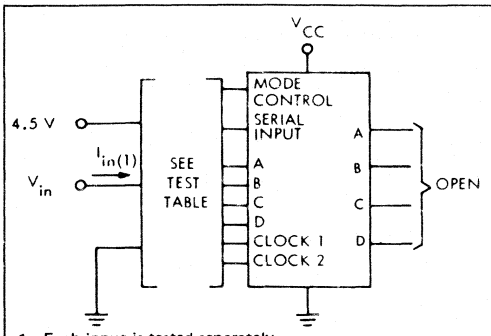
TEST	APPLY 4.5 V	APPLY GND
MODE CONTROL	CLOCK 2	NONE
SERIAL INPUT	NONE	MODE CONTROL
A INPUT	MODE CONTROL	NONE
B INPUT	MODE CONTROL	NONE
C INPUT	MODE CONTROL	NONE
D INPUT	MODE CONTROL	NONE
CLOCK 1	NONE	MODE CONTROL
CLOCK 2	MODE CONTROL	NONE

FIGURE 5

† Arrows indicate actual direction of current flow.

PARAMETER MEASUREMENT INFORMATION

d-c test circuits† (continued)

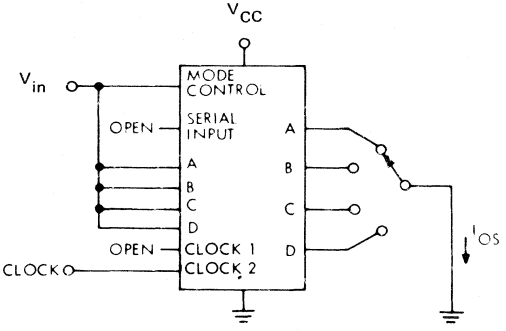


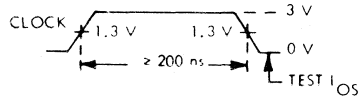
TEST TABLE

TEST	APPLY 4.5 V	APPLY GND
MODE CONTROL	NONE	CLOCK 2
SERIAL INPUT	MODE CONTROL	NONE
A INPUT	NONE	MODE CONTROL
B INPUT	NONE	MODE CONTROL
C INPUT	NONE	MODE CONTROL
D INPUT	NONE	MODE CONTROL
CLOCK 1	MODE CONTROL	NONE
CLOCK 2	NONE	MODE CONTROL

1. Each input is tested separately.

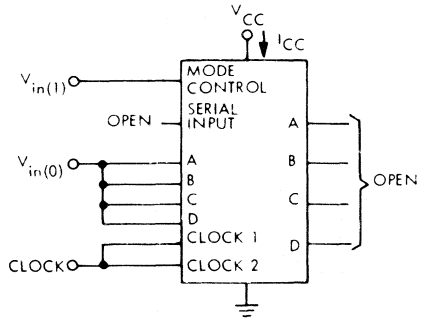
FIGURE 6





1. Each output is tested separately.

FIGURE 7



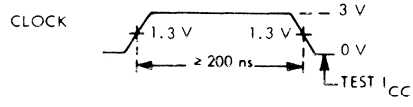
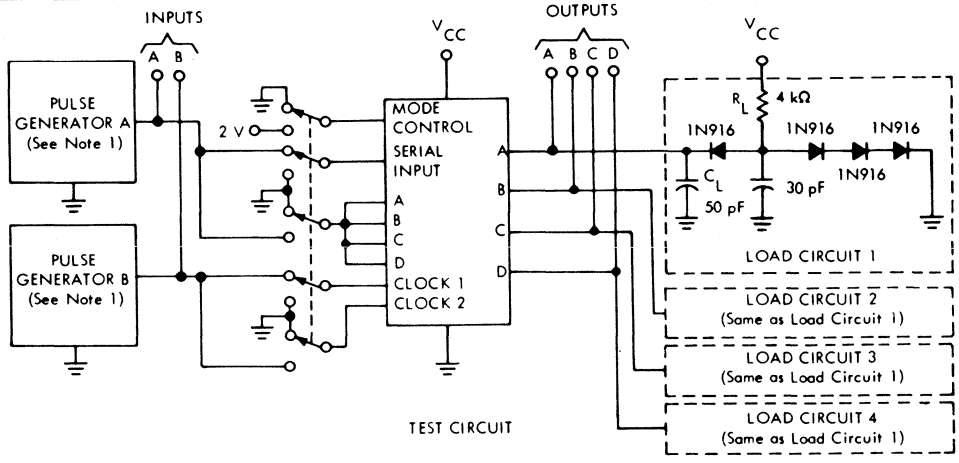


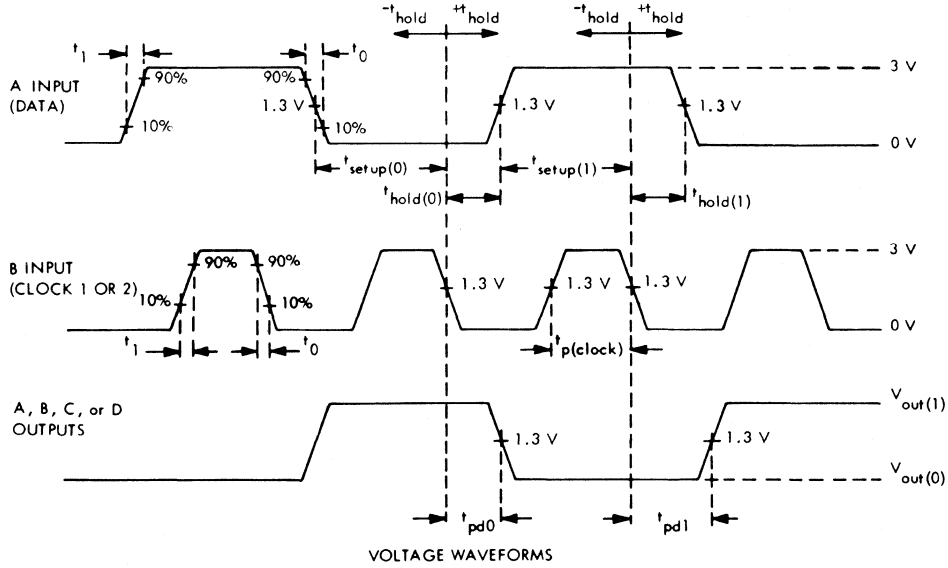
FIGURE 8

† Arrows indicate actual direction of current flow.

PARAMETER MEASUREMENT INFORMATION

switching characteristics



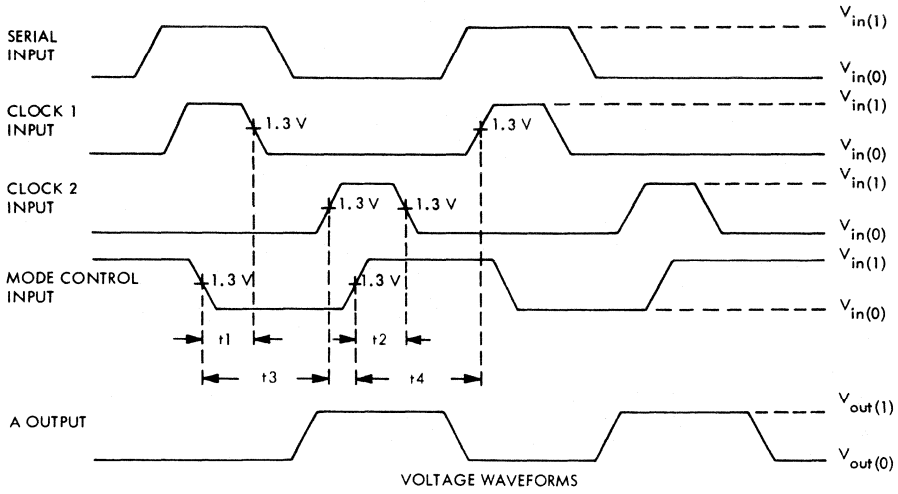


NOTES: 1. The pulse generators have the following characteristics: t_1 = 10 ns to 12 ns, t_0 = 10 ns to 12 ns, and $Z_{out} \approx 50\ \Omega$.
For pulse generator A : $t_p \geqslant 150$ ns and PRR = 500 kHz. For pulse generator B : $t_p \geqslant 10$ ns and PRR = 1 MHz.
When testing f_{max}, vary PRR.
2. Voltage values are with respect to network ground terminal.
3. C_L includes probe and jig capacitance.

FIGURE 9 – SWITCHING TIMES

PARAMETER MEASUREMENT INFORMATION

recommended mode control setup times



NOTE: A Input is at $V_{in(0)}$.

FIGURE 10–MODE CONTROL SETUP TIMES

SN54121/SN74121
The One-Shot
Heard 'Round the World

Pulse Width: 40 Nanoseconds to 40 Seconds

Pulse Stability: ±0.2%

Triggering: Ramps Up to One Volt Per Second

See Page 2-38 for specifications and Page B-1 for abstract and ordering information of Application Report CA-128

CIRCUIT TYPES SN5495, SN7495
4-BIT RIGHT-SHIFT LEFT-SHIFT REGISTERS

A TTL MSI PARALLEL-IN PARALLEL-OUT REGISTER

for application as

- N-Bit Serial-To-Parallel Converter
- N-Bit Parallel-To-Serial Converter
- N-Bit Storage Register

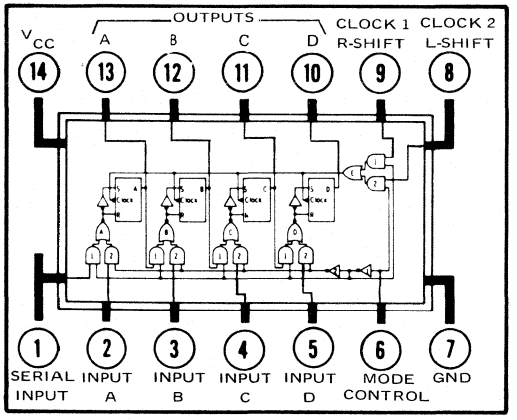
description

This monolithic shift register, utilizing transistor-transistor-logic (TTL) circuits in the familiar Series 54/74 configuration, is composed of four R-S master-slave flip-flops, four AND-OR-INVERT gates, one AND-OR-INVERT gates, one AND-OR gate, and six inverter-drivers. Internal interconnections of these functions provide a versatile register which will perform right-shift or left-shift operations dependent upon the logical input level to the mode control. A number of these registers may be connected in series to form an n-bit right-shifter or left-shift register. This register can also be used as a parallel-in, parallel-out storage register with gate (mode) control.

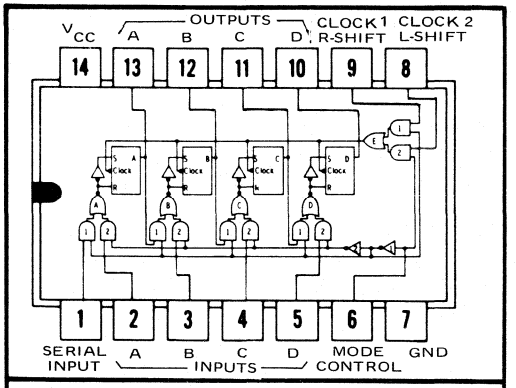
When a logical 0 level is applied to the mode control input, the number-1 AND gates are enabled and the number-2 AND gates are inhibited. In this mode the output of each flip-flop is coupled to the R-S inputs of the succeeding flip-flop and right-shift operation is performed by clocking at the clock 1 input. In this mode, serial data is entered at the serial input. Clock 2 and parallel inputs A through D are inhibited by the number-2 AND gates.

When a logical 1 level is applied to the mode control input, the number-1 AND gates are inhibited (decoupling the outputs from the succeeding R-S inputs to prevent right-shift) and the number-2 AND gates are enabled to allow entry of data through parallel inputs A through D and clock 2. This mode permits parallel loading of the register, or with external interconnection, shift-left operation. In this mode, shift-left can be accomplished by connecting the output of each flip-flop to the parallel input of the previous flip-flop (D_{out} to input C, and etc.), and serial data is entered at input D.

S
FLAT PACKAGE (TOP VIEW)



J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



positive logic

Mode control = 0 for right shift
Mode control = 1 for left shift or parallel load

Clocking for the shift register is accomplished through the AND-OR gate E which permits separate clock sources to be used for the shift-right and shift-left modes. If both modes can be clocked from the same source, the clock input may be applied commonly to clock 1 and clock 2. Information must be present at the R-S inputs of the master-slave flip-flops prior to clocking. Transfer of information to the output pins occurs when the clock input goes from a logical 1 to a logical 0.

This shift register is completely compatible with Series 54/74 TTL and DTL logic families. Average power dissipation is typically 250 milliwatts.

absolute maximum ratings (over operating temperature range unless otherwise noted)

Supply Voltage V_{CC} (See Note 1) . . . . . 7 V
Input Voltage, V_{in} (See Notes 1 and 2) . . . . . 5.5 V
Operating Case Temperature Range: SN5495S Circuits . . . . . −55°C to 125°C
Operating Free-Air Temperature Range: SN5495J, SN5495N Circuits . . . . . −55°C to 125°C
SN7495 Circuits . . . . . 0°C to 70°C
Storage Temperature Range . . . . . −65°C to 150°C

recommended operating conditions (over operating temperature range)

	MIN	NOM	MAX	UNIT
Supply Voltage V_{CC} (See Note 1): SN5495 Circuits	4.5	5	5.5	V
SN7495 Circuits	4.75	5	5.25	V
Normalized Fan-Out From Each Output			10	
Width of Clock Pulse $t_{p(clock)}$ (See Figure 9): SN5495 Circuits	20	10		ns
SN7495 Circuits	15	10		ns
Setup Time Required at Serial, A, B, C, or D Inputs t_{setup} (See Figure 9)	20	10		ns
Hold Time Required at Serial, A, B, C, or D Inputs t_{hold} (See Figure 9)	0	−10		ns
Logical 0 Level Setup Time Required at Mode Control (t1 in Figure 10) (With Respect to Clock 1 input)	20			ns
Logical 1 Level Setup Time Required at Mode Control (t2 in Figure 10) (With Respect to Clock 2 input)	20			ns
Logical 0 Level Setup Time Required at Mode Control (t3 in Figure 10) (With Respect to Clock 2 input)	10			ns
Logical 1 Level Setup Time Required at Mode Control (t4 in Figure 10) (With Respect to Clock 1 input)	10			ns

NOTES: 1. Voltage values are with respect to network ground terminal.
2. Input voltages must be zero or positive with respect to network ground terminal.

electrical characteristics (over operating temperature range unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
$V_{in(1)}$	Input voltage required to ensure logical 1 at any input terminal	1 and 3	V_{CC} = MIN		2			V
$V_{in(0)}$	Input voltage required to ensure logical 0 at any input terminal	2 and 4	V_{CC} = MIN				0.8	V
$V_{out(1)}$	Logical 1 output voltage	1 and 3	V_{CC} = MIN,	I_{load} = −400 μA	2.4			V
$V_{out(0)}$	Logical 0 output voltage	2 and 4	V_{CC} = MIN,	I_{sink} = 16 mA			0.4	V
$I_{in(0)}$	Logical 0 level input current at any input except mode control	5	V_{CC} = MAX,	V_{in} = 0.4 V			−1.6	mA
$I_{in(0)}$	Logical 0 level input current at mode control	5	V_{CC} = MAX,	V_{in} = 0.4 V			−3.2	mA
$I_{in(1)}$	Logical 1 level input current at any input except mode control	6	V_{CC} = MAX,	V_{in} = 2.4 V			40	μA
			V_{CC} = MAX,	V_{in} = 5.5 V			1	mA
$I_{in(1)}$	Logical 1 level input current at mode control	6	V_{CC} = MAX,	V_{in} = 2.4 V			80	μA
			V_{CC} = MAX,	V_{in} = 5.5 V			1	mA
I_{OS}	Short-circuit output current§	7	V_{CC} = MAX		−18		−57	mA
I_{CC}	Supply current	8	V_{CC} = MAX	SN5495		50	72	mA
				SN7495		50	82	mA

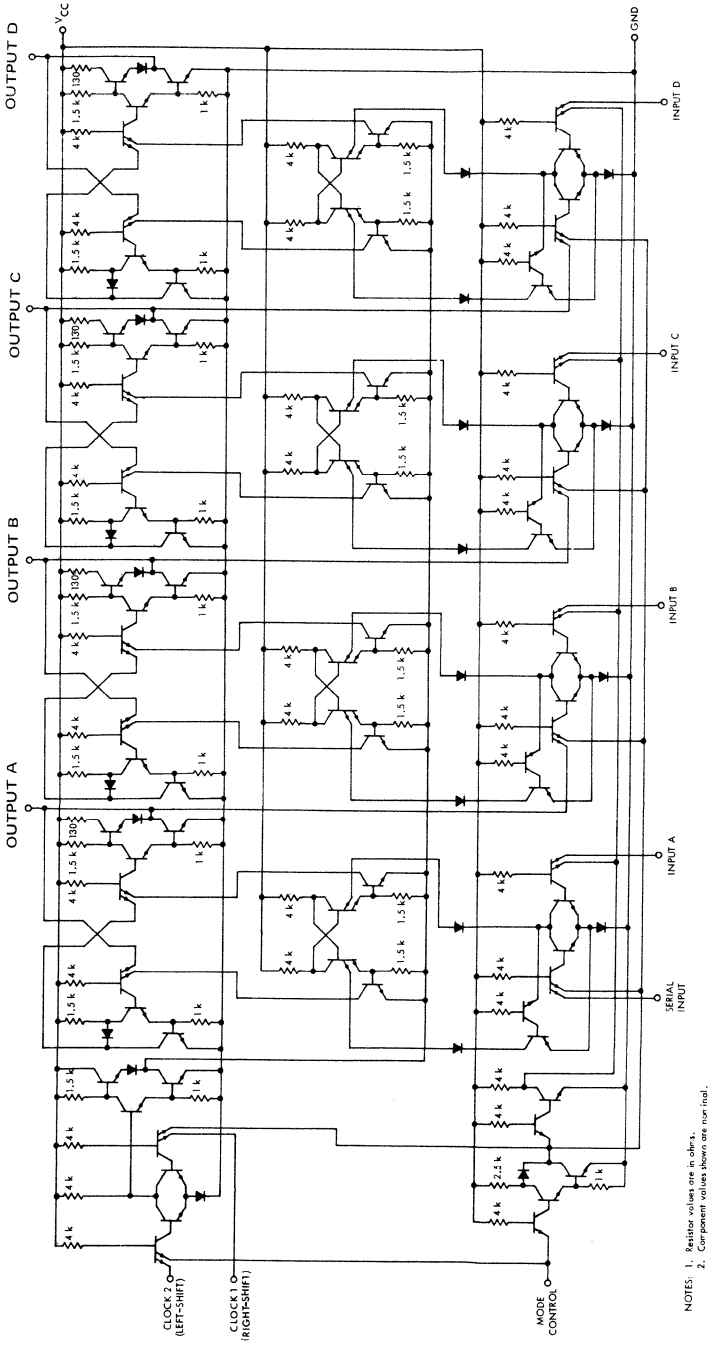
†For conditions shown as MIN or MAX use the appropriate value specified under recommended operating conditions for the particular circuit type.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ Not more than one output should be shorted at a time.

switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10

PARAMETER		TEST FIGURE	TEST CONDITIONS†		MIN	TYP	MAX	UNIT
f_{max}	Maximum shift frequency	9	C_L = 15 pF,	R_L = 400 Ω	20	31		MHz
t_{pd1}	Propagation delay time to logical 1 level from clock 1 or clock 2 to outputs	9	C_L = 15 pF,	R_L = 400 Ω		26	35	ns
t_{pd0}	Propagation delay time to logical 0 level from clock 1 or clock 2 to outputs	9	C_L = 15 pF,	R_L = 400 Ω		24	35	ns

— SEE ORDERING INSTRUCTIONS PAGE 1-1 —

schematic


OUTPUT D
OUTPUT C
OUTPUT B
OUTPUT A
V_{CC}
GND
INPUT D
INPUT C
INPUT B
INPUT A
SERIAL INPUT
CLOCK 2 (LEFT-SHIFT)
CLOCK 1 (RIGHT-SHIFT)
MODE CONTROL
NOTES: 1. Resistor values are in ohms.
2. Component values shown are nominal.

PARAMETER MEASUREMENT INFORMATION

d-c test circuits†

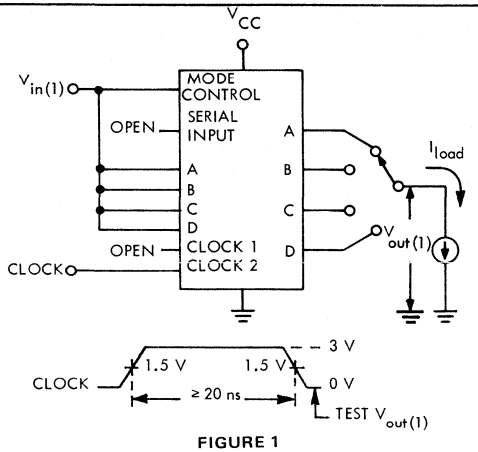


FIGURE 1

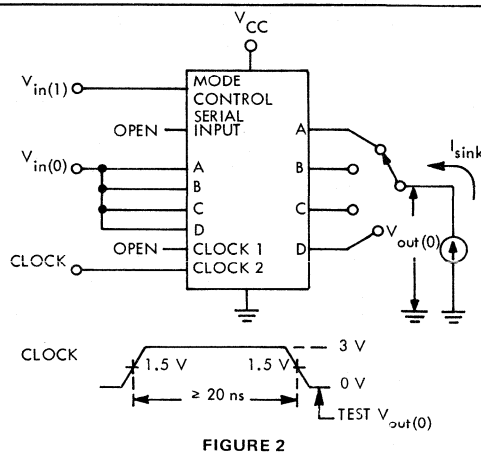


FIGURE 2

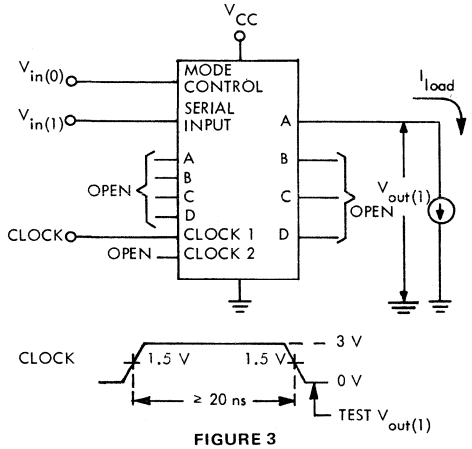


FIGURE 3

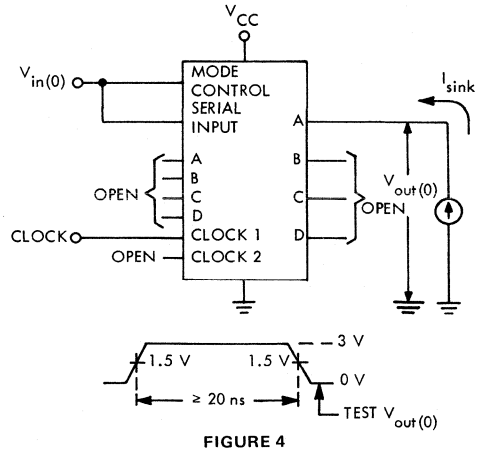
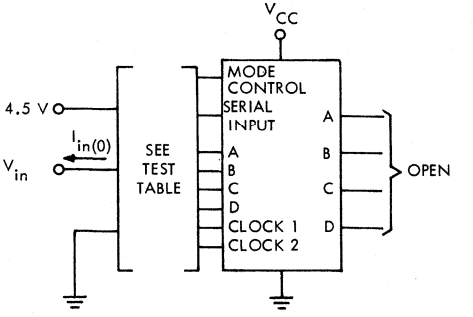


FIGURE 4



1. Each input is tested separately.

TEST TABLE

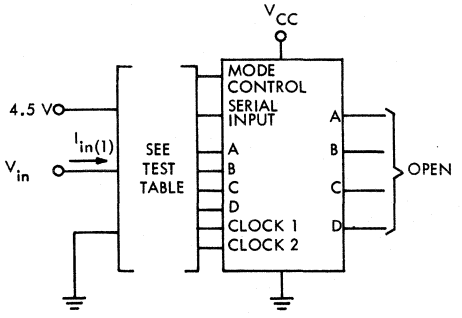
TEST	APPLY 4.5 V	APPLY GND
MODE CONTROL	CLOCK 2	NONE
SERIAL INPUT	NONE	MODE CONTROL
INPUT A	MODE CONTROL	NONE
INPUT B	MODE CONTROL	NONE
INPUT C	MODE CONTROL	NONE
INPUT D	MODE CONTROL	NONE
CLOCK 1	NONE	MODE CONTROL
CLOCK 2	MODE CONTROL	NONE

FIGURE 5

†Arrows indicate actual direction of current flow.

PARAMETER MEASUREMENT INFORMATION

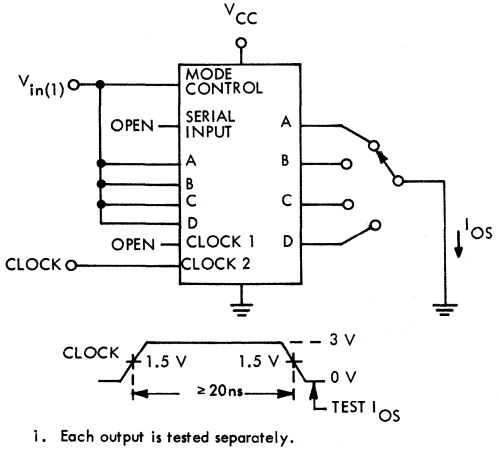
d-c test circuits† (continued)



TEST TABLE

TEST	APPLY 4.5 V	APPLY GND
MODE CONTROL	NONE	CLOCK 2
SERIAL INPUT	MODE CONTROL	NONE
INPUT A	NONE	MODE CONTROL
INPUT B	NONE	MODE CONTROL
INPUT C	NONE	MODE CONTROL
INPUT D	NONE	MODE CONTROL
CLOCK 1	MODE CONTROL	NONE
CLOCK 2	NONE	MODE CONTROL

FIGURE 6



1. Each output is tested separately.

FIGURE 7

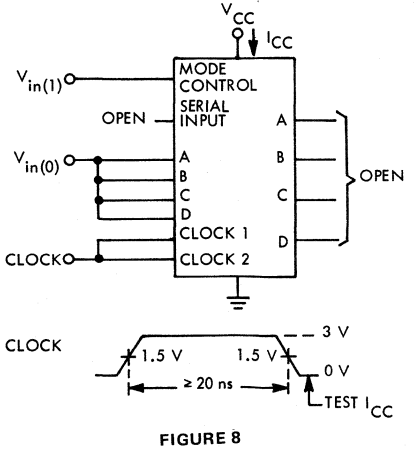
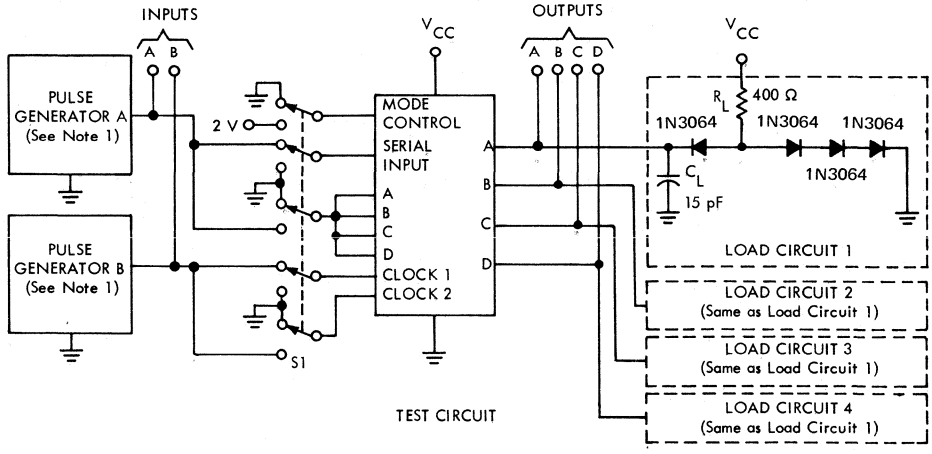


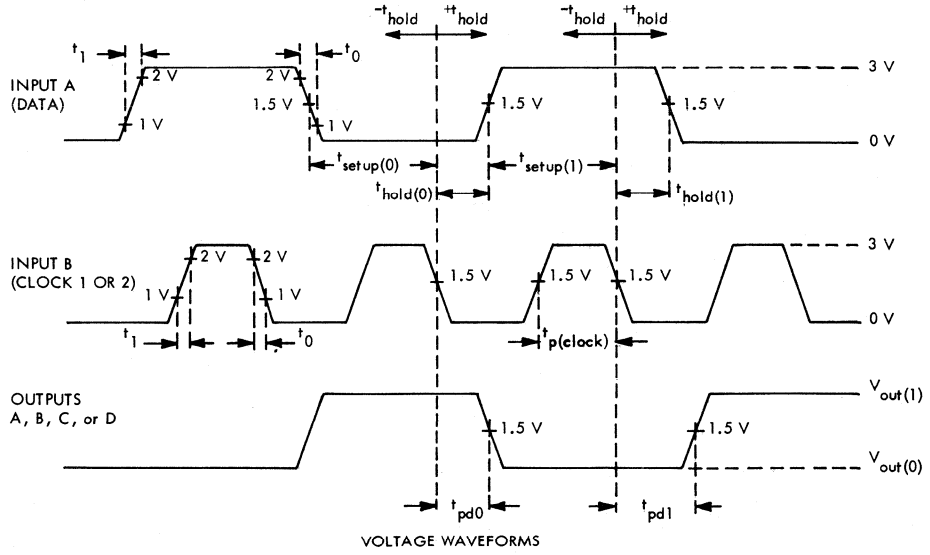
FIGURE 8

†Arrows indicate actual direction of current flow.

PARAMETER MEASUREMENT INFORMATION

switching charateristics





VOLTAGE WAVEFORMS

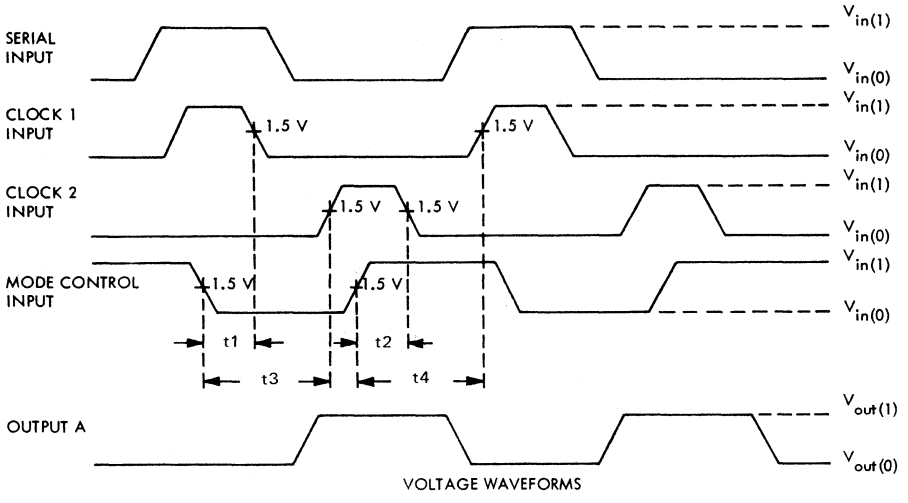
NOTES: 1. The pulse generators have the following characteristics: V_{gen} = 3 V, $t_1 = t_0 \leq$ 10 ns, and $Z_{out} \approx 50\ \Omega$. For pulse generator A : $t_p \geq$ 20 ns and PRR = 500 kHz. For pulse generator B : $t_p \geq$ 15 ns and PRR = 1 MHz. When testing f_{max} vary PRR.

2. Voltage values are with respect to network ground terminal.
3. C_L includes probe and jig capacitance.

FIGURE 9–SWITCHING TIMES

PARAMETER MEASUREMENT INFORMATION

recommended mode control setup times



NOTE: Input A is at $V_{in(0)}$.

FIGURE 10–MODE CONTROL SETUP TIMES

Write for

Valuable "How-to" Information for design of TTL integrated circuits:

See Pages B-1 and B-2 for abstracts of TTL Application Reports – free for the asking.

CIRCUIT TYPES SN5496, SN7496
5-BIT SHIFT REGISTERS

TTL MSI MULTIFUNCTION SHIFT REGISTERS

for application as

- N-Bit Serial-To-Parallel Converter
- N-Bit Parallel-To-Serial Converter
- N-Bit Storage Register

description

This shift register consists of five R-S master-slave flip-flops connected to perform parallel-to-serial or serial-to-parallel conversion of binary data. Since both inputs and outputs to all flip-flops are accessible, parallel-in/parallel-out or serial-in/serial-out operation may be performed.

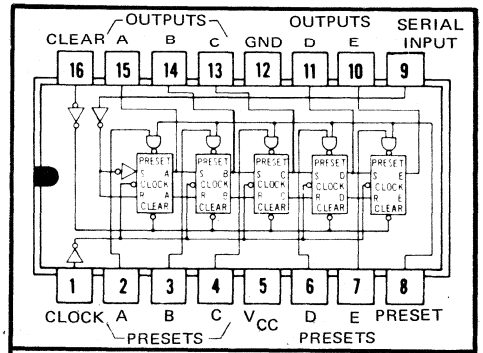
All flip-flops are simultaneously set to the logical 0 state by applying a logical 0 voltage to the clear input. This condition may be applied independent of the state of the clock input.

The flip-flops may be independently set to the logical 1 state by applying a logical 1 to both the preset input of the specific flip-flop and the common preset input. The common preset input is provided to allow flexibility of either setting each flip-flop independently or setting two or more flip-flops simultaneously. Preset is also independent of the state of the clock input or clear input.

Transfer of information to the output pins occurs when the clock input goes from a logical 0 to a logical 1. Since the flip-flops are R-S master-slave circuits, the proper information must appear at the R-S inputs of each flip-flop prior to the rising edge of the clock input voltage waveform. The serial input provides this information to the first flip-flop, while the outputs of the subsequent flip-flops provide information for the remaining R-S inputs. The clear input must be at a logical 1 and the preset input must be at a logical 0 when clocking occurs.

This shift register is completely compatible with Series 54/74 TTL and DTL logic families. Typically, average power dissipation is 240 milliwatts, and propagation delay time is 25 nanoseconds.

J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



positive logic: Low input of clear sets all outputs to logical 0.

absolute maximum ratings over operating temperature range (unless otherwise noted)

Supply Voltage V_{CC} (See Note 1)		7 V
Input Voltage, V_{in} (See Notes 1 and 2)		5.5 V
Operating Free-Air Temperature Range:	SN5496 Circuits	−55°C to 125°C
	SN7496 Circuits	0°C to 70°C
Storage Temperature Range		−65°C to 150°C

NOTES: 1. These voltage values are with respect to network ground terminal.
2. Input signals must be zero or positive with respect to network ground terminal.

CIRCUIT TYPES SN5496, SN7496
5-BIT SHIFT REGISTERS

recommended operating conditions (over operating temperature range)

	MIN	TYP	MAX	UNIT
Supply Voltage V_{CC} (See Note 1): SN5496 Circuits	4.5	5	5.5	V
SN7496 Circuits	4.75	5	5.25	V
Normalized Fan-Out from Output			10	
Width of Clock Pulse, $t_{p(clock)}$	35			ns
Width of Clear Pulse, $t_{p(clear)}$	30			ns
Width of Preset Pulse, $t_{p(preset)}$	30			ns
Serial Input Setup Time, t_{setup}	30			ns
Serial Input Hold Time, t_{hold}	0			ns

NOTE 1: This voltage value is with respect to network ground terminal.

electrical characteristics (over operating temperature range unless otherwise noted)

PARAMETER		TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
$V_{in(1)}$	Input voltage required to ensure logical 1 at any input terminal	V_{CC} = MIN		2			V
$V_{in(0)}$	Input voltage required to ensure logical 0 at any input terminal	V_{CC} = MIN				0.8	V
$V_{out(1)}$	Logical 1 output voltage	V_{CC} = MIN, I_{load} = −400 μA		2.4	3.5		V
$V_{out(0)}$	Logical 0 output voltage	V_{CC} = MIN, I_{sink} = 16 mA			0.22	0.4	V
$I_{in(1)}$	Logical 1 level input current at any input except preset (pin 8)	V_{CC} = MAX, V_{in} = 2.4 V				40	μA
		V_{CC} = MAX, V_{in} = 5.5 V				1	mA
$I_{in(1)}$	Logical 1 level input current at preset (pin 8)	V_{CC} = MAX, V_{in} = 2.4 V				200	μA
		V_{CC} = MAX, V_{in} = 5.5 V				1	mA
$I_{in(0)}$	Logical 0 level input current at any input except preset (pin 8)	V_{CC} = MAX, V_{in} = 0.4 V				−1.6	mA
$I_{in(0)}$	Logical 0 level input current at preset (pin 8)	V_{CC} = MAX, V_{in} = 0.4 V				−8	mA
I_{OS}	Short-circuit output current§	V_{CC} = MAX, V_{out} = 0	SN5496	−20		−57	mA
			SN7496	−18		−57	mA
I_{CC}	Supply current	V_{CC} = MAX	SN5496		48	68	mA
			SN7496		48	79	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the particular circuit type.

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

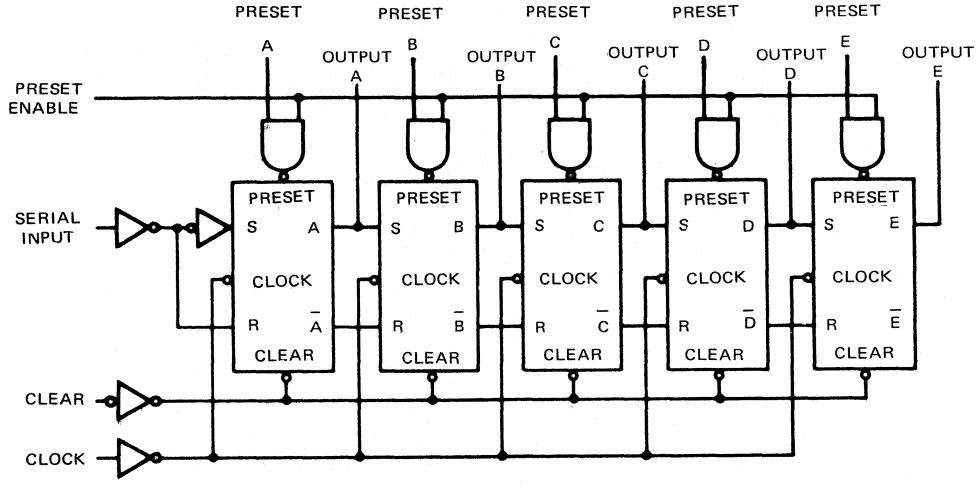
§Not more than one output should be shorted at a time

switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10

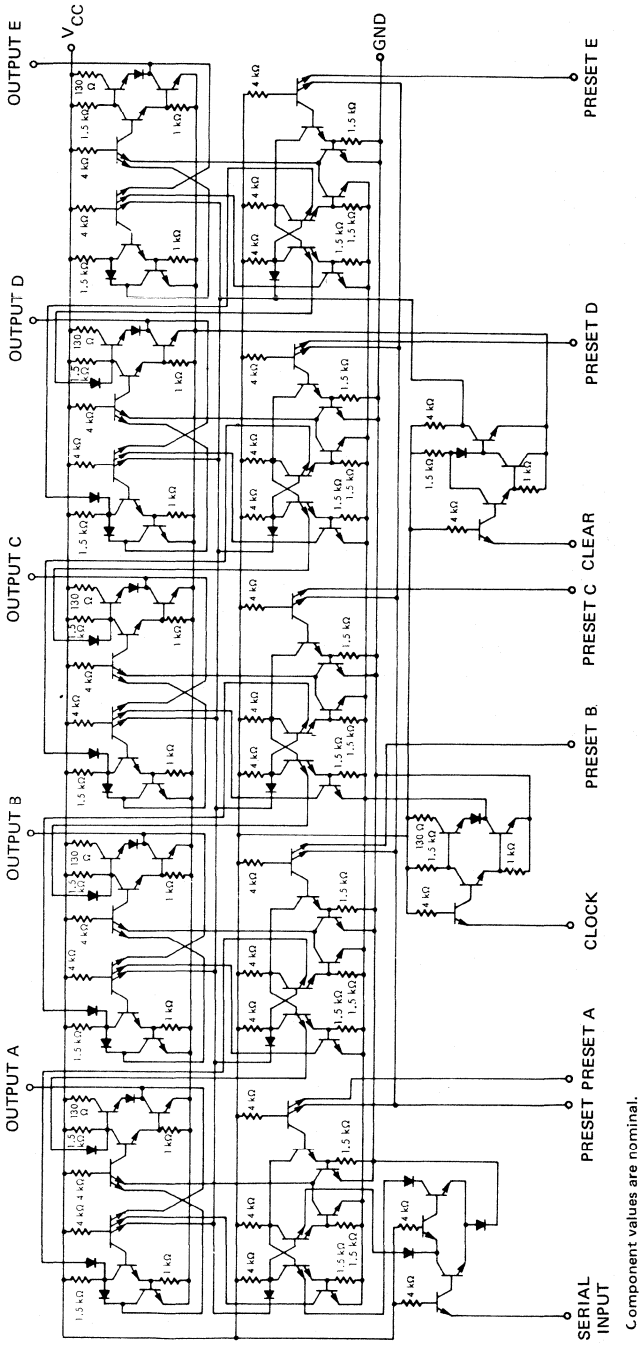
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max}	Maximum clock frequency	C_L = 15 pF, R_L = 400 Ω	10			MHz
t_{pd1}	Propagation delay time to logical 1 level from clock to output	C_L = 15 pF, R_L = 400 Ω		25	40	ns
t_{pd0}	Propagation delay time to logical 0 level from clock to output	C_L = 15 pF, R_L = 400 Ω		25	40	ns
t_{pd1}	Propagation delay time to logical 1 level from preset to output	C_L = 15 pF, R_L = 400 Ω			35	ns
t_{pd0}	Propagation delay time to logical 0 level from preset to output	C_L = 15 pF, R_L = 400 Ω		28	40	ns
t_{pd0}	propagation delay time to logical 0 level from clear to output	C_L = 15 pF, R_L = 400 Ω			55	ns

—SEE ORDERING INSTRUCTIONS PAGE 1-1—

functional block diagram



schematic



Component values are nominal.

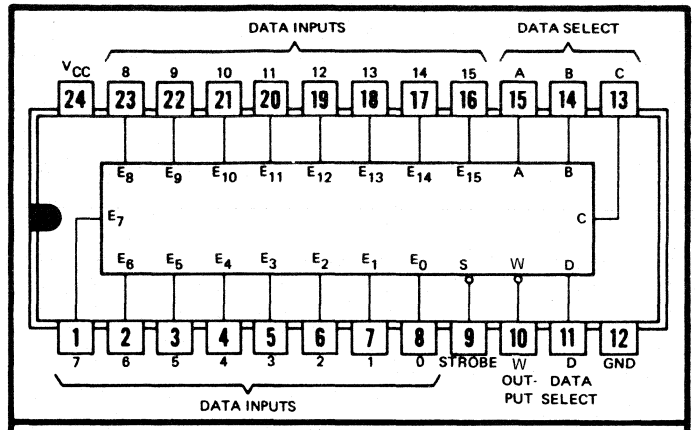
TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

CIRCUIT TYPES SN54150, SN54151, SN54152, SN74150, SN74151, SN74152
DATA SELECTORS/MULTIPLEXERS

features

- selects one-of-sixteen (or one-of-eight) data sources
- serves as a five-variable-function generator (SN54150, SN74150)
- performs parallel-to-serial conversion
- permits multiplexing from N-lines to l-line
- input-clamping diodes simplify system design
- typical propagation delay times:
  - through 4 select levels — 28 ns
  - through 3 select levels — 20 ns
  - data input to output — 10 ns
- high fan-out, low impedance, totem-pole outputs
- fully compatible with TTL, DTL and other MSI circuits

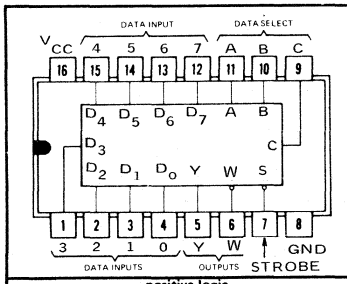
SN54150, SN74150
N DUAL-IN-LINE PACKAGE (TOP VIEW)



positive logic

$$W = S(\bar{A}\bar{B}\bar{C}\bar{D}E_0 + A\bar{B}\bar{C}\bar{D}E_1 + \bar{A}B\bar{C}\bar{D}E_2 + AB\bar{C}\bar{D}E_3 + \bar{A}\bar{B}C\bar{D}E_4 + A\bar{B}C\bar{D}E_5 + \bar{A}BC\bar{D}E_6 + ABC\bar{D}E_7$$
$$\bar{A}\bar{B}\bar{C}DE_8 + A\bar{B}\bar{C}DE_9 + \bar{A}B\bar{C}DE_{10} + AB\bar{C}DE_{11} + \bar{A}\bar{B}CDE_{12} + A\bar{B}CDE_{13} + \bar{A}BCDE_{14} + ABCDE_{15})$$

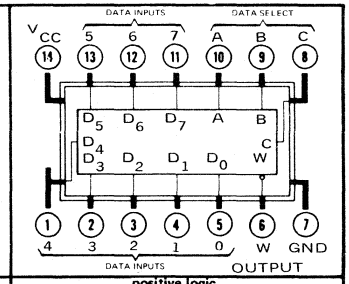
SN54151, SN74151
J OR N DUAL-IN-LINE PACKAGE (TOP VIEW)



positive logic

$$Y = \bar{S}(\bar{A}\bar{B}\bar{C}D_0 + A\bar{B}\bar{C}D_1 + \bar{A}B\bar{C}D_2 + AB\bar{C}D_3 + \bar{A}\bar{B}CD_4 + A\bar{B}CD_5 + \bar{A}BCD_6 + ABCD_7) \quad W = \bar{Y}$$

SN54152, SN74152
S FLAT PACKAGE
(TOP VIEW)



positive logic

$$W = (\bar{A}\bar{B}\bar{C}D_0 + A\bar{B}\bar{C}D_1 + AB\bar{C}D_3 + \bar{A}\bar{B}CD_4 + A\bar{B}CD_5 + \bar{A}BCD_6 + ABCD_7)$$

description

Each of these monolithic, data selectors/multiplexers contain inverter/drivers to supply fully complementary, on-chip, binary decoding data selection to the AND-OR-INVERT gate. The SN54151/74151 features complementary outputs whereas the SN54150/SN74150 and SN54152/SN74152 have inverted outputs only. The SN54150/SN74150 and SN54151/SN74151 circuits are provided with a strobe-input which, when taken to a logical 0, enables the function of these multiplexers.

These data selectors/multiplexers are fully compatible for use with other TTL or DTL circuits. Each input represents only one normalized Series 54/74 load, and full fan-out to 10 normalized Series 54/74 loads is available from each of the outputs in the logical 0 state. A fan-out to 20 normalized Series 54/74 loads is provided in the logical 1 state to facilitate connection of unused inputs to used inputs. Typical power dissipations are:

SN54150/SN74150 — 200 milliwatts
SN54151/SN74151 — 145 milliwatts
SN54152/SN74152 — 130 milliwatts

These data selectors feature Series 54H/74H circuitry for the OR function. This is done to minimize the capacitive effects of paralleling the phase-splitter transistors and thus reduce the propagation delay time. The SN54150, SN54151, and SN54152 are characterized for operation over the full military temperature range of −55°C to 125°C; and the SN74150, SN74151 and SN74152 are characterized for operation from 0°C to 70°C.

logic

TRUTH TABLE (SN54150/SN74150 ONLY)

INPUTS																		OUTPUT
D	C	B	A	STROBE	E_0	E_1	E_2	E_3	E_4	E_5	E_6	E_7	E_8	E_9	E_{10}	E_{11}	E_{12}	E_{13}	E_{14}	E_{15}	W
X	X	X	X	1	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	1
0	0	0	0	0	0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	1
0	0	0	0	0	1	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	0
0	0	0	1	0	X	0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	1
0	0	0	1	0	X	1	X	X	X	X	X	X	X	X	X	X	X	X	X	X	0
0	0	1	0	0	X	X	0	X	X	X	X	X	X	X	X	X	X	X	X	X	1
0	0	1	0	0	X	X	1	X	X	X	X	X	X	X	X	X	X	X	X	X	0
0	0	1	1	0	X	X	X	0	X	X	X	X	X	X	X	X	X	X	X	X	1
0	0	1	1	0	X	X	X	1	X	X	X	X	X	X	X	X	X	X	X	X	0
0	1	0	0	0	X	X	X	X	0	X	X	X	X	X	X	X	X	X	X	X	1
0	1	0	0	0	X	X	X	X	1	X	X	X	X	X	X	X	X	X	X	X	0
0	1	0	1	0	X	X	X	X	X	0	X	X	X	X	X	X	X	X	X	X	1
0	1	0	1	0	X	X	X	X	X	1	X	X	X	X	X	X	X	X	X	X	0
0	1	1	0	0	X	X	X	X	X	X	0	X	X	X	X	X	X	X	X	X	1
0	1	1	0	0	X	X	X	X	X	X	1	X	X	X	X	X	X	X	X	X	0
0	1	1	1	0	X	X	X	X	X	X	X	0	X	X	X	X	X	X	X	X	1
0	1	1	1	0	X	X	X	X	X	X	X	1	X	X	X	X	X	X	X	X	0
1	0	0	0	0	X	X	X	X	X	X	X	X	0	X	X	X	X	X	X	X	1
1	0	0	0	0	X	X	X	X	X	X	X	X	1	X	X	X	X	X	X	X	0
1	0	0	1	0	X	X	X	X	X	X	X	X	X	0	X	X	X	X	X	X	1
1	0	0	1	0	X	X	X	X	X	X	X	X	X	1	X	X	X	X	X	X	0
1	0	1	0	0	X	X	X	X	X	X	X	X	X	X	0	X	X	X	X	X	1
1	0	1	0	0	X	X	X	X	X	X	X	X	X	X	1	X	X	X	X	X	0
1	0	1	1	0	X	X	X	X	X	X	X	X	X	X	X	0	X	X	X	X	1
1	0	1	1	0	X	X	X	X	X	X	X	X	X	X	X	1	X	X	X	X	0
1	1	0	0	0	X	X	X	X	X	X	X	X	X	X	X	X	0	X	X	X	1
1	1	0	0	0	X	X	X	X	X	X	X	X	X	X	X	X	1	X	X	X	0
1	1	0	1	0	X	X	X	X	X	X	X	X	X	X	X	X	X	0	X	X	1
1	1	0	1	0	X	X	X	X	X	X	X	X	X	X	X	X	X	1	X	X	0
1	1	1	0	0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	0	X	1
1	1	1	0	0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	1	X	0
1	1	1	1	0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	0	1
1	1	1	1	0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	1	0

When used to indicate an input condition, X = LOGICAL 1 OR LOGICAL 0

logic (continued)

TRUTH TABLE (SN54151/SN74151 AND SN54152/SN74152 ONLY)

INPUTS												OUTPUTS	
C	B	A	STROBE(1)	D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7	Y(1)	W
X	X	X	1	X	X	X	X	X	X	X	X	0	1
0	0	0	0	0	X	X	X	X	X	X	X	0	1
0	0	0	0	1	X	X	X	X	X	X	X	1	0
0	0	1	0	X	0	X	X	X	X	X	X	0	1
0	0	1	0	X	1	X	X	X	X	X	X	1	0
0	1	0	0	X	X	0	X	X	X	X	X	0	1
0	1	0	0	X	X	1	X	X	X	X	X	1	0
0	1	1	0	X	X	X	0	X	X	X	X	0	1
0	1	1	0	X	X	X	1	X	X	X	X	1	0
1	0	0	0	X	X	X	X	0	X	X	X	0	1
1	0	0	0	X	X	X	X	1	X	X	X	1	0
1	0	1	0	X	X	X	X	X	0	X	X	0	1
1	0	1	0	X	X	X	X	X	1	X	X	1	0
1	1	0	0	X	X	X	X	X	X	0	X	0	1
1	1	0	0	X	X	X	X	X	X	1	X	1	0
1	1	1	0	X	X	X	X	X	X	X	0	0	1
1	1	1	0	X	X	X	X	X	X	X	1	1	0

NOTES: 1. SN54151/SN74151 only.
2. When used to indicate an input, X = irrelevant.

absolute maximum ratings (over operating temperature range unless otherwise noted)

Supply Voltage V_{CC} (See Note 1) . . . . . 7 V
Input Voltage, V_{in} (See Note 1) . . . . . 5.5 V
Operating Case Temperature Range: SN54152 . . . . . −55°C to 125°C
Operating Free-Air Temperature Range: SN54150, SN54151 Circuits . . . . . −55°C to 125°C
SN74150, SN74151, SN74152 Circuits . . . . . 0°C to 70°C
Storage Temperature Range . . . . . −65°C to 150°C

recommended operating conditions (over operating temperature range)

	MIN	NOM	MAX	UNIT
Supply Voltage V_{CC} (See Note 1): SN54150, SN54151, SN54152 Circuits	4.5	5	5.5	V
SN74150, SN74151, SN74152 Circuits	4.75	5	5.25	V
Normalized Fan-Out from Each Output (N): Logical 0			10	
Logical 1			20	

electrical characteristics (over operating temperature range unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
$V_{in(1)}$	Input voltage required to ensure logical 1 at any input terminal	1	V_{CC} = MIN		2			V
$V_{in(0)}$	Input voltage required to ensure logical 0 at any input terminal	2	V_{CC} = MIN				0.8	V
$V_{out(1)}$	Logical 1 output voltage	1 AND 2	V_{CC} = MIN, $V_{in(1)}$ = 2 V, $V_{in(0)}$ = 0.8 V, I_{load} = −800 μA		2.4			V
$V_{out(0)}$	Logical 0 output voltage	1 AND 2	V_{CC} = MIN, $V_{in(1)}$ = 2 V, $V_{in(0)}$ = 0.8 V, I_{sink} = 16 mA				0.4	V
$I_{in(1)}$	Logical 1 level input current (each input)	3	V_{CC} = MAX, V_{in} = 2.4 V				40	μA
			V_{CC} = MAX, V_{in} = 5.5 V				1	mA
$I_{in(0)}$	Logical 0 level input current (each input)	3	V_{CC} = MAX, V_{in} = 0.4 V				−1.6	mA
I_{OS}	Short circuit output current §	4	V_{CC} = MAX, V_{out} = 0	SN54150, SN54151, SN54152	−20		−55	mA
				SN74150, SN74151, SN74152	−18		−55	mA
I_{CC}	Supply current (SN54150/SN74150)	5	V_{CC} = MAX, V_{in} = 4.5 V			40	68	mA
I_{CC}	Supply current (SN54151/SN74151)	5	V_{CC} = MAX, V_{in} = 4.5 V			29	48	mA
I_{CC}	Supply current (SN54152/SN74152)	5	V_{CC} = MAX, V_{in} = 4.5 V			26	43	mA

switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{pd0}	A, B, or C (4 levels)	Y	6	C_L = 15 pF, R_L = 400 Ω		20	30	ns
t_{pd1}	A, B, or C (4 levels)	Y				35	52	ns
t_{pd0}	A, B, C, or D (3 levels)	W				19	30	ns
t_{pd1}	A, B, C, or D (3 levels)	W				20	30	ns
t_{pd0}	STROBE	Y				19	30	ns
t_{pd1}	STROBE	Y				35	52	ns
t_{pd0}	STROBE	W				21	30	ns
t_{pd1}	STROBE	W				12	20	ns
t_{pd0}	D_0 thru D_7	Y				8.5	14	ns
t_{pd1}	D_0 thru D_7	Y				13	20	ns
t_{pd0}	E_0 thru E_{15}	W				8.5	14	ns
t_{pd1}	E_0 thru E_{15}	W				11	20	ns

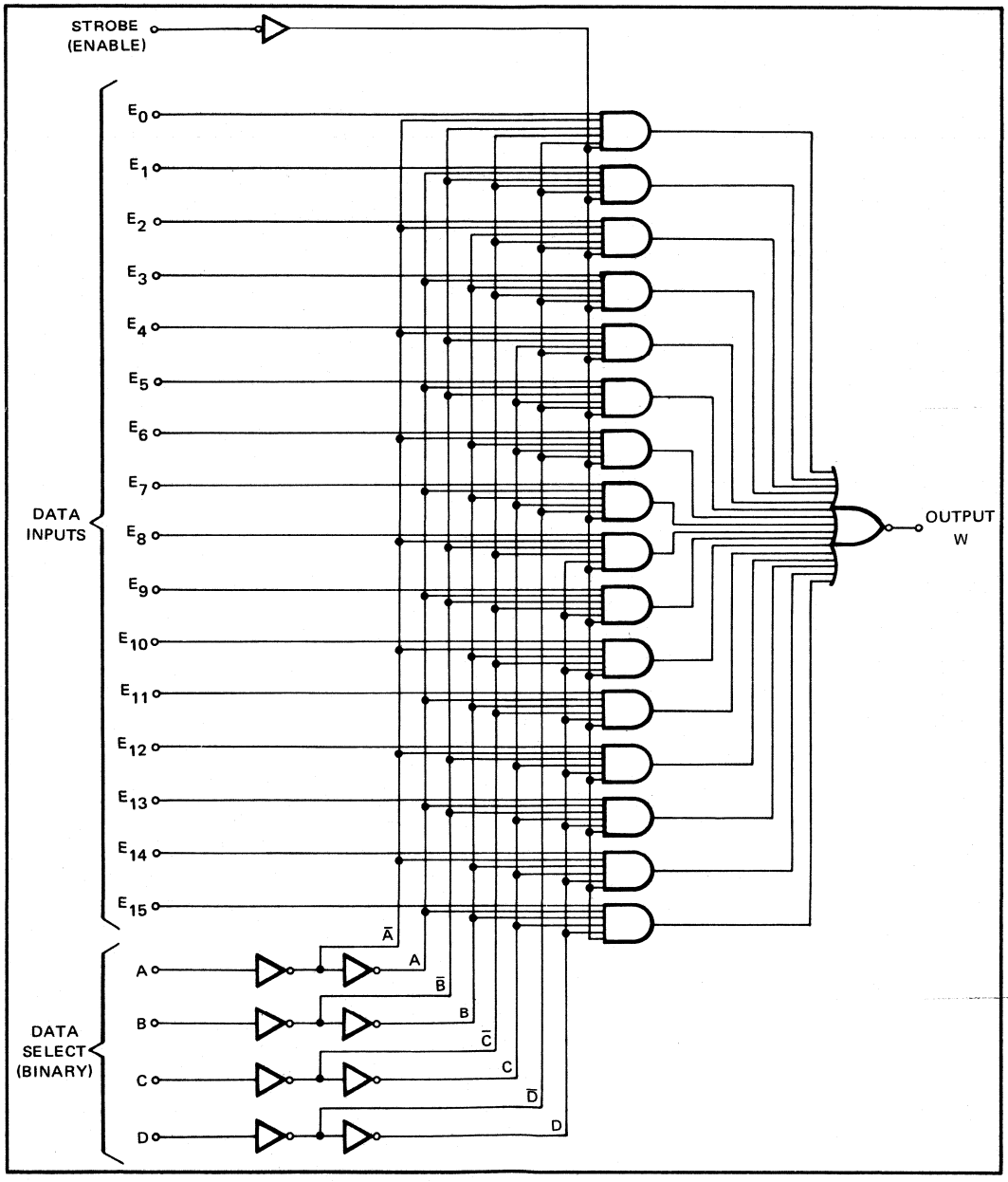
† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable circuit type.

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

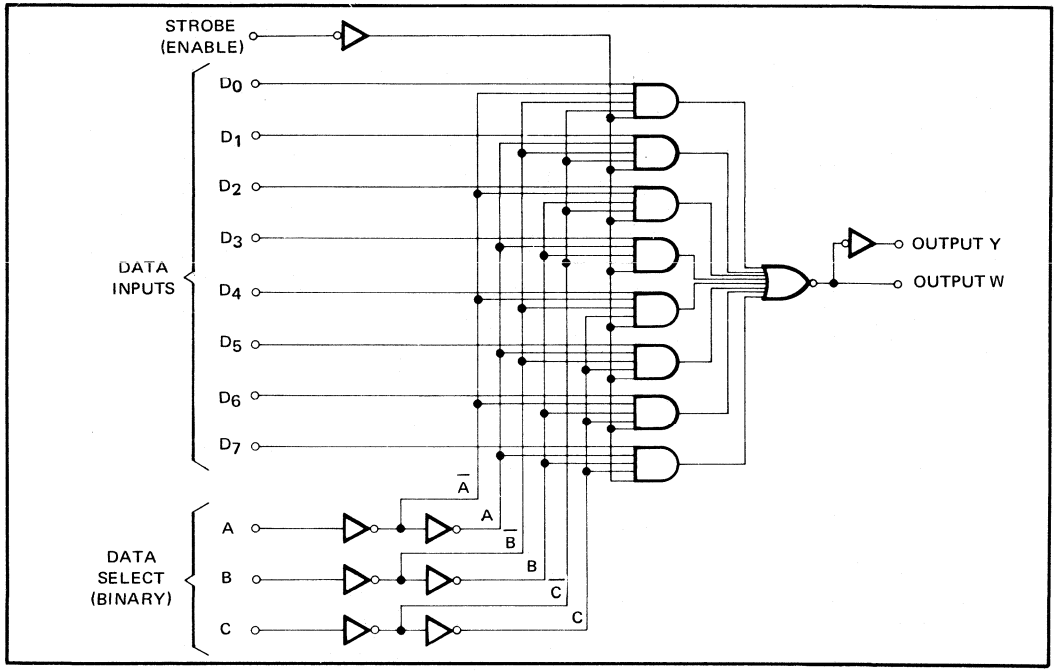
§ Not more than one output of the SN54151/SN74151 should be shorted at a time.

— SEE ORDERING INSTRUCTIONS PAGE 1-1 —

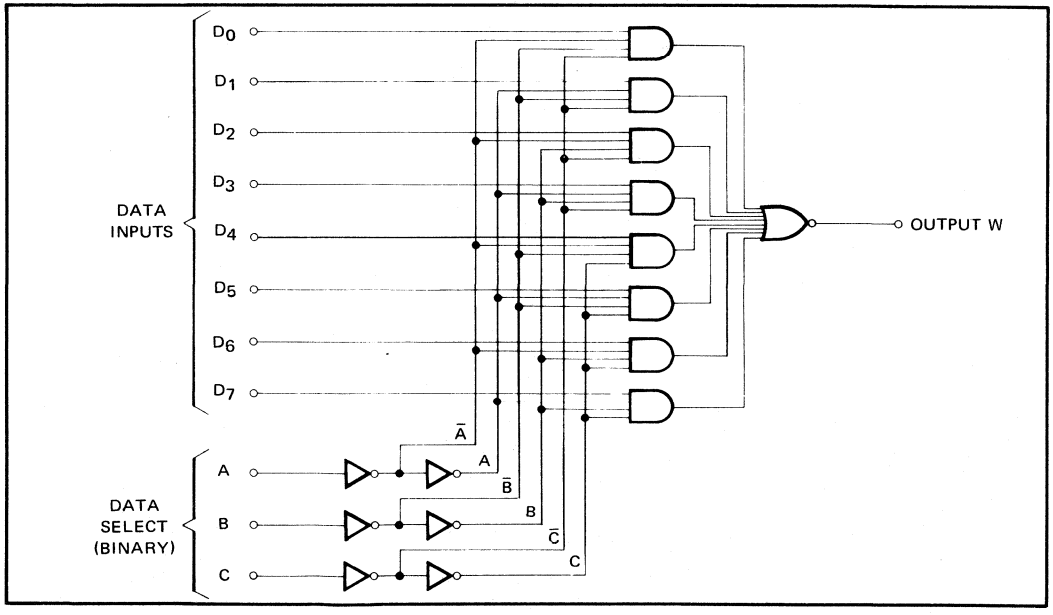
functional block diagram



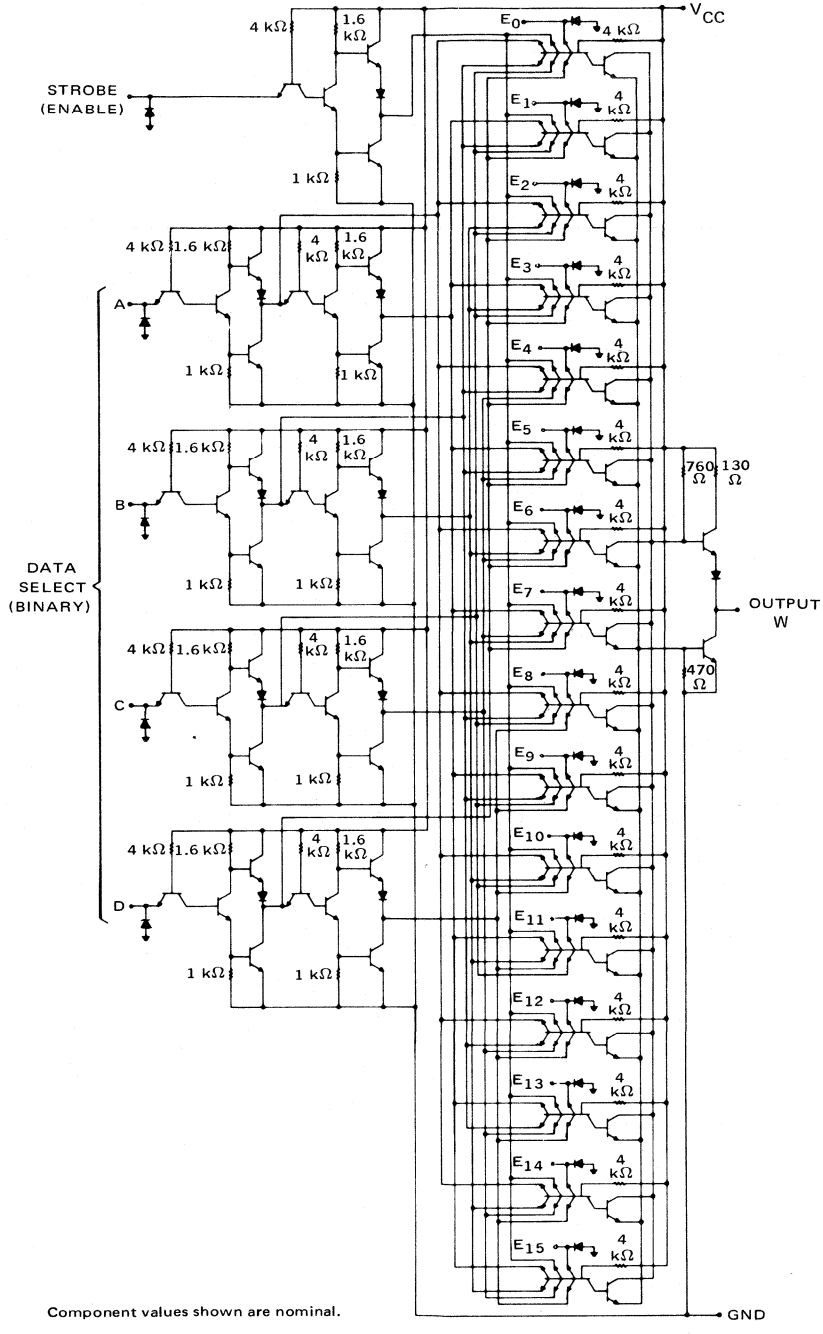
functional block diagram (SN54151, SN74151)



functional block diagram (SN54152, SN74152)

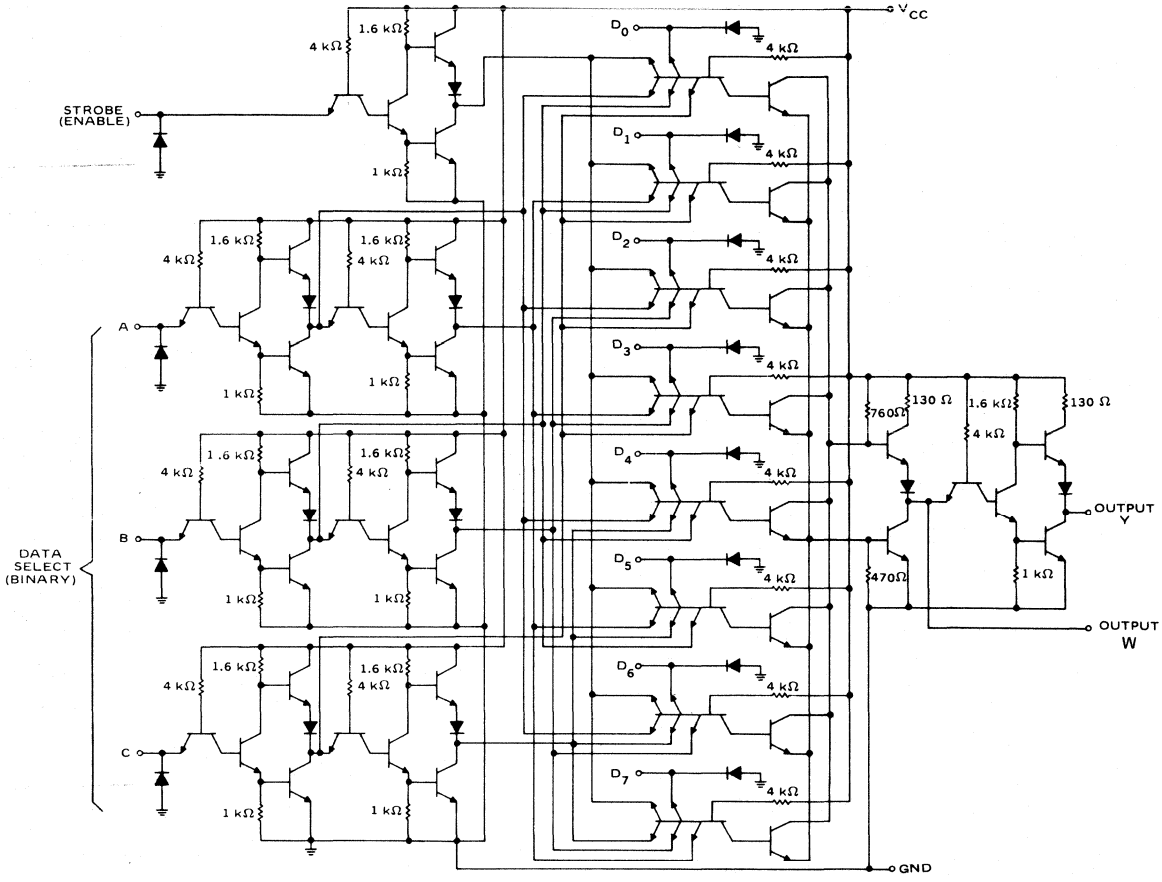


schematic



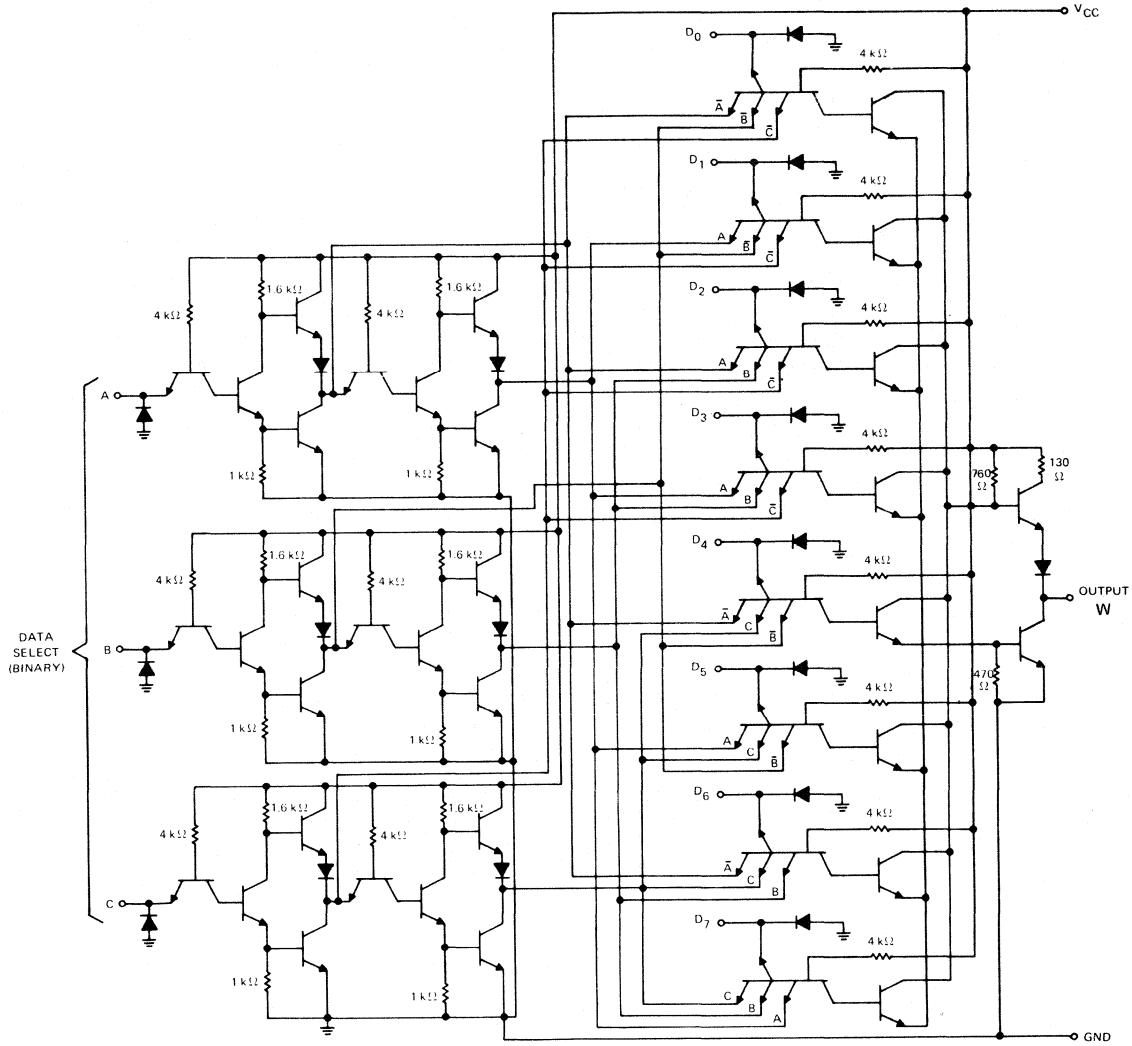
Component values shown are nominal.

schematic



Component values shown are nominal.

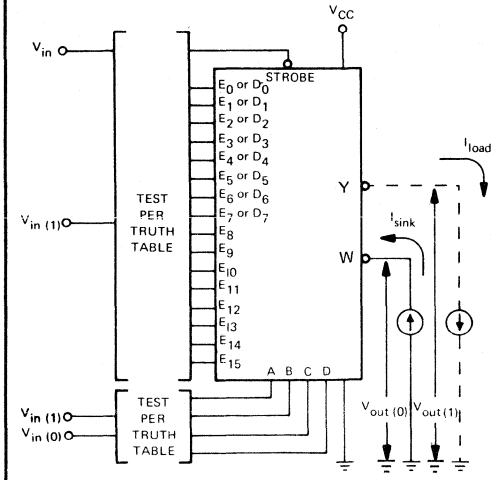
schematic



Component values shown are nominal.

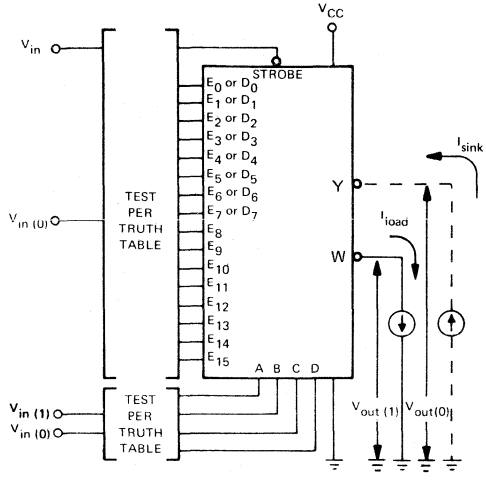
PARAMETER MEASUREMENT INFORMATION

d-c test circuits†



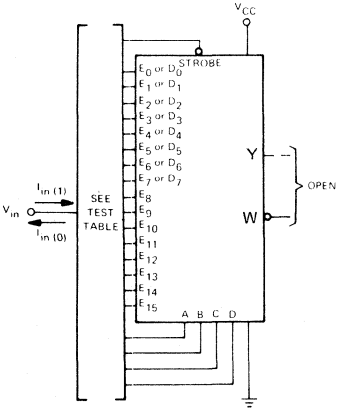
1. $V_{in(0)}$ is applied to STROBE; 8-4-2-1 code is applied to A, B, C, D; and input/output condition is tested for each step of the code.
2. $V_{in(1)}$ is applied to STROBE at which time $V_{out(0)}$ is measured at Y and $V_{out(1)}$ is measured at W.

FIGURE 1



1. $V_{in(0)}$ is applied to STROBE; 8-4-2-1 is applied to A, B, C, D; and input/output condition is tested for each step of the code.

FIGURE 2



TEST TABLE

INPUT CONDITIONS				TEST	
A	B	C	D	$I_{in(0)}$	$I_{in(1)}$
0	0	0	0	E_0 or D_0	E_{15} or D_7
1	0	0	0	E_1 or D_1	E_{14} or D_6
0	1	0	0	E_2 or D_2	E_{13} or D_5
1	1	0	0	E_3 or D_3	E_{12} or D_4
0	0	1	0	E_4 or D_4	E_{11} or D_3
1	0	1	0	E_5 or D_5	E_{10} or D_2
0	1	1	0	E_6 or D_6	E_9 or D_1
1	1	1	0	E_7 or D_7	E_8 or D_0
0	0	0	1	E_8	E_7
1	0	0	1	E_9	E_6
0	1	0	1	E_{10}	E_5
1	1	0	1	E_{11}	E_4

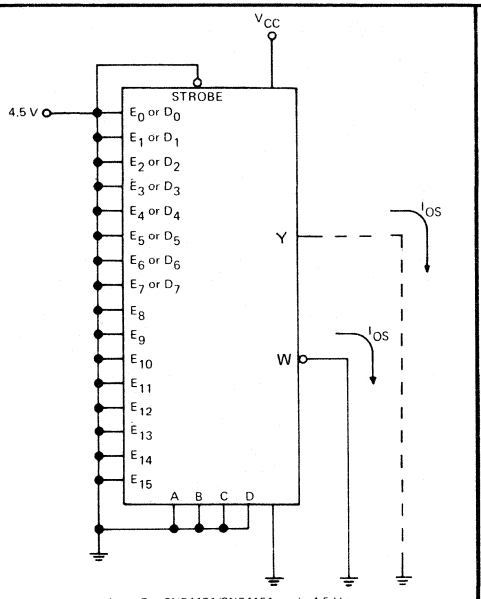
INPUT CONDITIONS				TEST	
A	B	C	D	$I_{in(0)}$	$I_{in(1)}$
0	0	1	1	E_{12}	E_3
1	0	1	1	E_{13}	E_2
0	1	1	1	E_{14}	E_1
1	1	1	1	E_{15}	E_0
0				A	
	0			B	
		0		C	
			0	D	
1					A
	1				B
		1			C
			1		D

FIGURE 3

† Arrows indicate actual direction of current flow. Tests as shown, are for the SN54150/SN74150. Identical tests as applicable are performed for the SN54151/SN74151 and SN54152/SN74152.

PARAMETER MEASUREMENT INFORMATION

d-c test circuits† (continued)



1. For SN54151/SN74151 apply 4.5 V to D_0 and measure I_{OS} at output Y

FIGURE 4

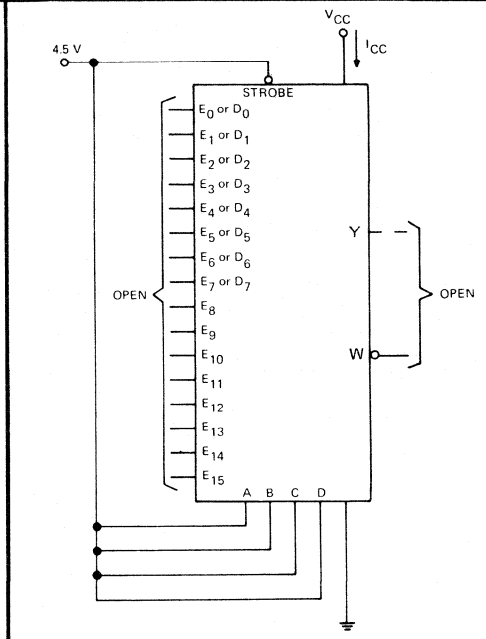


FIGURE 5

† Arrows indicate actual direction of current flow. Tests, as shown are for the SN54150/SN74150. Identical tests as applicable are performed for the SN54151/SN74151 and SN54152/SN74152.

switching characteristics†

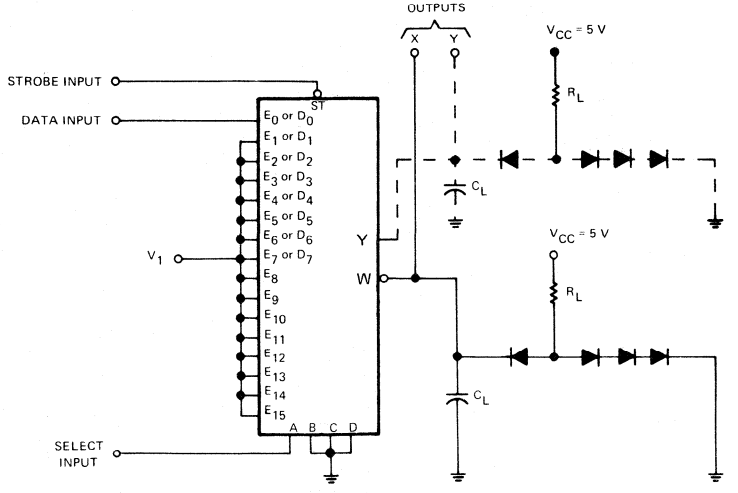
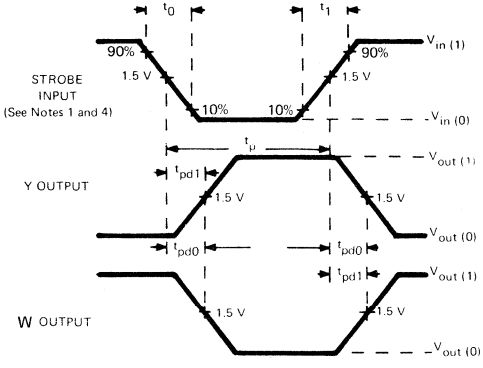


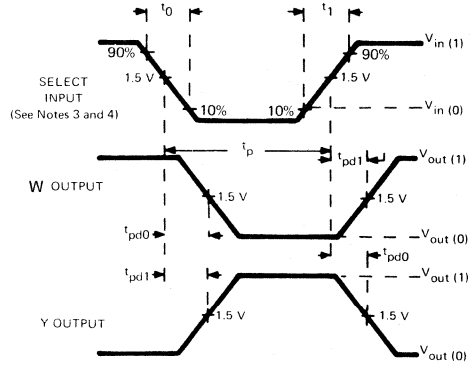
FIGURE 6–SWITCHING TIMES (SHEET 1 OF 2)

PARAMETER MEASUREMENT INFORMATION

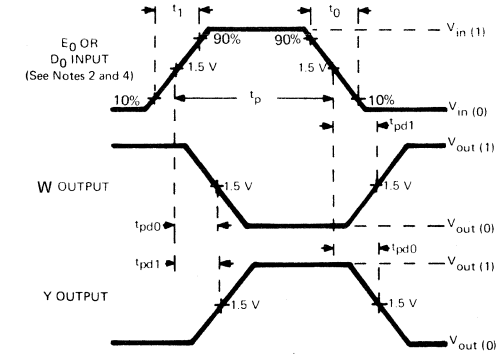
switching characteristics (continued)



STROBE-TO-OUTPUT VOLTAGE WAVEFORMS



SELECT INPUT-TO-OUTPUT VOLTAGE WAVEFORMS



DATA INPUT-TO-OUTPUT VOLTAGE WAVEFORMS

NOTES:
1. When measuring strobe-to-output times select input is at a logical 0, E_0 or D_0 is at a logical 1, V_1 = 4.5 V.
2. When measuring data input-to-output times strobe and select inputs are at a logical 0, and V_1 = 4.5 V.
3. When measuring select input-to-output times strobe input is at a logical 0, data input is at a logical 1, and V_1 = 0.
4. The input pulse has the following characteristics: $V_{in(1)}$ = 3 V, $V_{in(0)}$ = 0 V, $t_1 = t_0$ = 10 ns, PRR = 1 MHz, duty cycle = 50%, and generator $Z_{out} \approx 50\ \Omega$.
5. C_L includes probe and jig capacitance.
6. All diodes are 1N3064.

FIGURE 6–SWITCHING TIMES (SHEET 2 OF 2)

† Tests, as shown, are for the SN54150/SN74150, Identical tests as applicable are performed for the SN54151/SN74151 and SN54152/SN74152.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

CIRCUIT TYPES SN54180, SN74180
8-BIT ODD/EVEN PARITY GENERATORS/CHECKERS

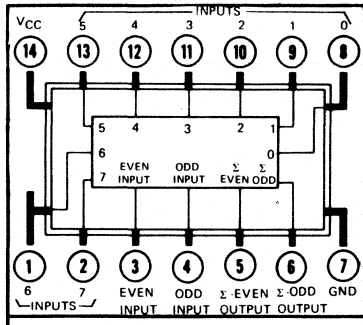
logic

TRUTH TABLE

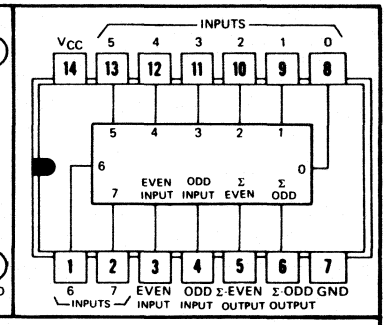
INPUTS			OUTPUTS	
Σ OF 1's AT 0 THRU 7	EVEN	ODD	Σ EVEN	Σ ODD
EVEN	1	0	1	0
ODD	1	0	0	1
EVEN	0	1	0	1
ODD	0	1	1	0
X	1	1	0	0
X	0	0	1	1

X= irrelevant

S FLAT PACKAGE
(TOP VIEW)



J OR N DUAL-IN-LINE PACKAGES
(TOP VIEW)



positive logic: see truth table

description

These universal, monolithic, 8-bit parity generators/checkers, utilizing familiar Series 54/74 TTL circuitry, feature odd/even outputs and control inputs to facilitate operation in either odd- or even-parity applications. The word-length capability is easily expanded by cascading. Typical applications are shown for these parity circuits being used to generate and check parity.

The SN54180/74180 are fully compatible with other TTL or DTL circuits. Input buffers are provided so that each data input represents only one normalized series 54/74 load. A full fan-out to 10 normalized series 54/74 loads is available from each of the outputs in the logical 0 state. A fan-out to 20 normalized loads is provided in the logical 1 state to facilitate the connection of unused inputs to used inputs. Typical power dissipation is 170 mW.

The SN54180 is characterized for operation over the full military temperature range of −55°C to 125°C; and the SN74180 is characterized for operation from 0°C to 70°C.

absolute maximum ratings (over operating temperature range unless otherwise noted)

Supply Voltage V_{CC} (See Note 1) . . . . . 7 V
Input Voltage, V_{in} (See Note 1) . . . . . 5.5 V
Operating Case Temperature Range, SN54180S . . . . . −55°C to 125°C
Operating Free-Air Temperature Range: SN54180J, SN54180N . . . . . −55°C to 125°C
SN74180 . . . . . 0°C to 70°C
Storage Temperature Range . . . . . −65°C to 150°C

NOTE 1: These voltage values are with respect to network ground terminal.

recommended operating conditions (over operating temperature range)

		MIN	NOM	MAX	UNIT
Supply Voltage V_{CC} (See Note 1):	SN54180	4.5	5	5.5	V
	SN74180	4.75	5	5.25	V
Normalized Fan-Out from Each Output (N):	Logical 0			10	V
	Logical 1			20	V

electrical characteristics (over operating temperature range unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
$V_{in(1)}$	Input voltage required to ensure logical 1 at any input terminal	1	V_{CC} = MIN		2			V
$V_{in(0)}$	Input voltage required to ensure logical 0 at any input terminal	1	V_{CC} = MIN				0.8	V
$V_{out(1)}$	Logical 1 output voltage	1	V_{CC} = MIN, $V_{in(1)}$ = 2 V, $V_{in(0)}$ = 0.8 V, I_{load} = −800 μA		2.4			V
$V_{out(0)}$	Logical 0 output voltage	1	V_{CC} = MIN, $V_{in(1)}$ = 2 V, $V_{in(0)}$ = 0.8 V, I_{sink} = 16 mA				0.4	V
$I_{in(1)}$	Logical 1 level input current at each data input	2	V_{CC} = MAX, V_{in} = 2.4 V				40	μA
			V_{CC} = MAX, V_{in} = 5.5 V				1	mA
$I_{in(0)}$	Logical 0 level input current at each data input	2	V_{CC} = MAX, V_{in} = 0.4 V				−1.6	mA
$I_{in(1)}$	Logical 1 level input current at even or odd input	2	V_{CC} = MAX, V_{in} = 2.4 V				80	μA
			V_{CC} = MAX, V_{in} = 5.5 V				1	mA
$I_{in(0)}$	Logical 0 level input current at even or odd input	2	V_{CC} = MAX, V_{in} = 0.4 V				−3.2	mA
I_{OS}	Short circuit output current§	3	V_{CC} = MAX	SN54180	−20		−55	mA
				SN74180	−18		−55	mA
I_{CC}	Supply current	3 and 4	V_{CC} = MAX	SN54180		34	49	mA
				SN74180		34	56	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the particular circuit type.

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

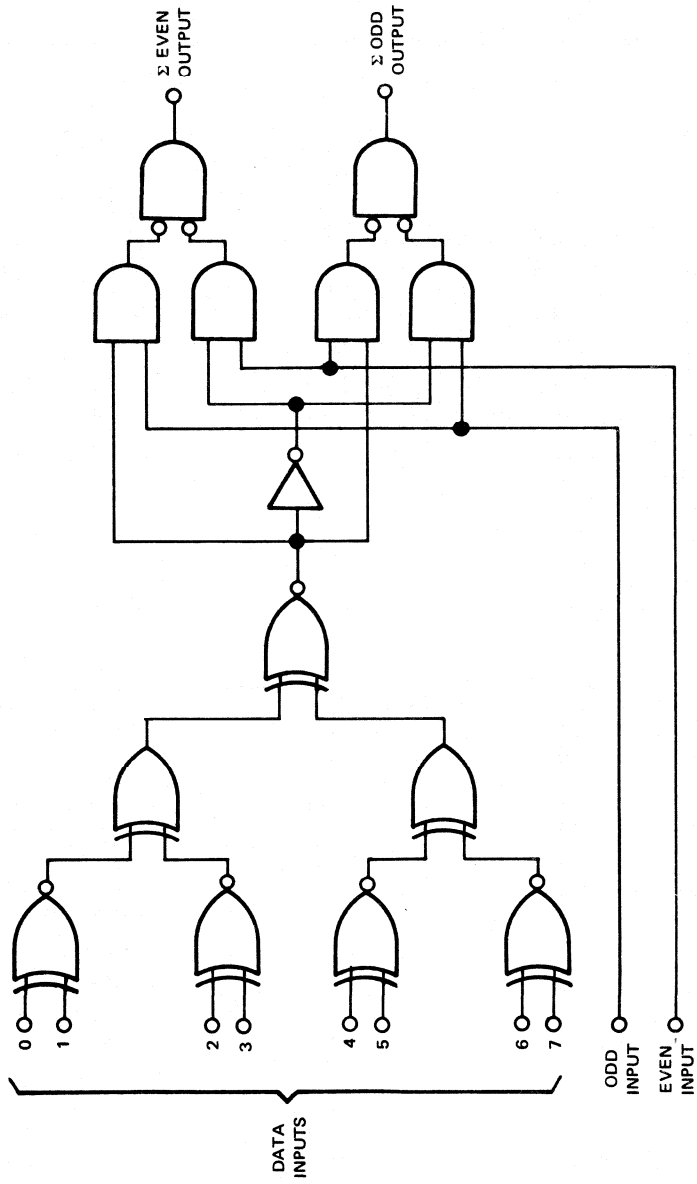
§ Not more than one output should be shorted at a time.

switching characteristics V_{CC} = 5 V, T_A = 25°C, N = 10

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{pd1}	Data	Σ Even	5	C_L = 15 pF, R_L = 400 Ω		40	60	ns
t_{pd0}	Data	Σ Even	5	C_L = 15 pF, R_L = 400 Ω		25	38	ns
t_{pd1}	Data	Σ Odd	5	C_L = 15 pF, R_L = 400 Ω		32	48	ns
t_{pd0}	Data	Σ Odd	5	C_L = 15 pF, R_L = 400 Ω		45	68	ns
t_{pd1}	Data	Σ Even	5	C_L = 15 pF, R_L = 400 Ω		32	48	ns
t_{pd0}	Data	Σ Even	5	C_L = 15 pF, R_L = 400 Ω		45	68	ns
t_{pd1}	Data	Σ Odd	5	C_L = 15 pF, R_L = 400 Ω		40	60	ns
t_{pd0}	Data	Σ Odd	5	C_L = 15 pF, R_L = 400 Ω		25	38	ns
t_{pd1}	Even or Odd	Σ Even or Σ Odd	5	C_L = 15 pF, R_L = 400 Ω		13	20	ns
t_{pd0}	Even or Odd	Σ Even or Σ Odd	5	C_L = 15 pF, R_L = 400 Ω		7	10	ns

–SEE ORDERING INSTRUCTIONS PAGE 1-1–

functional block diagram



PARAMETER MEASUREMENT INFORMATION

d-c test circuits†

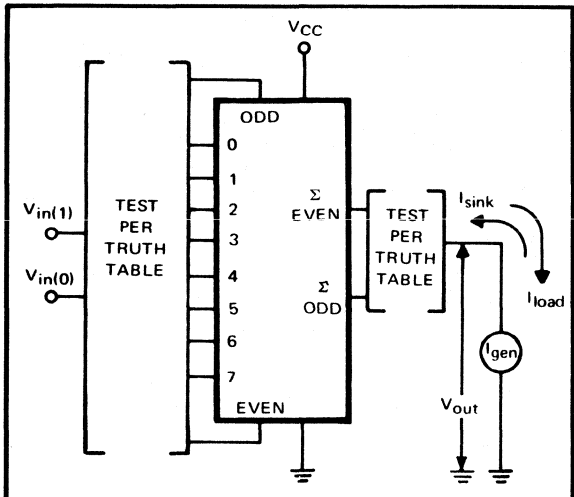
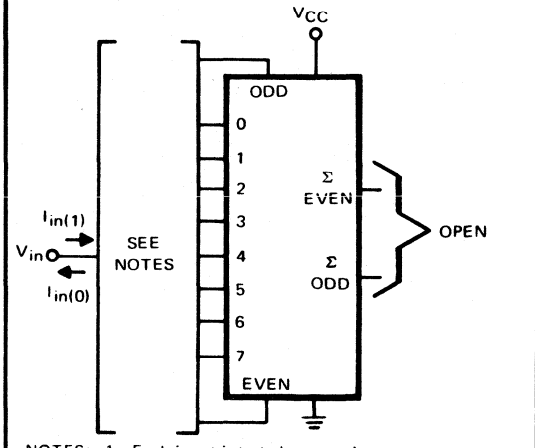
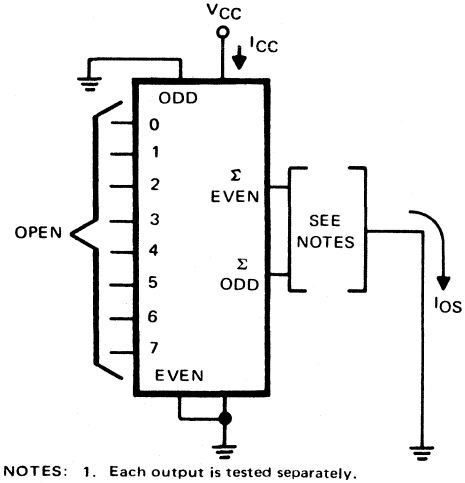


FIGURE 1



NOTES: 1. Each input is tested separately.
2. Odd and even inputs are each tested for $I_{in(1)}$ and $I_{in(0)}$ with both an even-code and an odd-code applied at the data inputs.

FIGURE 2



NOTES: 1. Each output is tested separately.
2. When testing I_{CC} both outputs are open.

FIGURE 3

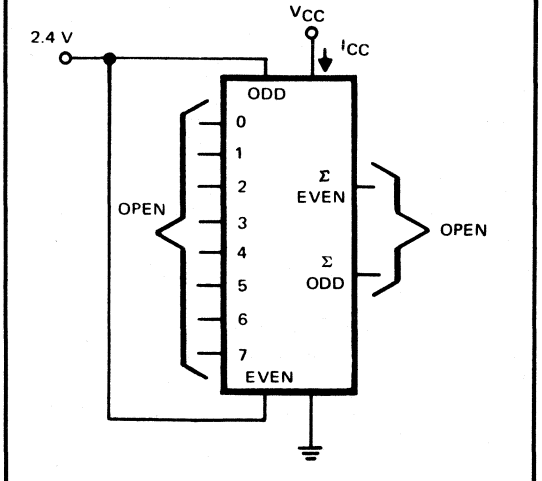
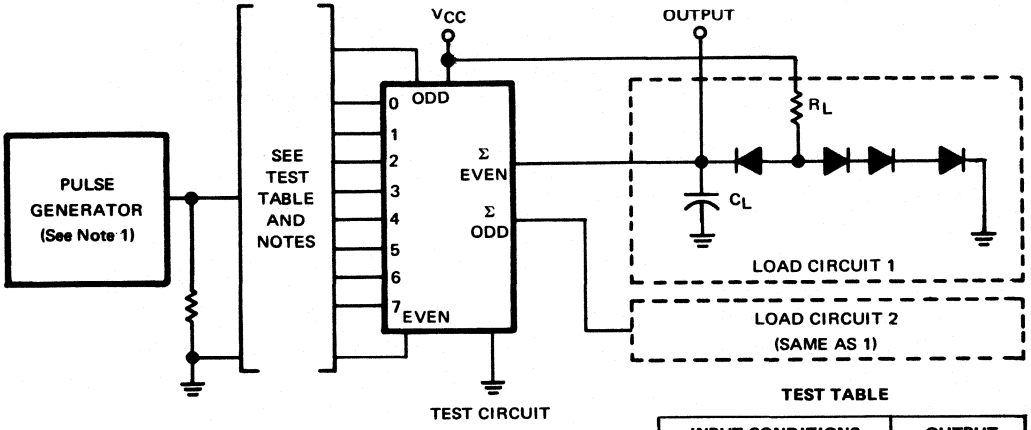


FIGURE 4

†Arrows indicate actual direction of current flow.

PARAMETER MEASUREMENT INFORMATION

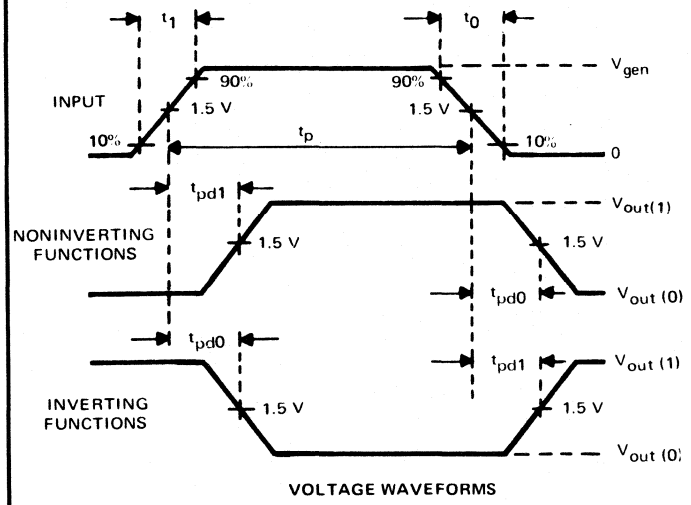
switching characteristics



TEST CIRCUIT

TEST TABLE

INPUT CONDITIONS		OUTPUT
PULSE	GND	TESTED
0	ODD	Σ EVEN
1	ODD	Σ EVEN
2	ODD	Σ EVEN
3	ODD	Σ EVEN
4	ODD	Σ EVEN
5	ODD	Σ EVEN
6	ODD	Σ EVEN
7	ODD	Σ EVEN
0	ODD	Σ ODD
1	ODD	Σ ODD
2	ODD	Σ ODD
3	ODD	Σ ODD
4	ODD	Σ ODD
5	ODD	Σ ODD
6	ODD	Σ ODD
7	ODD	Σ ODD
EVEN	NONE	Σ EVEN
ODD	0	Σ EVEN
EVEN	0	Σ ODD
ODD	NONE	Σ ODD



VOLTAGE WAVEFORMS

NOTES: 1. The pulse generator has the following characteristics: V_{gen} = 3 V, $t_1 = t_0 = 10$ ns, t_p = 500 ns, PRR = 1 MHz, and $Z_{out} \approx 50\ \Omega$.
2. Inputs not specified are open.
3. C_L includes probe and jig capacitance.
4. All diodes are 1N3064.

FIGURE 5 – SWITCHING TIMES

TYPICAL APPLICATIONS

verifying transmitted data

In this example (Figure A), data is being transmitted from data register A to data register B. Parity generators A1 and A2 are connected to generate an even-parity bit Q_{16} which is transmitted to register B. Parity checkers B1 and B2 verify the accuracy of the transmitted data and generate an even true (logical 1) or false (logical 0) parity output signal.

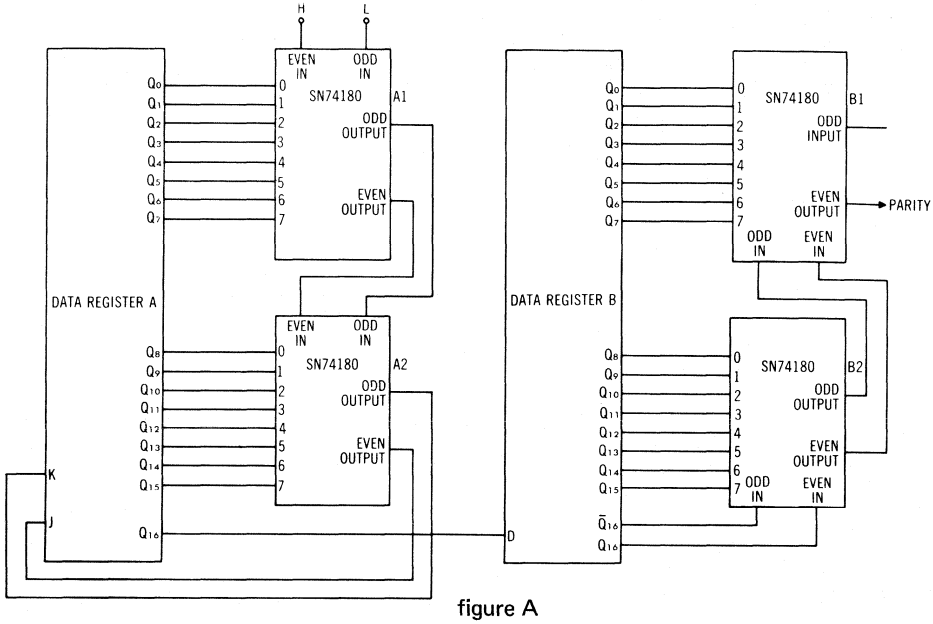


figure A

cascading for longer word lengths

The parity generator/checker may be cascaded for applications requiring longer word lengths. See Figure B. The ODD IN control is grounded for even parity generation and the EVEN IN control is grounded for odd parity generation. Two control inputs and two outputs ensure faster operation when cascading for word lengths over 8 bits, as only one gate delay is added for each additional 8-bit group. For a 32-bit word, parity can be generated in approximately 65 ns.

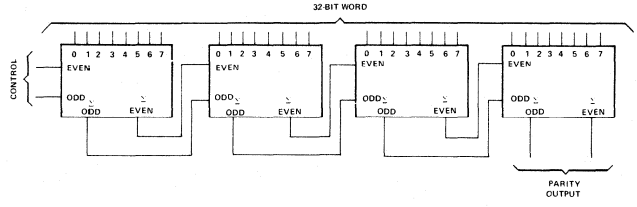


figure B

TEXAS INSTRUMENTS
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normalized fan-out

Fan-out capabilities shown on the individual data sheets in this catalog have been normalized to reflect the circuits' ability to supply a load or sink current to a number (N) of selected unit loads. In each of the three TTL families, the selected unit load consists of a circuit representative of the worst-case current required to drive one emitter of the multiple-emitter, input transistor characteristic of that family. A summary of the values used for normalizing is shown in Table I. Figures 1 and 2 illustrate the direction of the currents.

Table I. Values Used for Normalizing

SERIES	OUTPUT STATE	CHARACTERISTICS		FAN-OUT (SEE NOTE 1)	
		STANDARD TOTEM-POLE OR DARLINGTON OUTPUT	EACH STANDARD INPUT EMITTER	ACTUAL	NORMALIZED
54/74	Logical 1	I_{load} = −400 μA, $V_{out(1)}$ = 2.4 V min	$I_{in(1)}$ = 40 μA max @ V_{in} = 2.4 V	10	10
	Logical 0	I_{sink} = 16 mA, $V_{out(0)}$ = 0.4 V max	$I_{in(0)}$ = 1.6 mA max @ V_{in} = 0.4 V	10	
54H/74H	Logical 1	I_{load} = −500 μA, $V_{out(1)}$ = 2.4 V min	$I_{in(1)}$ = 50 μA max @ V_{in} = 2.4 V	10	10
	Logical 0	I_{sink} = 20 mA, $V_{out(0)}$ = 0.4 V max	$I_{in(0)}$ = −2 mA max @ V_{in} = 0.4 V	10	
54L/74L	Logical 1	I_{load} = −100 μA, $V_{out(1)}$ = 2.4 V min	$I_{in(1)}$ = 10 μA max @ V_{in} = 2.4 V	10	10*
	Logical 0	I_{sink} = 2 mA, $V_{out(0)}$ = 0.3 V max	$I_{in(0)}$ = −18 mA max @ V_{in} = 0.3 V	>11	

NOTE 1: Actual fan-out values shown here are: Logical 1 fan-out = $I_{load} \div I_{in(1)}$
Logical 0 fan-out = $I_{sink} \div I_{in(0)}$

* Limiting parameter is I_{load} of driving circuit.

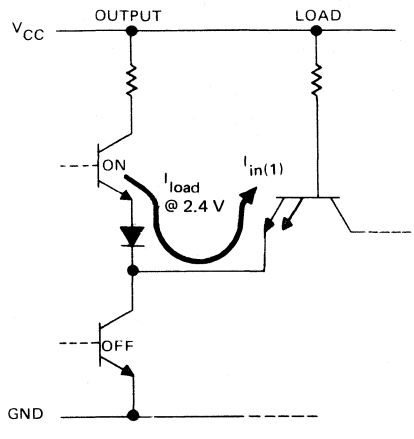

FIGURE 1–LOGICAL 1 CURRENTS

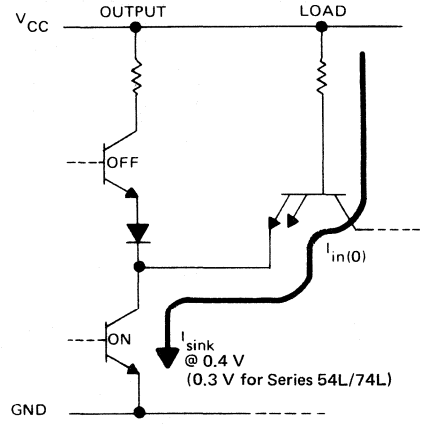

FIGURE 2–LOGICAL 0 CURRENTS

termination of unused inputs

Input current requirements for multiple emitters of the same input transistor which are connected so as to be driven by the same output are detailed in Table II.

Table II. Input Currents When Emitters are Tied Together

NUMBER OF EMITTERS TIED TOGETHER	TOTAL INPUT CURRENT REQUIRED	
	$I_{in(0)}$	$I_{in(1)}$
1	$1 \times I_{in(0)}$	$1 \times I_{in(1)}$
2	$1 \times I_{in(0)}$	$2 \times I_{in(1)}$
3	$1 \times I_{in(0)}$	$3 \times I_{in(1)}$
–	–	–
–	–	–
N	$1 \times I_{in(0)}$	$N \times I_{in(1)}$

This merely illustrates the fact that when unused inputs are tied to used inputs, only the $I_{in(1)}$ current requirements are increased. Most new TI TTL MSI circuits are characterized to drive 20 normalized logical 1 level loads to simplify the termination of unused inputs to used inputs.

combining standard, high-speed, and low-power circuits

Since various sections of digital logic systems have different speed requirements, a considerable improvement in system efficiency is realized when all three speed/power ranges of TI's compatible TTL are utilized. For example, Series 54H/74H high-speed circuits may be employed in critical arithmetic sections, while standard-speed Series 54/74 and Series 54L/74L SSI and MSI circuits can be selectively used without degradation in system performance (and without special interface circuits) to minimize power consumption.

The most efficient calculations for maximum fan-out when mixing standard, high-speed, and low-power TTL circuits are achieved by using the actual current values. As an example,consider a Series 54L/74L gate (see Figure 3) driving one Series 54/74 load (A), two Series 54L/74L loads (B and C), and four unused emitters (B_1, B_2, C_1, and C_2, two on each of the 54L74L input transistors, B and C). The calculations are shown in Table III.

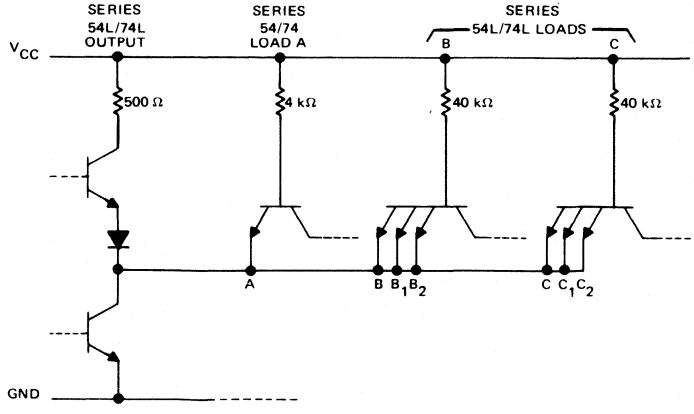

FIGURE 3

Table III. Examples of Calculating Maximum Fan-Out (Series 54L/74L)

AVAILABLE DRIVE		LOADS			
I_{load} = 100 μA	I_{sink} = 2 mA	A	$I_{in(1)}$ = 40 μA	$I_{in(0)}$ =	1.6 mA
		B	$I_{in(1)}$ = 10 μA	$I_{in(0)}$ =	0.18 mA
		B_1	$I_{in(1)}$ = 10 μA	$I_{in(0)}$ =	
		B_2	$I_{in(1)}$ = 10 μA	$I_{in(0)}$ =	
		C	$I_{in(1)}$ = 10 μA	$I_{in(0)}$ =	0.18 mA
		C_1	$I_{in(1)}$ = 10 μA	$I_{in(0)}$ =	
Less Total		C_2	$I_{in(1)}$ = 10 μA	$I_{in(0)}$ =	
Load Values: 100 μA	1.96 mA	Total	100 μA		1.96 mA
0	0.04 mA				

This illustrates the fact that a Series 54L/74L output will actually drive any combination of logical 1 and logical 0 loads which does not exceed its rating of 100-μA logical 1 drive and 2-mA logical 0 drive. The combination could just as well have been one Series 54/74 logical 0 level load, two Series 54/74 logical 1 level loads, and two Series 54L/74L loads.

generalized loading rules for the TTL families

Attempts to normalize the three families to a single set of fan-out numbers result in the apparent loss of some drive capability when compared to the calculations using actual current values. In addition, to be usable, the group of generalized fan-out numbers should be a small group of easily remembered values. A look at the actual normalized fan-out capability of each TTL family, when compared to input current requirements of the other two families, is provided in Table IV.

Table IV. Actual D-C Fan-Out Capabilities

SERIES 54/74 DRIVING SERIES 54H/74H I_{load} = 400 μA ÷ 50 μA = 8 loads I_{sink} = 16 mA ÷ 2 mA = 8 loads (A)	54H/74H and 54L/74L Normalized to 54/74
SERIES 54/74 DRIVING SERIES 54L/74L I_{load} = 400 μA ÷ 10 μA = 40* loads (B) I_{sink} = 16 mA ÷ 0.18 mA = 88.8 loads	
SERIES 54H/74H DRIVING SERIES 54/74 I_{load} = 500 μA ÷ 40 μA = 12.5 loads (C) I_{sink} = 20 mA ÷ 1.6 mA = 12.5 loads	54/74 and 54L/74L Normalized to 54H/74H
SERIES 54H/74H DRIVING SERIES 54L/74L I_{load} = 500 μA ÷ 10 μA = 50* loads (D) I_{sink} = 20 mA ÷ 0.18 mA = 111.1 loads	
SERIES 54L/74L DRIVING SERIES 54/74 I_{load} = 100 μA ÷ 40 μA = 2.5 loads I_{sink} = 2 mA ÷ 1.6 mA = 1.25† loads (E)	54/74 and 54H/74H Normalized to 54L/74L
SERIES 54L/74L DRIVING SERIES 54H/74H I_{load} = 100 μA ÷ 50 μA = 2 loads I_{sink} = 2 mA ÷ 2 mA = 1† load (F)	

*Limiting parameter is I_{load} of driving circuit.
†Limiting parameter is I_{sink} of driving circuit.

It is obvious that this group of values would be difficult to remember; however, these numbers do serve as a reference for logical 1 and logical 0 fan-out based on actual current values when the loads to be driven are all of the same family.

To develop a set of generalized loading rules which will determine fan-out from either of the three types of outputs to mixed loads consisting of any combination of 54/74, 54H/74H, or 54L/74L loads, it is necessary to ratio the various input current requirements and fan-out capabilities to the same constant. Ideally, the results will be a single set of numbers which are applicable for both logical 1 and logical 0 fan-out conditions. Testing various formulas proved that generalizing input current requirements and drive capabilities to Series 54/74 values best filled these requirements. The calculations are explained in Table V.

Table V. Ratio Calculations

LOGIC FAMILY	INPUT CURRENT REQUIREMENTS		FAN-OUT CAPABILITIES	
	Logical 1 (Base = μA)	Logical 0 (Base = mA)	Logical 1 (Base = μA)	Logical 0 (Base = mA)
Series 54/74	40 ÷ 40 = 1	1.6 ÷ 1.6 = 1	400 ÷ 40 = 10	16 ÷ 1.6 = 10
Series 54H/74H	50 ÷ 40 = 1.25	2 ÷ 1.6 = 1.25	500 ÷ 40 = 12.5	20 ÷ 1.6 = 12.5
Series 54L/74L	10 ÷ 40 = 0.25	0.18 ÷ 1.6 = 0.112	100 ÷ 40 = 2.5‡	2 ÷ 1.6 = 1.25‡

‡ Limiting parameter varies depending on type of loads driven.

When the limiting parameter of each family is considered with respect to the other two families, these ratios produce the generalized numbers listed in Table VI.

Table VI. Generalized Loading Factors

INPUT LOAD FACTOR	SERIES	OUTPUT LOAD FACTOR		
		TO SERIES 54/74	TO SERIES 54H/74H	TO SERIES 54L/74L
1	54/74	10	10	10*
1.25	54H/74H	12.5	12.5	12.5*
0.25	54L/74L	1.25†	1.25†	2.5*

*Limiting parameter is I_{load} of driving circuit.
†Limiting parameter is I_{sink} of driving circuit.

When each generalized input load factor (first column) is used to determine fan-out to loads of the same family (shaded boxes), the result in each case is 10, the same normalized value used on the data sheets.

Examples:	Input Load Factor	Output Load Factor	Fan-Out
Series 54/74	1	10	10
Series 54H/74H	1.25	12.5	10
Series 54L/74L	0.25	2.5	10

Further examination indicates that when these generalized load factors are used to determine fan-out to mixed loads (output load factor ÷ input load factor, see Table VII), the maximum loads obtained are the same as the actual d-c fan-out of the limiting parameter shown in Table IV.

The most significant variation between actual and generalized fan-out capabilities occurs when Series 54L/74L outputs are used to drive Series 54/74 and 54L/74L inputs. The generalized numbers indicate that the Series 54L/74L output will drive only one Series 54/74 load and one Series 54L/74L load simultaneously. Calculations in Table III indicate that a Series 54L/74L output will drive at least one Series 54/74 load and two Series 54L/74L loads.

Series 54/74 Input Load Factor	1
Series 54L/74L Input Load Factor	(+) 0.25
Series 54L/74L Output Load Factor	1.25

When Series 54L/74L is used to drive 54L/74L loads, the generalized fan-out number for 54L/74L outputs is actually twice as large as when driving Series 54/74 or 54H/74H loads. This can easily be compensated for by:

a. Doubling the Series 54/74 or 54H/74H input load factor and using 2.5 as fan-out capability for Series 54L/74L.

Example:

Input Load Factor—	
Series 54/74	2
(one load doubled)	
Input Load Factor—	
Series 54L/74L	(+) 0.50
(two 0.25 loads)	
Output Load Factor—	
Series 54L/74L	2.50

b. Or, double the remaining Series 54L/74L output load factor after subtracting Series 54/74 loads.

Example:

Output Load Factor—	
Series 54L/74L	1.25
Input Load Factor—	
Series 54/74	(−) 1
Remaining Output Load Factor—	
Series 54L/74L	0.25
Double	0.25 X 2 = 0.50
Input Load Factor—	
Series 54L/74L	0.50
(two 0.25 loads)	
	0

Table VII. Generalized D-C Fan-Out Capabilities To Mixed Loads

SERIES 54/74 DRIVING SERIES 54H/74H 10 ÷ 1.25 = 8 Ⓐ	54H/74H and 54L/74L Normalized to 54/74
SERIES 54H/74H DRIVING SERIES 54L/74L 10 ÷ 0.25 = 40 Ⓑ	
SERIES 54H/74H DRIVING SERIES 54L/74L 12.5 ÷ 1 = 12.5 Ⓒ	54/74 and 54L/74L Normalized to 54H/74H
SERIES 54H/74H DRIVING SERIES 54L/74L 1.25 ÷ 0.25 = 50 Ⓓ	
SERIES 54L/74L DRIVING SERIES 54/74 1.25 ÷ 1 = 1.25 Ⓔ	54/74 and 54H/74H Normalized to 54L/74L
SERIES 54/74 DRIVING SERIES 54/74 1.25 ÷ 1.25 = 1 Ⓕ	

TTL LOADING DATA

These fan-out rules are very useful for tabulating loading of outputs. However, if these maximums are reached for a particular output, it will be advantageous if the actual current values are considered, especially if loads remain which could be driven within the allowable maximum. A detailed listing of generalized load and fan-out factors for inputs and outputs of the three TTL families is provided in Tables VIII, IX, and X on the following pages.

Table VIII. Series 54/74 Generalized Loading Factors (1 of 2)

SERIES 54/74			
Device	**Location**	**Input Load Factor**	**Output Load Factor**
SN5400/7400	Any Input Any Output	1.0	10.0
SN5401/7401	Any Input Any Output	1.0	10.0
SN5402/7402	Any Input Any Output	1.0	10.0
SN5403/7403	Any Input Any Output	1.0	10.0
SN5404/7404	Any Input Any Output	1.0	10.0
SN5405/7405	Any Input Any Output	1.0	10.0
SN5410/7410	Any Input Any Output	1.0	10.0
SN5420/7420	Any Input Any Output	1.0	10.0
SN5430/7430	Any Input Output	1.0	10.0
SN5440/7440	Any Input Any Output	1.0	30.0
SN7441A	B, C, or D Input A Input Any Output	1.0 2.0	N/A
SN5442/7442	Any Input Any Output	1.0	10.0
SN5443/7443	Any Input Any Output	1.0	10.0
SN5444/7444	Any Input Any Output	1.0	10.0
SN5445/7445	Any Input Any Output	1.0	12.5
SN5446/7446	Any Input except BI/RBO BI/RBO Node Any Output except BI/RBO BI/RBO Node	1.0 2.6	12.5 5.0

SERIES 54/74			
Device	**Location**	**Input Load Factor**	**Output Load Factor**
SN5447/7447	Any Input except BI/RBO BI/RBO Node Any Output except BI/RBO BI/RBO Node	1.0 2.6	12.5 5.0
SN5448/7448	Any Input except BI/RBO BI/RBO Node Any Output except BI/RBO BI/RBO Node	1.0 2.6	6.0 5.0
SN5449/7449	Any Input Any Output	1.0	6.0
SN5450/7450	A, B, C, or D Input X and $\overline{X}$ Input Any Output	1.0 N/A	10.0
SN5451/7451	Any Input Any Output	1.0	10.0
SN5453/7453	A, B, C, D, E, F, G, and H Input X or $\overline{X}$ Input Output	1.0 N/A	10.0
SN5454/7454	Any Input Output	1.0	10.0
SN5460/7460	Any Input X or $\overline{X}$ Output	1.0	N/A
SN5470/7470	J_1, J_2, J^*, K_1, K_2, or K^* Input Clock Input Preset or Clear Input Q or $\overline{Q}$ Output	1.0 1.0 2.0	10.0
SN5472/7472	J_1, J_2, J_3, K_1, K_2, or K_3 Inputs Clock Input Preset or Clear Inputs Q or $\overline{Q}$ Output	1.0 2.0 2.0	10.0
SN5473/7473	J or K Input Clock Input Clear Input Q or $\overline{Q}$ Output	1.0 2.0 2.0	10.0
SN5474/7474	D Input Clock Input Preset Input Clear Input Q or $\overline{Q}$ Output	1.0 2.0 2.0 3.0	10.0

Table VIII. Series 54/74 Generalized Loading Factors (2 of 2)

SERIES 54/74			
Device	**Location**	**Input Load Factor**	**Output Load Factor**
SN5475/7475	D_1, D_2, D_3, or D_4 Input Clock 1-2, or Clock 3-4 Input Any Output	2.0 4.0 	 10.0
SN5476/7476	J or K Input Clock Input Clear Input Preset Input Q or $\overline{Q}$ Output	1.0 2.0 2.0 2.0 	 10.0
SN5477/7477	Any D Input Clock 1-2 or Clock 3-4 Input Any Output	2.0 4.0 	 10.0
SN5480/7480	A_1, A_2, B_1, B_2, A_C, or B_C Input A* or B* Input C_n Input Σ or $\overline{\Sigma}$ Output $\overline{C_{n+1}}$ Output A* or B* Output	1.0 1.65 5.0 	 10.0 5.0 3.0
SN5481/7481	Write 1 and Write 0 Input X and Y Inputs: Logical 0 Logical 1 S_0 or S_1: SN5481 SN7481	1.0 7.0 10.0 	 12.5 25.0
SN5482/7482	A_1 or B_1 Input A_2 or B_2 Input C_0 Input C_2 Output Σ_1 or Σ_2 Output	4.0 1.0 4.0 	 5.0 10.0
SN5483/7483	A_1, B_1, A_3, or B_3 Input A_2, B_2, A_4, or B_4 Input C_0 Input C_4 Output Σ_1, Σ_2, Σ_3, or Σ_4 Output	4.0 1.0 4.0 	 5.0 10.0
SN5484/7484	Write 1 and Write 0 Input X and Y Inputs: Logical 0 Logical 1 S_0 or S_1	1.0 7.0 10.0 	 25.0
SN5486/7486	Any Input Any Output: Logical 1 Logical 0	1.0 	 20.0 10.0
SN5490/7490	$R_{0(1)}$, $R_{0(2)}$, $R_{9(1)}$, or $R_{9(2)}$ Input BD Input A Input Any Output	1.0 4.0 2.0 	 10.0

SERIES 54/74			
Device	**Location**	**Input Load Factor**	**Output Load Factor**
SN5491A/7491A	A or B Input $\overline{CP}$ Input Q or $\overline{Q}$ Output	1.0 1.0 	 10.0
SN5492/7492	$R_{0(1)}$ or $R_{0(2)}$ Input BC Input A Input Any Output	1.0 4.0 2.0 	 10.0
SN5493/7493	$R_{0(1)}$ or $R_{0(2)}$ Input B Input A Input Any Output	1.0 2.0 2.0 	 10.0
SN5494/7494	Any Input except Preset 1 or 2 Preset 1 or Preset 2 Input Any Output	 1.0 4.0 	 10.0
SN5495/7495	Any Input except Mode Control Mode Control Input Any Output	 1.0 2.0 	 10.0
SN5496/7496	Any Input except Preset Preset Input Any Output	1.0 5.0 	 10.0
SN54100/74100	Any D Input Clock 1 or Clock 2 Input Any Output	2.0 8.0 	 10.0
SN54107/74107	J or K Input Clock Input Clear Input Q or $\overline{Q}$ Output	1.0 2.0 2.0 	 10.0
SN54121/74121	A_1 and A_2 Inputs B Input Any Output	1.0 2.0 	 10.0
SN54145/74145	Any Input Any Output	1.0 	 12.5
SN54150/74150	Any Input Any Output: Logical 1 Logical 0	1.0 	 20.0 10.0
SN54151/74151	Any Input Any Output: Logical 1 Logical 0	1.0 	 20.0 10.0
SN54152/74152	Any Input Any Output: Logical 1 Logical 0	1.0 	 20.0 10.0
SN54180/74180	Data Input Odd or Even Inputs Any Output: Logical 1 Logical 0	1.0 2.0 	 20.0 10.0

Table IX. Series 54H/74H Generalized Loading Factors

SERIES 54H/74H			
Device	Location	Input Load Factor	Output Load Factor
SN54H00/74H00	Any Input Any Output	1.25	12.5
SN54H01/74H01	Any Input Any Output	1.25	12.5
SN54H04/74H04	Any Input Any Output	1.25	12.5
SN54H05/74H05	Any Input Any Output	1.25	12.5
SN54H10/74H10	Any Input Any Output	1.25	12.5
SN54H11/74H11	Any Input Any Output	1.25	12.5
SN54H20/74H20	Any Input Any Output	1.25	12.5
SN54H21/74H21	Any Input Any Output	1.25	12.5
SN54H22/74H22	Any Input Any Output	1.25	12.5
SN54H30/74H30	Any Input Any Output	1.25	12.5
SN54H40/74H40	Any Input Any Output	2.5	37.5
SN54H50/74H50	A, B, C, or D Input X or $\overline{X}$ Input Any Output	1.25 N/A	12.5
SN54H51/74H51	Any Input Any Output	1.25	12.5
SN54H52/74H52	A, B, C, D, E, F, G, H, or J Input X Input Output	1.25 N/A	12.5
SN54H53/74H53	A, B, C, D, E, F, G, H, or J Input X or $\overline{X}$ Input Output	1.25 N/A	12.5
SN54H54/74H54	Any Input Output	1.25	12.5
SN54H55/74H55	A, B, C, D, E, F, G, or H Input X or $\overline{X}$ Input Output	1.25 N/A	12.5
SN54H60/74H60	Any Input X or $\overline{X}$ Output	1.25	N/A

SERIES 54H/74H			
Device	Location	Input Load Factor	Output Load Factor
SN54H61/74H61	Any Input Any Output	1.25	N/A
SN54H62/74H62	Any Input X or $\overline{X}$ Output	1.25	N/A
SN54H71/74H71	J1A, J2A, J1B, J2B, K1A, K2A, K1B, or K2B Input Clock Input Preset Input Q or $\overline{Q}$ Output	1.25 2.50 3.75	12.5
SN54H72/74H72	J1, J2, J3, K1, K2, or K3 Input Preset or Clear Input Clock Input Q or $\overline{Q}$ Output	1.25 2.50 1.25	12.5
SN54H73/74H73	J, K, or Clock Input Clear Input Q or $\overline{Q}$ Output	1.25 2.50	12.5
SN54H76/74H76	J, K, or Clock Input Clear or Preset Input Q or $\overline{Q}$ Output	1.25 2.50	12.5
SN54H78/74H78	J or K Input Clear Input Clock or Preset Input Q or $\overline{Q}$ Output	1.25 5.00 2.50	12.5
SN54H87/74H87	Any Input Any Output	1.25	12.5
SN54H101/74H101	J or K Inputs Preset Input Clock Input Any Output	1.25 2.50 3.0	12.5
SN54H102/74H102	J or K Inputs Preset or Clear Inputs Clock Input Any Output	1.25 2.50 3.0	12.5
SN54H103/74H103	J or K Inputs Clear Inputs Clock Inputs Any Output	1.25 2.50 3.0	12.5
SN54H106/74H106	J or K Inputs Preset or Clear Inputs Clock Inputs Any Output	1.25 2.5 3.0	12.5
SN54H108/74H108	J or K Inputs Preset Inputs Clear Input Clock Input Any Output	1.25 2.5 5.0 6.0	12.5

Table X. Series 54L/74L Generalized Loading Factors

SERIES 54L/74L				
Device	**Location**	**Input Load Factor**	**Output Load Factor**	**Output Load Factor‡**
SN54L00/74L00	Any Input Any Output	0.25	1.25	2.5*
SN54L04/74L04	Any Input Any Output	0.25	1.25	2.5*
SN54L10/74L10	Any Input Any Output	0.25	1.25	2.5*
SN54L20/74L20	Any Input Any Output	0.25	1.25	2.5*
SN54L30/74L30	Any Input Output	0.25	1.25	2.5*
SN54L51/74L51	Any Input Any Output	0.25	1.25	2.5*
SN54L54/74L54	Any Input Any Output	0.25	1.25	2.5*
SN54L55/74L55	Any Input Any Output	0.25	1.25	2.5*
SN54L71/74L71	R1, R2, R3, S1, S2, or S3 Input Clock Input Preset or Clear Input Q or $\overline{Q}$ Output	0.25 0.50 0.50	1.25	2.5*
SN54L72/74L72	J1, J2, J3, K1, K2, or K3 Input Clock Input Preset or Clear Input Q or $\overline{Q}$ Output	0.25 0.50 0.50	1.25	2.5*
SN54L73/74L73	J or K Input Clock Input Clear Input Q or $\overline{Q}$ Output	0.25 0.50 0.50	1.25	2.5*
SN54L78/74L78	J or K Input Preset Input Clear or Clock Input Q or $\overline{Q}$ Output	0.25 0.50 1.00	1.25	2.5*
SN54L86/74L86	Any Input Any Output	0.50	1.25	2.5*
SN54L91/74L91	Any Input Any Output	0.25	1.25	2.5*
SN54L93/74L93	$R_{0(1)}$ or $R_{0(2)}$ Input B Input A Input Any Output	0.25 0.50 0.50	1.25	2.5*
SN54L95/74L95	Any Input except Mode Control Mode Control Input Any Output	0.25 0.50	1.25	2.5*

*Use these numbers when driving Series 54L/74L loads only.

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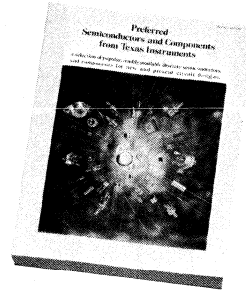

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